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COMPUTER EQUIPMENT DEPARTMENT
PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh.10-59 Sh. No. 10-58

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

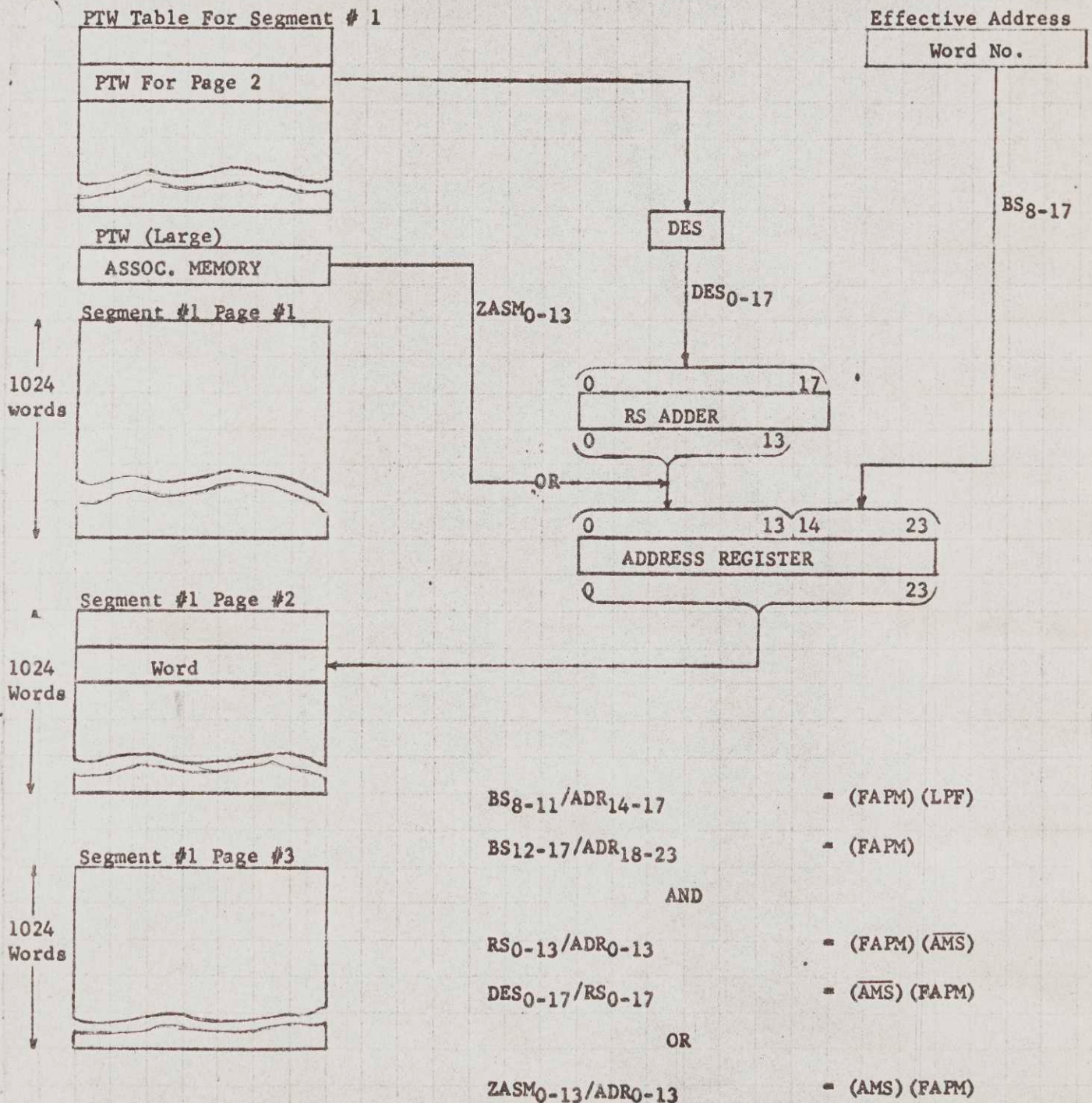


Fig. 10.1.4k Final Address Fetch Paged - Large Page, Flow Chart

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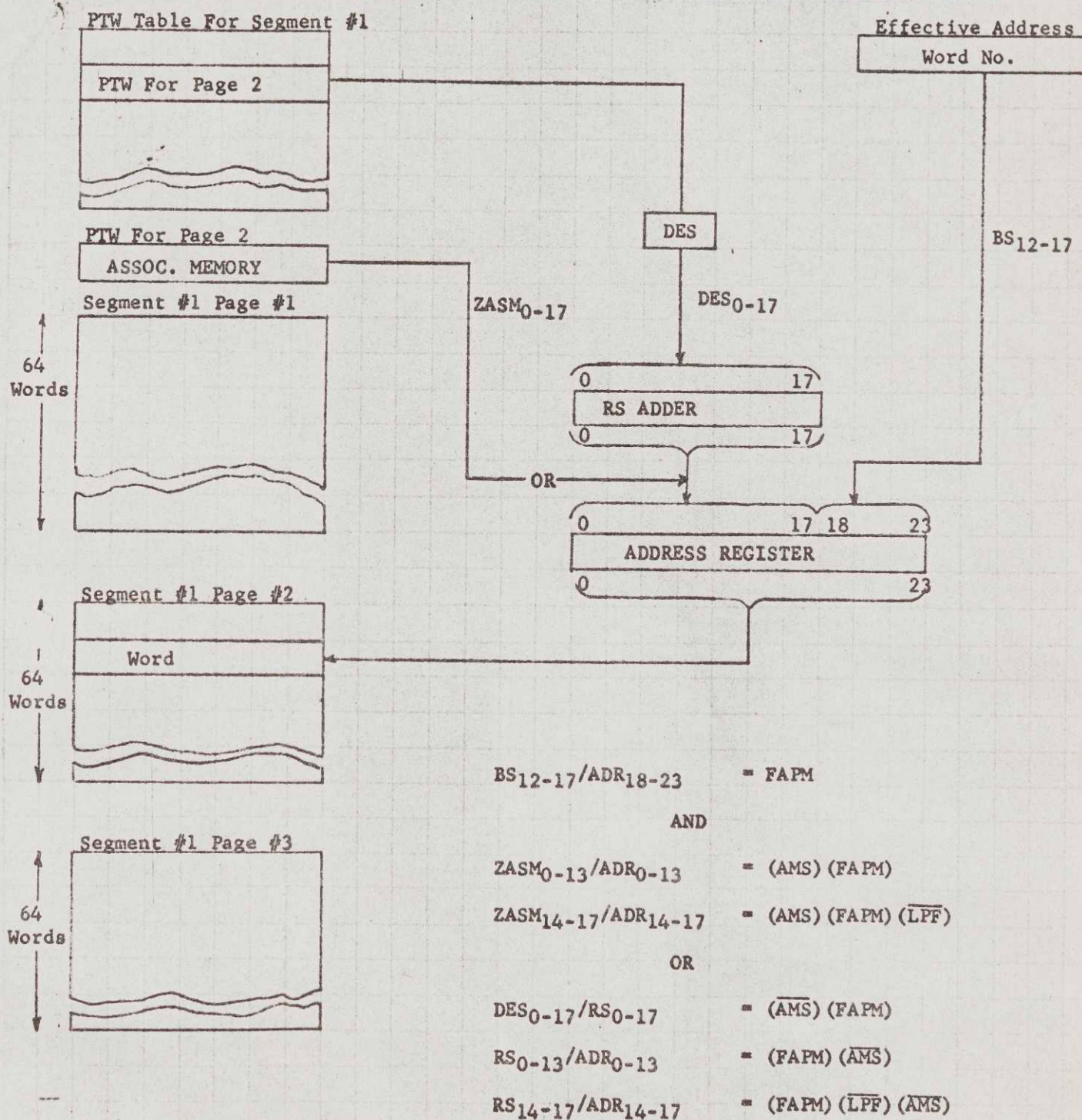


Fig. 10.1.4m Final Address Fetch Paged - Small Page, Flow Chart

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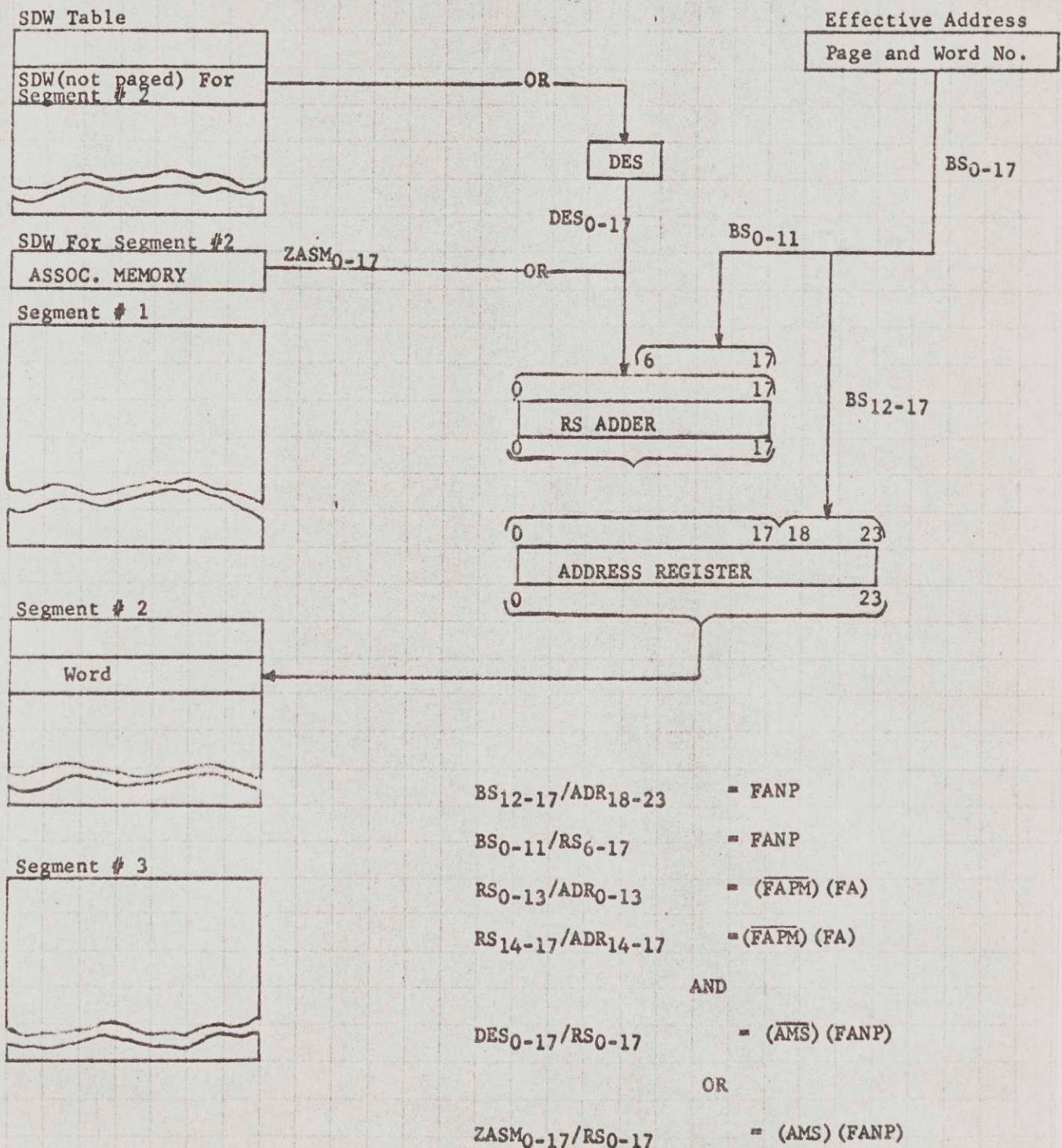


Fig. 10.1.4n Final Address Fetch - Nonpaged, Flow Chart

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Spec. No. M50EB00107

Cont. on Sh.10-62 Sh. No.10-61

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

10.1.4.2 Descriptor Generator

The Descriptor Generator receives the Descriptor field of all words from core memory, that are to be stored in the Descriptor Register. It checks for Directed Faults, Illegal Class Faults, and Access Violations as required. It generates the descriptor fields for PTWs. It presents the descriptor field to the inputs of DES₂₇₋₃₅.

Directed Fault--Anytime the Interface Frame is doing any cycle other than ABS, SWU, FAPM, or FANP ZDI lines 33-35 are checked to see if all three lines are "0." If they are the DFC line will come true indicating a Directed Fault.

Illegal Class Fault--During any cycle other than ABS, DSPTW, SWU, FAPM, or FANP the code on the three ZDI lines (33-35) will be checked. Five of these codes 000 through 100 are legitimate. If a code of 101, 110, or 111 is detected a \$ICF will be sent to the Control Frame indicating an Illegal Class Fault.

Access Violation--During a FAPM or FANP cycle the descriptor field is compared with the type of operation in progress. There are four classes of faults each dealing with a particular type of Segment or Page.

- 1) FC1 -- The descriptor has been decoded as indicating a Data Only Segment and the current operation is:
 - a) A transfer.
 - b) A store against the write permit (Slave mode and bit 30 a "0").
 - c) An access in violation of access rights (Slave mode and bit 31 a "0").
 - d) An access during a PI cycle (Instruction Fetch).

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COMPUTER EQUIPMENT DEPARTMENT
PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh.10-632 Sh. No. 10-62

TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR

10.1.4.2 - contd

- 2) FC2 -- The descriptor has been decoded as indicating a Slave Procedure Segment and the current operation is:
 - a) A store against the write permit (Slave mode and bit 30 a "0").
 - b) An access for an operand or indirect word in violation of access rights (Slave mode and bit 31 a "0").
- 3) FC3 -- The descriptor has been decoded as indicating a Procedure Only Segment and the current operation is:
 - a) A store against the write permit (Slave mode and bit 30 a "0").
 - b) An access for an operand or indirect word in violation of access rights (Slave mode and bit 31 a "0").
 - c) An access for an operand or indirect word from another segment.
 - d) A transfer from another segment, in Slave mode, to any location in this segment other than zero.
- 4) FC4 -- The descriptor has been decoded as indicating a Master Procedure Segment and the current operation is:
 - a) An access for an operand or indirect word in Slave mode.

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Spec. No. M50EB00107
 Cont. on Sh. 10-64 Sh. No. 10-63

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10.1.4.2 - contd

PTW descriptor generation - When a PTW is received from core memory bits 33-35 of its descriptor field are compared against bits 33-35 of the descriptor field of the SDW. The resultant descriptor will be as shown in Table 10.1.4.2. Bits 27 and 28 will be taken from the SDW. Bit 29 will be a 1 if bit 26 of the PTW was a "1" or if WBF is set. Bits 30-32 will be taken from the PTW if there is no Directed Fault.

Table 10.1.4.2 Resultant Descriptor
 for PTW-SDW Comparisons.

ZDI Lines 33 34 35	Descriptor Bits 33 34 35 of SDW											
	33	34	35	33	34	35	33	34	35	33	34	35
0 0 1	0	0	1	0	1	0	0	1	1	1	0	0
0 0 1	0	0	1	0	0	1	0	0	1	0	0	1
0 1 0	0	0	1	0	1	0	0	1	0	0	1	0
0 1 1	0	0	1	0	1	0	0	1	1	0	1	1
1 0 0	0	0	1	0	1	0	0	1	1	1	0	0

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PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh. 10-65 Sh. No. 10-64

TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR

10.1.4.3 Base Instruction, Multiple Load Store

During LREG and SREG instructions the Control Frame goes through its P cycles for each pair of operands. The Interface Frame will go through an appending cycle for each pair of operands. However, the address from the BS Adder will only be utilized once. From then on the address in the Address Register will be incremented by the INA logic. The \$ADR for the first Final Address cycle will set MLSF which prevents ADR₀₋₁₇ from being strobed and allows the increment logic to go into action. Each succeeding \$ADR will strobe a new count from INA into bits 18-23 of ADR. The fourth \$ADR will reset MLSF.

If the multiple load store involves a Base Frame Register BIF will be set at the same time as MLSF. If it is a store operation \$ADR will be generated by a special last pulse detector before \$INT. In all Base Frame multiple operations the CF will do only one P cycle and the Interface Frame will do only one appending cycle. CFR and IFR will remain set throughout the operation. MLSF and BIF control the increment logic and BIF determines whether the inputs or outputs of the Address Register will be used by the interface control. Both BIF and MLSF are reset by the last \$ADR as determined by the count in ADR₁₈₋₂₃. During load Base Frame Register operations a \$BORY will be sent to the Base Frame when the operand is ready. BIF is set for all Base Frame Operations except single loads.

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GENERAL ELECTRIC COMPANY
COMPUTER EQUIPMENT DEPARTMENT
PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh.10-66 Sh. No.10-65

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

10.1.5 MEMORY CONTROL

The Interface Frame controls all communication with the Memory Controller(s). It accepts instructions and addresses prepared by the Control Frame and by its own logic, and causes the appropriate action in the Memory Controller. It must decide which Memory Controller is to be used. It must respond to all signals received from a Memory Controller and remember which one it came from. This discussion will as much as possible deal only with the control logic. Only where necessary for clarity will functions of the address preparation logic or Memory Controller logic be discussed.

10.1.5.1 Configuration and Interlace

Memories of various sizes can be connected to the eight ports. The memories connected to different ports do not have to be the same size. This may result in holes in the address spectrum. The smallest size memory must be assigned the low order portion of the address spectrum. If interlace is used the memories involved must be of the same size.

The size and portion of the address spectrum assigned to each port is determined by a jumper card. There is one jumper card for each port that is used. Table 10.1.5.1 is the jumper schedule for all contemplated memory sizes. Figure 10.1.5.1 is a layout of the jumper card. Each jumper card also has three toggle switches that determines the block of addresses assigned to that port. These two factors plus the interlace control determine which port will receive the \$INT. Figure 10.1.5.1a is a logic diagram of this circuitry.

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COMPUTER EQUIPMENT DEPARTMENT
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Spec. No. M50EB00107

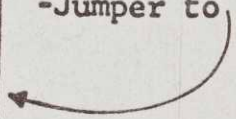
Cont. on Sh. 10-67 Sh. No. 10-66

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

Table 10.1.5.1 Jumper Schedule For Various Memory Sizes

Memory Size	A 5	B 9	C 13	D 17	E 21	F 25	G 29	H 33	J 37	K 41
16K	3	7	11	15	19	23	27	31	35	39
32K	1	3	7	11	15	19	23	27	31	35
64K	1	1	3	7	11	15	19	23	27	31
128K	1	1	1	3	7	11	15	19	23	27
256K	1	1	1	1	3	7	11	15	19	23
512K	1	1	1	1	1	3	7	11	15	19
1M	1	1	1	1	1	51	3	7	11	15
2M	1	1	1	1	1	51	51	3	7	11
4M	1	1	1	1	1	51	51	51	3	7
8M	1	1	1	1	1	51	51	51	51	3
16M	1	1	1	1	1	51	51	51	51	51

-Jumper to



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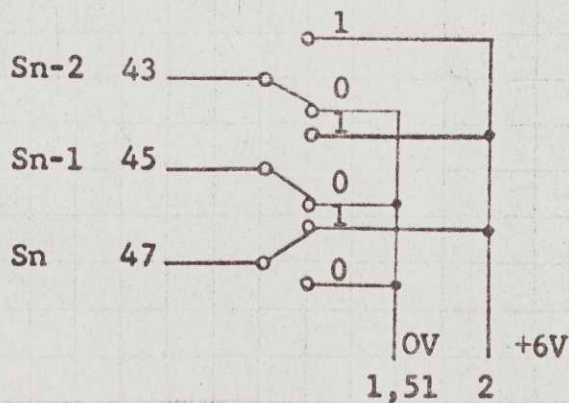
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PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh. 10-68 Sh. No. 10-67

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GE-645 PROTOTYPE PROCESSOR

Ground	1	
A0	3	
An-9	5	
A1	7	
An-8	9	
A2	11	
An-7	13	
A3	15	
An-6	17	
A4	19	
An-5	21	
A5	23	
An-4	25	
A6	27	
An-3	29	
A7	31	
An-2	33	
A8	35	
An-1	37	
A9	39	
An-0	41	
Ground	51	



A0-A9 from address
An-0-An-9 to Port Selection
Sn-Sn-2 to Port Selection

Fig. 10.1.5.1 Jumper Card Layout

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Spec. No. M50EB00107

Cont. on Sh.10-69 Sh. No. 10-68

TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR

10.1.5.1 - contd

Assume that a 64 k memory is connected to port n, the switch settings are Sn-2 and Sn set to "0" and Sn-1 set to "1", and all interlace control off. ϕ_4 and $\phi_2 + \phi_4$ will both be low. This will inhibit gates 1, 2, and 3. By comparing the jumper card with Table 10.1.5.1 for a 64 k memory and its output to the logic diagram (Fig. 10.1.5.1b) it can be seen that to enable gate 4 bits 0 through 5 of the address must be "0" and bit 6 must be a "1." This will mean that any address between 128 k and 192 k will enable the \$INT to be sent to port n, if that port is turned on.

Now assume that two 32 k memories are attached to port n and port n+1. They are to be used between 0 and 64 k, and they are to be interlaced. Both jumper cards will be jumpered for 32 k as per table 10.1.5.1. Port n will have all three switches set to "0." Port n + 1 will have Sn - 2 and Sn - 1 set to "0" and Sn set to "1." In all cases address bits 0 through 7 must be "0." With $\phi_2 + \phi_4$ high the output of its gate will depend upon address bit 22. For word pair 0 and 1 bit 22 and bit 8 will be "0," which will inhibit gates 1, 2, and 3. Therefore port n will receive the \$INT. For word pair 2 and 3 bit 22 will be "1" and bit 8 will be "0." Now gates 1, 2, and 4 will be inhibited. Therefore port n + 1 will receive the \$INT. Each word pair up to 32 k will toggle bit 22 and alternate the port that receives the \$INT. At 32 k bit 8 will become a "1" and this will reverse the order that the ports will receive the \$INT. Words will be stored as per Fig. 10.1.5.1b.

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GENERAL ELECTRIC COMPANY
COMPUTER EQUIPMENT DEPARTMENT
PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh. 10-70 Sh. No.10-69

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

10.1.5.1 - contd

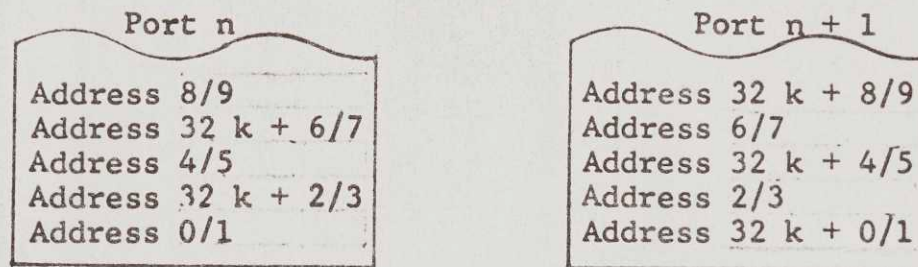
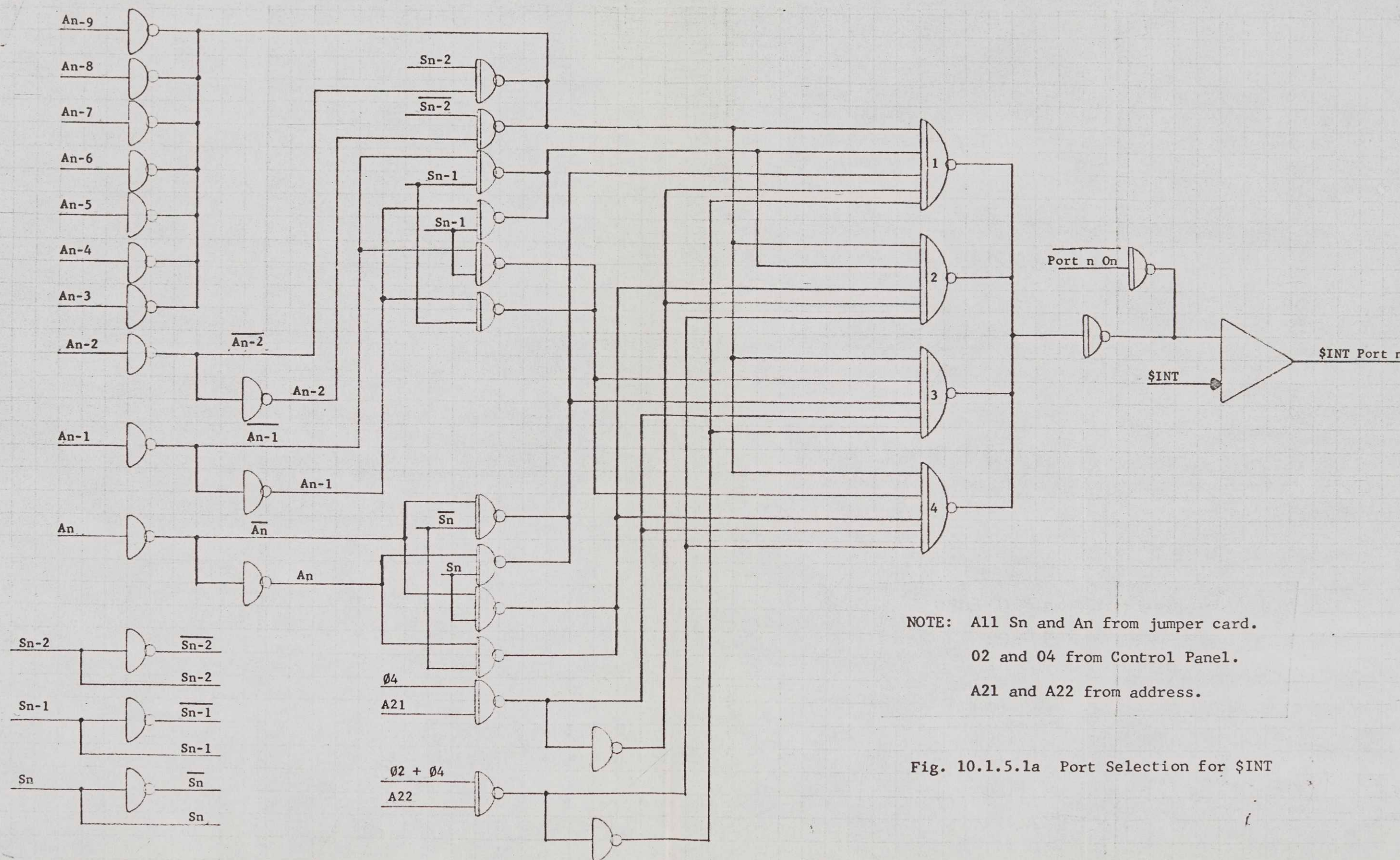


Fig. 10.1.5.1b Word Storage For Two 32K
Memories With 02 Interlace

Now assume that four 64 k memories are attached to port n, port n + 1, port n + 2, and port n + 3. They are to be used between 0 and 256 k, and they are to be interlaced. All four jumper cards will be jumpered for 64 k as per Table 10.1.5.1. Port n will have all switches set to "0." Port n + 1 will have Sn - 2 and Sn - 1 set to "0" and Sn set to "1." Port n + 2 will have Sn - 2 and Sn set to "0" and Sn - 1 set to "1." Port n + 3 will have Sn - 2 set to "0" and Sn - 1 and Sn set to "1." In all cases bits 0 through 5 of the address must be "0." With 02 + 04 high the output of its gate will depend upon address bit 22. With 04 high the output of its gate will depend upon address bit 21. For word pair 0 and 1 address bits 21, 22, 6 and 7 will be "0," which will inhibit gates 1, 2, and 3. Therefore, port n will receive the \$INT. For word pair 2 and 3 address bits 21, 6, and 7 will be "0" and bit 22 will be a "1," which will inhibit gates 1, 2, and 4. Therefore, port n + 1 will receive the \$INT. For word pair 4 and 5 address bits 22, 6, and 7 will be "0" and bit 21 will be a "1," which will inhibit gates 1, 3, and 4. Therefore, port n + 2 will receive the \$INT. For word pair 6 and 7 address

TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR

Spec. No. M50EB00107
 Cont. on Sh. 10-71 Sh. No. 10-70



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COMPUTER EQUIPMENT DEPARTMENT
PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh.10-72 Sh. No.10-71

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

10.1.5.1 - contd

bits 6 and 7 will be "0" and bits 21 and 22 will be "1," which will inhibit gates 2, 3, and 4. Therefore, port $n + 3$ will receive the \$INT. For word pair 8 and 9 the \$INT will again go to port n and it will continue to rotate in this manner up to 64 k. At that point address bit 7 will become a "1" and port $n + 1$ will receive the \$INT for word pair $64 k + 0$ and 1. See Fig. 10.1.5.1c for the pattern of word storage.

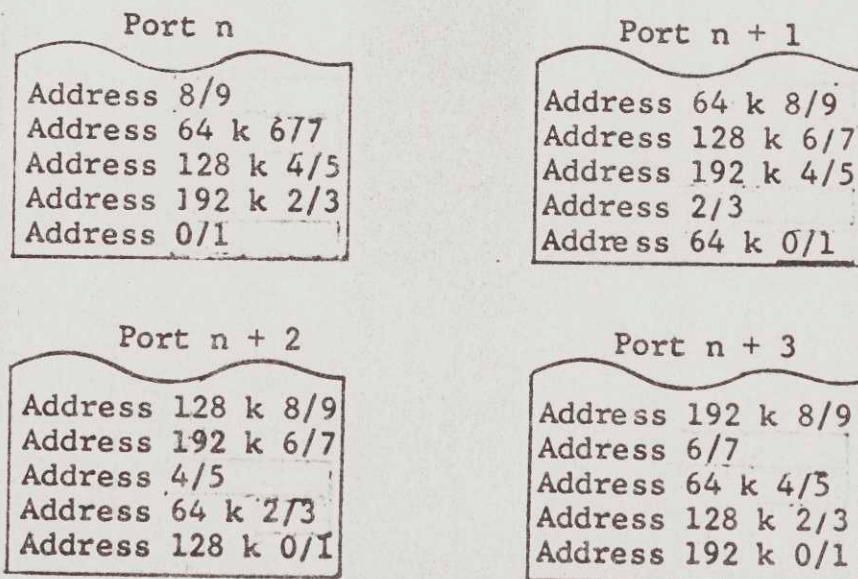


Fig. 10.1.5.1c Word Storage For Four 64K
Memories With 0 Interlace

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Spec. No. M50EB00107

Cont. on Sh. 10-73 Sh. No. 10-72

TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR

10.1.5.2 Port Selection Flip-Flops

There are two flip-flops for each port (DIR1_n and DIR2_n). The DIR1_n flip-flops remember what port received the last \$INT. The interlace logic that selected the port also enables \$INT to set the corresponding DIR1_n. If the operation is a Clear-Write Double-Precision or a Read-Alter-Rewrite DIR1_n will select the same port to receive the \$DP.

When a Memory Controller acknowledges a \$INT, it will return a \$PIN. This pulse will strobe all DIR2_n's. DIR1_n remembers which port received the \$INT, so it will control which DIR2_n will set. The output of DIR2_n is sent to the Base Frame to select the port to place on the ZDI lines during any read or first half of a Read-Alter-Rewrite operation. It also gates the Illegal Action Lines for the same port to the Illegal Action Register.

Any time the Control Frame recognizes an Interrupt it will go into a prepare Execute Interrupt Address cycle (PC). During this time the Interface Frame will select the highest priority port that has an Interrupt present, and enables the \$INT logic and the set DIR1_n for that port. When the address and the execute command for the Memory Controller are ready a \$INT is issued to it at the same time that it sets DIR1_n. The Memory Controller responds with a \$PIN, which will set DIR2_n for that port, and it places the address of its highest priority Interrupt Cell that is set on the ZDI lines. The DIR2_n's are decoded and used to complete the address received from the Memory Controller, which will be added to the Fault Vector switches to form the address of the instruction pair to be executed (see Fig. 10.1.5.2).

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PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh. 10-74 Sh. No. 10-73

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GE-645 PROTOTYPE PROCESSOR

10.1.5.2 - contd

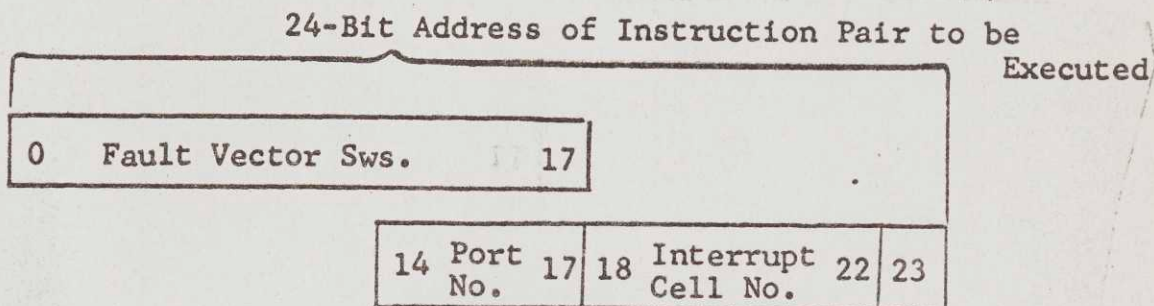


Fig. 10.1.5.2 Interrupt Address Formation

10.1.5.3 Command Logic

There are four command flip-flops that tell the Memory Controller what action is required of it. These flip-flops are strobed at the same time as the Address Register. The ZI lines from the Control Frame make up the major portion of the decode logic for these flip-flops. The operation code is decoded and the proper command flip-flops set. During appending cycles when an appending word is to be retrieved from core memory the decode logic is disabled by the lack of the FA (Final Address) level. Therefore, all four flip-flops will be reset, which is the command code for a Read-Restore Single-Precision operation. During an Indirect Word fetch EA (Effective Address) will be low preventing the ZI lines from being decoded. However, certain types of indirect sequences will cause a Read-Alter-Rewrite operation. Special conditions such as Set Written and Used bits, Execute Interrupt sequence, etc., can cause certain flip-flops to be set to perform the special operation. The output of the command flip-flops is sent to all eight ports.

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GENERAL ELECTRIC COMPANY
COMPUTER EQUIPMENT DEPARTMENT
PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh. 10-75 Sh. No.10-74

TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR

10.1.5.4 Zone Lines

The zone lines control what portion of a word is changed by a Clear-Write or Read-Alter-Rewrite operation. There are eight zone flip-flops. The portion of a word that they control is as follows:

<u>Flip-Flop</u>	<u>Bits Controlled</u>
EZ00	0-5
EZU1	6-8
EZL1	9-11
EZ02	12-17
EZ03	18-23
EZU4	24-26
EZL4	27-29
EZ05	30-35

If the flip-flop is set, it will allow the corresponding bit positions to be altered. If reset, it will prevent the bits from being altered. These eight flip-flops are strobed at the same time as the address register. The decode logic that controls these flip-flops is made up of the ZI lines from the Control Frame and by the SWU level made up in the Interface Frame. During normal operation all eight flip-flops will set. During address modification the flip-flops are controlled by the op code (ZI lines 0-8) and by bits 30-35 of the instruction word (ZI lines 12-17). During instructions involving storing 18-bit operands these flip-flops are controlled by the op code (ZI lines 0-8). During a set written and used bits cycle all flip-flops except EZU4 will be reset by the SWU level.

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GENERAL ELECTRIC COMPANY
COMPUTER EQUIPMENT DEPARTMENT
PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh.10-76 Sh. No.10-75

TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR

10.1.5.5 Illegal Action Register (IAR)

If the Memory Controller operation results in an illegal action it notifies the Processor by placing a designating code on the three Illegal Action Lines and a pulse on the \$IAL Line. A \$IAL pulse when all three Illegal Action Lines are a "0" indicates that the operation was completed correctly.

The Interface Frame contains a 3-bit Illegal Action Register that holds the code sent by the Memory Controller. When a \$IAL is received by the Interface Frame it is sent to the Base Frame and Control Frame. It also samples a gated pulse amplifier. If conditions are right it will generate a \$IAL₀₋₂, which will strobe the IAR. The conditions that must be met are:

- 1) There has been an illegal action.
- 2) The Processor is not in a fault procedure.
- 3) There is no error code in the IAR or if there is it was placed there during a buffer filling PI.
- 4) The error is not a legally masked parity error.

A parity error can be legally masked unless it occurs on an appending word fetch. In that case it will be detected and it will cause a fault.

The Interface Frame will hold the error code in the IAR as long as the Control Frame needs it. When the Control Frame goes into the fault sequence the inputs to the IAR are disabled and the next \$C will generate a \$IAL₀₋₂, which will reset all the IAR flip-flops.

COMPANY CONFIDENTIAL

GENERAL ELECTRIC COMPANY
COMPUTER EQUIPMENT DEPARTMENT
PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh.10-77 Sh. No.10-76

TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR

10.1.5.6 Data Out Register

All data to be stored in core memory is first stored in the Data Out Register (DOR₀₋₇₁) and held there until the memory has accepted it. During double-precision stores it will hold both words. In any case it allows the contributing frame to be released and continue about its business earlier than if that frame had to wait for memory. During fault and interrupt operation a "snapshot" is taken of various registers and flip-flops and this information is stored in DOR.

During normal store operations the frame that has data to be stored places that data on its Data Out lines. The Interface Frame proceeds with the preparation of the address. When the final effective address has been formed a \$INT will be generated. This pulse will strobe the data into DOR₀₋₃₅ and will issue a \$DA/S to the contributing frame. If it is a double-precision store operation the second data word will be placed on the Data Out lines and a \$DP issued to the Interface Frame. This pulse strobes this data into DOR₃₆₋₇₁, is issued to the contributing frame as the second \$DA/S, and is sent to the Memory Controller as \$DP.

During PR Control Frame cycles, the tally that is to be rewritten in core memory is stored in DOR₅₄₋₇₁.

The output of the DOR is gated onto the Data Out Lines to memory by the DDAF flip-flop. DDAF is set during the second half of a Clear-Write Double-Precision operation or during the rewrite portion of a Read-Alter-Rewrite operation, and will gate DOR₃₆₋₇₁ onto the Data Out lines to memory. At all other times DDAF will be reset, and it will gate DOR₀₋₃₅ onto the Data Out lines to memory.

COMPANY CONFIDENTIAL

GENERAL ELECTRIC COMPANY
COMPUTER EQUIPMENT DEPARTMENT
PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh.10-78 Sh. No.10-77

TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR

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PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh.10-79 Sh. No. 10-78

TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR

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GENERAL ELECTRIC COMPANY
COMPUTER EQUIPMENT DEPARTMENT
PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh.10-80 Sh. No.10-79

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

10.2 BASE FRAME DETAILED OPERATION

10.2.1 GENERAL DESCRIPTION

The purpose of the Base Frame is to hold address pointers to specific segments in memory, and to send these pointers to the Interface Frame and/or the Control Unit when requested by the Control Unit. To fulfill this function requires 11 basic registers: Eight Address Base Registers, a Procedure Base Register, a Temporary Base Function, and a Descriptor Segment Base Register. In addition to the 11 basic registers and the control logic required to select them, the Base Frame contains logic to enable the adding, loading, and storing of the 11 basic registers when GE-645 instructions that effect the Base Frame are decoded and the Interface Frame issues a start signal. Performing these two major functions, that is, Address Appending and Base Frame operations, requires circuits for: control point decode; access discrimination for access, Master/Slave and locked base restrictions; load base register fault detection; register selection and Base Frame counting of cycles for all multiple load/store operations.

Additional functions that the Base Frame performs which are not part of the address appending process are: Processor power on/off sequencing and fault detection and servicing for the Processor. These functions are located in the Base Frame because of space limitations within other areas of the Processor. The discussions of the additional functions are presented separately from that of address appending.

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GENERAL ELECTRIC COMPANY
COMPUTER EQUIPMENT DEPARTMENT
PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh. 10-81 Sh. No. 10-80

TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR

10.2.1.1 Interface Line Summary

The Interface between the Base Frame and other frames within the Processor is listed by individual line in Tables 10.2.1.1 and 10.2.1.1a. Listing is by EDA mnemonic with the last character of the mnemonic indicating the origin of the signal. Interfaces between all frames within the Processor are contained in the Processor Interface Document, G.E. drawing 43A164138.

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GENERAL ELECTRIC COMPANY
COMPUTER EQUIPMENT DEPARTMENT
PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh.10-82 Sh. No.10-81

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

TABLE 10.2.1.1 Base Frame Inputs

Mnemonic	Description
Register Frame	
QOUGD	\$GS.GF
Control Frame	
BBCRB(BCR)	INSTRUCTION IS REPEAT OR STORE
BCDBB(CDB0-17/)	CONTROL FOR DB-REG./ZDIBF0-17
BCTAB(CT)	TAG REG.MODIFICATION IDC OR DIC
BDDBB(CDB0-17/)	CONTROL FOR DB-REG./ZDIRF18-35)
DEPIB(SPI)	DECODE(SPI(DPI AND EXI AND RPI
BEADB(EA)	PREPARED ADDRESS IS FOR OPERAND
BHLTB(HALT)	LOGIC DECODE FOR STOP
BICFB(CSETIC)	LEVEL TO SET IC FLIP FLOPS
BICRB(CRESET IC)	LEVEL TO RESET IC FLIP FLOPS
BIPCB(PC)	INTERRUPT PRIORITY CHANNEL
BIPFB(IPF)	DECODE LOGIC IPR STROBE
BMPAB(FPA)	FAULT OR EXECUTE INT. IN PA CYCLE
BPNLB(CPNL SW/ZDI)	CONTROL FOR PANEL SWTCHS/ZDIRFO(35
BSPAB(CSET PA)	LEVEL TO SET PA FLIP FLOP
BSPIB(CSET PI)	LEVEL TO SET PI FLIP FLOP
BSPNB(CSET PN)	LEVEL TO SET PN FLIP FLOP
BSPTB(CSET PT)	LEVEL TO SET PT FLIP FLOP
BSPZB(CSET PZ)	LEVEL TO SET PZ FLIP FLOP
BSWNB(CSET WN)	LEVEL TO SET WN FLIP FLOP
BTDLB(TMCH(2)	TOO MUCH COUNTER EQUALS 2
BTDMB(TMCH(1)	TOO MUCH COUNTER EQUALS 1
BTDNB(TMCH(0)	TOO MUCH COUNTER EQUALS 2
BTRGB(TRG01)	TRANSFER GO GROUP SUB 1 DECODE
BYCFB(Y)	DIRECT OPERAND THE Y OF IT
BZERB(CZEROES/)	CONTROL FOR ZEROES/ZDIRFO-17
DA00B-DA02B(ZY0-2)	INST. REG. SW. EVEN

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GENERAL ELECTRIC COMPANY
COMPUTER EQUIPMENT DEPARTMENT
PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh.10-83 Sh. No.10-82

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

TABLE 10.2.1.1 Base Frame Inputs - Cont'd.

Mnemonic	Description
Control Frame - Cont'd.	
DA29B(ZY29)	INST. REG. SW. EVEN
DB00B-DB02B(ZC0-2)	INST. REG. SW. ODD
DB29B(ZC29)	INST. REG. SW. ODD
DW00B-DW08B(ZI0-8)	INST. REGISTER DECODE BUS
DW12B-DW17B(ZI12-17)	INSTRUCTION REGISTER DECODE BUS
ECICB(CIOC)	
EDVKB(DVCK)	DIVIDE CHECK FF
EEXFB(EXF)	EXECUTE FF
EFLFB(FOLF)	FAULT OVERFLOW FF
EKC1B(1KC)	TIMER 1KC OUTPUT
ELSTB(LST1)	
EMSYB(M/S)	MASTER/SLAVE FLAG ICTA8
EPINB(PIN)	
ERPDB(FD)	REPEAT DOUBLE MODE
ERPTB(FT)	REPEAT MODE
ESTPB(STOP)	STOP FLIP FLOP
ETERB(TERM)	TERMINATION OF INSTRUCTION
EWIWB(WI2)	W WAIT FLAG SUB 2 FLIP FLOP
EXDEB(XDE)	EXECUTE DOUBLE FROM EVEN LOCATION
MB00B-MB17B(BS0-17)	ADDRESS BASE ADDER
QIPRB(\$IPR)	STROBE TO SET PIR FLIP FLOPS
QSCOB(\$C)	
QZCRB(\$CSR)	
QZSRB(\$R)	
Interface Frame	
BFAAM(FA)	FINAL ADDRESS FETCH [FAPM+FANP+ABS]
EIFAM-EIFCM(IARA-C)	3-BIT ILLEGAL ACTION REG.
EP20M-EP27M(DIR20-7)	
FD30M-FD32M(DFA-C)	
QAVFM(\$AVF)	ACCESS VIOLATION FAULT PULSE
QBORM(\$BORY)	START BASE OPERATION PULSE

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GENERAL ELECTRIC COMPANY
COMPUTER EQUIPMENT DEPARTMENT
PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh. 10-84 Sh. No. 10-83

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

TABLE 10.2.1.1 Base Frame Inputs - Cont'd.

<u>Mnemonic</u>	<u>Description</u>
Control Frame - Cont'd.	
QBORM(\$BORY)	START BASE OPERATION PULSE
QDFCM(\$DF)	DIRECTED FAULT PULSE
QDSTM(\$DS)	DATA STORED PULSE
QIASM(\$SIAL)	SPECIAL ILLEGAL ACTION PULSE
QICFM(\$ICF)	ILLEGAL CLASS FAULT PULSE
QINTM(\$INT)	GENERAL STROBE
QOBFM(\$OBF)	OUT OF BOUNDS FAULT PULSE
QOCNM(\$CON)	CONNECT PULSE FROM ALL PORTS
QOIAM(\$IAL)	ILLEGAL ACTION PULSE FROM ALL PORTS
QPINM(\$PIN)	DELAYED QOPNM PULSE
QRSFM(\$RSF)	IF READY TO FAULT PULSE
QSDAM(\$DA)	READ ONLY PULSE

Maintenance Panel

SDOOT-SD35T	DATA SWITCHES
SIHFT	INHIBIT FAULT SWITCH
SIHFT	INHIBIT FAULT SWITCH
SLOOT-SL17T	FAULT VECTOR SWITCHES
SLPAT-SLPHT	PORT SWITCHES A-H
SPOFT	POWER OFF SWITCH
SPONT	POWER ON SWITCH
SQB1T	TEST CLOCK SWITCH
SQB1T	TEST CLOCK SWITCH
SSTFT	STOP ON FAULT SWITCH
SSTFT	STOP ON FAULT SWITCH
STSTT	TEST SWITCH
STSTT	TEST SWITCH

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GENERAL ELECTRIC COMPANY
COMPUTER EQUIPMENT DEPARTMENT
PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh. 10-85 Sh. No. 10-84

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

TABLE 10.2.1.1a Base Frame Outputs

Mnemonic	Description
Register Frame	
DVOOF-DV35F (ZDI RFO-35)	DATA INPUT TO REGISTER FRAME
Control Frame	
BCLTF(<u>FLT</u>)	RECOGNIZE FAULT TAG 1-3
BEOTF(BIT29?ITS?ITB)	
BFRQF(FRQ)	GROUP 6 FAULT PRESENT
BONCF(GP2 PONC)	GP2 AND PONC
BPETF(<u>PBR</u> =TBR)	CONTENTS OF PBR EQUALS TBR CONTENTS
BRROF(RR)	RELEASE \$R
BS03F(RS3)	RESET GROUP 3.4.5.6 FAULTS
BSBTf(<u>SABT</u>)	START ABORT SEQUENCE
BSFFF(SFF)	STOP FOR FAULTS
DFAOF-DFA4F(FAA-E)	FAULT ADDRESS ENCODES FAO MOST SIG.
DIOOF-DI35F(ZDIO-35)	DATA INPUT BUS
DOMRF	MEMORY READY
DZ0OF-DZ17F(ZBRI0-17)	BASE REGISTER INTERNAL BUS
EDPIF(DPI)	DOUBLE PI CYCLE
EGBOF(GB0)	GENERAL BASE INSTRUCTION F/F
EINAF	INITIALIZE
EN03F-EN05F(INC3-5)	INCREMENTOR REGISTER
EPEOF(<u>PEO</u>)	PARITY ERROR IN OPERAND
EPFIF(PFPI)	PARITY ERROR IN BUFFRD. INTRCN.
EPWPF(PWPI)	PRTY.ERR.IN PTW OR SDW FOR BUFFRD. INTRCN.
ERSTF	REMOTE STOP F/F
ESEPF(SEP)	PRTY.ERR.IN OU OPERAND
ESNOF(SNO)	SNAPSHOT ZERO F/F
ESN1F(SN1)	SNAPSHOT ONE F/F
EWCCF(WC)	WAIT FOR EXECUTE INTRPT.CELL NO.CYCLE
EWFOF(WF)	ABORT F/F
EWFBF(WFTB)	WAIT FOR TROUBLE FLIP-FLOP
QABTF(\$ABT)	END OF WF PULSE

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GENERAL ELECTRIC COMPANY
COMPUTER EQUIPMENT DEPARTMENT
PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh. 10-86 Sh. No.10-85

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

TABLE 10.2.1.1a Base Frame Outputs

Mnemonic	Description
Control Frame - Cont'd.	
QSN0F(\$SNO)	END OF SNAPSHOT 0 PULSE
QSNZF	END OF SNAPSHOT 1 PULSE
QZBCF(\$BC)	DATA IS READY
QZCEF(\$ESTR)	STROBE FOR EVEN SEGMENT TAG REGISTER
QZCOF(\$OSTR)	STROBE FOR ODD SEGMENT TAG REGISTER
Associative Memory Frame	
BCAMF(CAM)	CLEAR ASSOC.MEMORY
BSAMF(SAM)	STORE ASSOC.MEMORY
BSAZF(SAZ)	STORE ASSOC.ZERO
DX00F-DX17F(ZBRX0-17)	BASE REGISTER EXTERNAL BUS
EN01F-EN04F(INC1-4)	INCREMENTOR REGISTER
EWFOF(WF)	WF ABORT F/F
Interface Frame	
BAB4F	PH. 4 SIG. TO PORTS A+B INTERLACE
BABIF	PH. 2 OR 4 SIG. TO PORTS A+B INTERLACE
BCD4F	PH. 4 SIG. TO PORTS C+D INTERLACE
BCDIF	PH. 2 OR 4 SIG. TO PORTS C+D INTERLACE
BEF4F	PH. 4 SIG. TO PORTS E+F INTERLACE
BEFIF	PH. 2 OR 4 SIG. TO PORTS E+F INTERLACE
BGH4F	PH.4 SIG. TO PORTS G+H INTERLACE
BGHIF	PH. 2 OR 4 SIG. TO PORTS G+H INTERLACE
BP04F(GP4)	RECOGNIZE BUFFER FILLING PI PARITY FAULT
BPETF(PBR=TBR)	CONTENTS OF PBR EQUALS CONTENTS OF TBR
BROOF-BR17F	REM.OR LOC.CONTRL.FAULT VECTOR SWITCHES
BRPAF-BRPHF(PORT ON)	A-H PORT ON
BSFFF(SFF)	STOP FOR FAULTS
DD00F-DD35F(ZDOBF0-35)	36-BIT BASE FRAME DATA OUT BUS
DI00F-DI35F(ZDIO-35)	DATA INPUT BUS
DX00F-DX17F(ZBRX0-17)	BASE REGISTER EXTERNAL BUS

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GENERAL ELECTRIC COMPANY
COMPUTER EQUIPMENT DEPARTMENT
PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh.10-87 Sh. No.10-86

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

TABLE 10.2.1.1a Base Frame Outputs - Cont'd.

Mnemonic	Description
Interface Frame - Cont'd.	
EGBOF(GB0)	GENERAL BASE INSTRUCTION F/F
ENO3F-ENO5F(INC3-5)	INCREMENTOR REGISTER
EPNBF(PNB)	\$PIN AND BUFFRD.INSTRCN.REQUEST
ESNOF(SNO)	SNAPSHOT ZERO F/F
ESN1F(SN1)	SNAPSHOT ONE F/F
EWFOF(WF)	WF ABORT F/F
FS00F-FS28F(DSBRO-28)	29-BIT DESCRIPTOR SEG.BASE REGISTER
QBRYF(\$BRY)	BASE READY PULSE
QDPBF(\$DP)	
QSNOF(\$SN0)	SNAPSHOT ZERO PULSE
QSNZF(\$SN1)	SNAPSHOT ONE PULSE

Relay Box

DXBOF-DXB2F	ZXBNO-2	EXTERNAL BASE NUMBER BUS
EESOF-EES3F	ESTRO-3	4-BIT EVEN SEG. TAG REGISTER
EOSOF-EOS3F	OSTRO-3	4-BIT ODD SEG. TAG REGISTER
FA00F-FA23F	ABR0 0-23	23-BIT ADDRESS BASE REG. NO.0
FB00F-FB23F	ABR1 0-23	23-BIT ADDRESS BASE REG. NO.1
FC00F-FC23F	ABR2 0-23	23-BIT ADDRESS BASE REG. NO.2
FD00F-FD23F	ABR3 0-23	23-BIT ADDRESS BASE REG. NO.3
FE00F-FE23F	ABR4 0-23	23-BIT ADDRESS BASE REG. NO.4
FF00F-FF23F	ABR5 0-23	23-BIT ADDRESS BASE REG. NO.5
FG00F-FG23F	ABR6 0-23	23-BIT ADDRESS BASE REG. NO.6
FH00F-FH23F	ABR7 0-23	23-BIT ADDRESS BASE REG. NO.7
FP00F-FP17F	PBR0-17	18-BIT PROCEDURE BASE REGISTER
FS00F-FS28F	DSBRO-28	29-BIT DESCRIPTOR SEG. BASE REG.
FT00F-FT17F	TBR0-17	18-BIT TEMPORARY BASE REGISTER

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Spec. No. M50EB00107

Cont. on Sh. 10-88 Sh. No. 10-87

TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR

TABLE 10.2.1.1a Base Frame Outputs -contd

Mnemonic	Description
Maintenance Panel	
EAPDF	PAPZPNPT
EGBOF	GB0
EINAF	
EITBF	ITB
EITSF	ITS
ENOOF-ENO5F	INCO-5
ERWNF	IR/RI
EWFMF	WFM
	APPENDING CONTROL F/F
	GENERAL BASE INSTRUCTION F/F
	INITIALIZE POWER F/F
	INDIRECT TO BASE F/F
	INDIRECT TO SEGMENT F/F
	INCREMENTOR REGISTER
	WAIT FOR INDIRECT WITH PREVIOUS
	IR/RI -F/F
	WAIT FOR MODIFIER F/F

Junction Panel

JAOOF-JA35F	PORT A MEMORY DATA
JAMRF	PORT A MEMORY READY
JBOOF-JB35F	PORT B MEMORY DATA
JBMRF	PORT B MEMORY READY
JCOOF-JC35F	PORT C MEMORY DATA
JCMRF	PORT C MEMORY READY
JDOOF-JD35F	PORT D MEMORY DATA
JDMRF	PORT D MEMORY READY
JEOOF-JE35F	PORT E MEMORY DATA
JEMRF	PORT E MEMORY READY
JFOOF-F35F	PORT F MEMORY DATA
JFMRF	PORT F MEMORY READY
JGOOF-JG35F	PORT G MEMORY DATA
JGMRF	PORT G MEMORY READY
JHOOF-JH35F	PORT H MEMORY DATA
JHMR	PORT H MEMORY READY
JRSAF	PORT A REMOTE STOP
JRSBF	PORT B REMOTE STOP
JRSCF	PORT C REMOTE STOP
JRSDF	PORT D REMOTE STOP
JRSEF	PORT E REMOTE STOP
JRSFF	PORT F REMOTE STOP
JRSGF	PORT G REMOTE STOP
JRSHF	PORT H REMOTE STOP
KPONF	SEQUENCER PWR. ON CONTRACTOR
VP25F	725-VOLTS DC
SAB4N	INTERLACE PORTS A+B 4 PHASE SELECTION
SABIN	INTERLACE PORTS A+B 2 OR 4 PHASE SELECTION

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PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh. 10-89 Sh. No. 10-88

TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR

TABLE 10.12.1.1a Base Frame Outputs - contd

<u>Mnemonic</u>	<u>Description</u>
SCD4N	INTERLACE PORTS C+D 4 PHASE SELECTION
SCDIN	INTERLACE PORTS C+D 2 or 4 PHASE SELECTION
SEF4N	INTERLACE PORTS E+F 4 PHASE SELECTION
SEFIN	INTERLACE PORTS E+F 2 OR 4 PHASE SELECTION
SGH4N	INTERLACE PORTS G+H 4 PHASE SELECTION
SGHIN	INTERLACE PORTS G+H 2 OR 4 PHASE SELECTION
SROON-SRI7N	REMOTE PANEL FAULT VECTOR SWITCHES
SRPAN-SRPHN	PORT ENABLE A-H SWITCHES
SRPSN	INTERLACE

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Spec. No. M50EB00107

Cont. on Sh.10-90 Sh. No. 10-89

TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR

10.2.1.2 Register Formats

Prior to any discussion of Base Frame operations, it is necessary to describe the format of the 11 basic registers and the use to which specific fields within each register are put. Subsequent operations within the Base Frame are based to a large extent, on the contents of the registers involved. The various register formats are shown in Fig. 10.2.1.2.

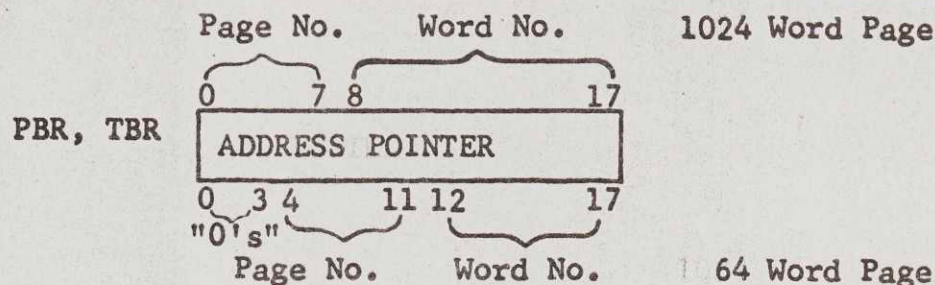
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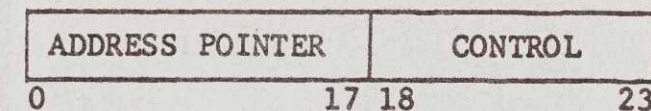
Spec. No. M50EB00107

Cont. on Sh. 10-91 Sh. No. 10-90

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOYTPE PROCESSOR



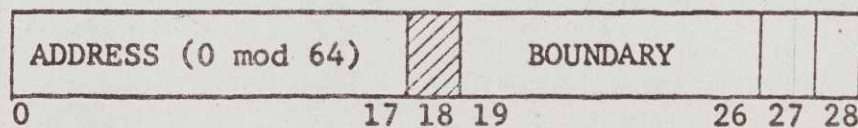
ABRn
(n=0-7)



Bits

- 0-17 - Address pointer as in the PBR, TBR
- 18-20 - External base register designator (0-7)
- 21 - Internal/External base bit ("0"/"1" respectively)
- 22 - Lock base bit (0 = Master/Slave; 1 = Master only)
- 23 - Unassigned

DSBR



Bits

- 0-17 - Base address of segment (0 mod 64)
- 19-26 - Boundary (number of pages if paged; number of blocks if nonpages.)
- 27 - Page Size 64/1024 ("1"/"0" respectively)
- 28 - Descriptor segment paged or nonpaged ("0"/"1" respectively)

Fig. 10.2.1.2 Base Frame, Register Formats

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COMPUTER EQUIPMENT DEPARTMENT
PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh. 10-92 Sh. No. 10-91

TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR

10.2.2 BASIC OPERATING CYCLES

The basic operating cycles for address appending within the Base Frame are designated by the set condition of certain flags analogous to the various prepare and wait flags of the Control Unit. These flags define:

- 1) Appending for the preparation of the address of an instruction (PI).
- 2) Appending for the preparation of the address of an operand (PA, PZ, PN, PT).
- 3) Preparing for the expected receipt of an ITS or ITB tag modified word that is pulled as the result of an RI, or IR modification (WFM).
- 4) Performing a series of operations that are considered general base operations because they involve the adding, loading, storing, or movement of data into or out of the 11 registers that contain address pointers and related control information (GB0).

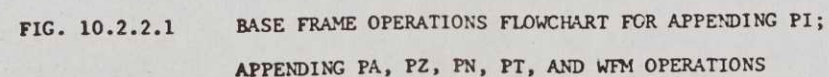
The general base operations cycle (GB0) may occur during an appending for operands cycle if a base instruction is received by the Processor and is being processed. Additionally, all operations within the Base Frame may be ignored by the Interface Frame if the Processor is addressing the Absolute mode.

10.2.2.1 Base Frame Block Diagram

General Electric drawing 43D160212, sheet 9, shows the major data flow paths between the various elements within the Base Frame. The control points and strobes shown are by EDA and engineering mnemonic. Detailed logic diagrams for the control circuitry are included or are referenced under paragraph 10.3.

NOTE: All discussion of the Base Frame in the following paragraphs is in reference to 43D160212, sheet 9, and the simplified flow chart of Fig. 10.2.2.1.

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PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh.10-94 Sh. No. 10-93

TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR

10.2.2.2 Appending Instructions (PI)

The first cycle that the Base Frame would normally go through is the prepare cycle for an instruction. This cycle is started when a ϕ Set PI level is present from the Control Frame at the time that the Control Frame issues a ϕ C to start the prepare cycle for the instruction address. Strobe ϕ C sets a flip-flop in the Base Frame that indicates the PI cycle (ϕ Set PI present) which turns on the control point to place the PBR on the ZBRX bus to the Interface Frame and inhibits any ABR selection. By definition the PBR always contains the Pointer to the base of the Procedure Segment where the instruction is contained. The Pointer remains on the ZBRX bus until the next ϕ C is received from the Control Frame to reset the PI flip-flop and close out the cycle.

10.2.2.3 Appending for Operands (PA, PZ, PN, PT)

Appending for operands when the Control Frame is in a PA, PZ, PN, or PT cycle is essentially the same as for a PI cycle, that is, sending an address pointer to the Interface Frame. However, in this case the pointer is to an external segment and the selection is more sophisticated. Selection may involve the addition of an internal base to the effective address in the Control Frame, in addition to the external base designated by the instruction, or by the ABR designated by the instruction.

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GENERAL ELECTRIC COMPANY
COMPUTER EQUIPMENT DEPARTMENT
PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh. 10-95 Sh. No. 10-94

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

10.2.2.3 - contd

Consider the "normal" case and assume that all required registers have been initialized by the Operating System and contain address pointers to specified segments and pages of segments of a users program. The first \$C from the Control Frame sets a PA cycle flip-flop and also sets an IC flip-flop if the Control Frame is working on an odd instruction; an even instruction causes the IC flip-flop to remain reset. Since we are assuming that this is the first prepare cycle for the address, no ITS tag can be present. When bit 29 of the instruction word is a "1," then the address specified is assumed to consist of a segment tag (bits 0-2 of the address) and a signed 15 bit number to be used in finding the final address. If bit 29 of the instruction word is not set to a "1," then the address specified in the instruction word is assumed to be 18 bits, is located in the segment that is currently in execution and the PBR is gated onto the ZBRX bus.

When bit 29 of the instruction word is set to "1," the even or odd segment tag register (ESTR or OSTR) is decoded to select the ABR specified by the instruction word. If this ABR is defined as external ($ABR_{21} = 1$) meaning external to the segment currently specified by the PBR, then the external ABR designated by the instruction address field is switched to the ZBRX bus. If the ABR selected is internal ($ABR_{21} = 0$) then two things happen: the selected ABR (designated ABR_n for internal) is switched to the ZBRI (internal) bus to the Control Frame, and bits 18-20 of the selected ABR_n are placed on the ZXBNI bus to another set of selection gates for the eight ARBs. Bits 18-20 of the internal base specify the linked external base, and when decoded put the linked external base on the ZBRX bus to the IF. The reason for this method of selection is because by definition an internal ABR_n may not be selected without specifying a linked external base, but an external ABR_m may be specified directly. This philosophy is a part of the total system hardware software requirements.

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GENERAL ELECTRIC COMPANY
COMPUTER EQUIPMENT DEPARTMENT
PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh. 10-96 Sh. No. 10-95

TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR

10.2.2.3 - contd

If the Control Frame was in the PA first prepare cycle for an operand, and bit 29 of the instruction word was a "1," then an internal base must be added to the address in the BS-adder in the Control Frame in addition to the external base that is sent on the ZBRX bus to the Interface Frame. What all this selection of ABRs or bases means; is that the address pointer to the instruction operand, is either selected by the tag portion of the address in the instruction word (external base to ZBRX bus), or bits 18-20 of the internal ABR (ZBRI bus to pick the external ABR); the internal ABR having been designated in the address field of the instruction word.

The output on the ZBRX bus is also present at the input to the TER. This means that the TBR always contains the Pointer that is currently on the ZBRX bus. If a satisfied conditional transfer is indicated by the Control Frame ($TRGO_1$.EA present) then the pointer in the TBR is transferred into the PBR. The PBR now contains the pointer to the new Procedure Segment. When the next $\$C$ is received from the Control Frame, the prepare cycle flip-flops may be changed and $\$TBR$ and $\$PBR$ may be generated.

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GENERAL ELECTRIC COMPANY
COMPUTER EQUIPMENT DEPARTMENT
PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh. 10-97 Sh. No. 10-96

TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR

10.2.2.4 Wait for Modifier (WFM)

The WFM cycle is entered when the Control Frame is waiting for an even indirect word that is the result of an RI/IR modification on the original or previous indirect word currently being processed. The \$C that closes out the prepare cycle for the word being processed sets an RI/IR flip-flop indicating that RI/IR was the modification tag that is resulting in an indirect word fetch from memory. When strobe \$PIN is received from memory indicating that an interrupt has been honored, the WFM flip-flop is set and the Base Frame is prepared to strobe the even or odd segment tag registers for an ITB tag, or the TBR for an ITS tag. If an ITB tag is present on the ZDI lines at the time that a \$DA is received from memory, then the state of the IC flip-flop determines whether the even or odd segment tag register is strobed and the ITB tag flip-flop is set. When an ITS tag is decoded then the TBR is strobed with ZDI₀₋₁₇ (the new address pointer) and the ITS tag flip-flop is set. Strobe \$DA also results in resetting the WFM flip-flop effectively closing out the WFM cycle for the Base Frame.

When the prepare cycle for the indirect word just brought in is started by the next \$C from the Control Frame, then the RI/IR flip-flop is reset. The ITB or ITS tag flip-flops remain set during the next prepare cycle started by \$C. Resetting of the ITB flip-flop is dependent on the second \$C that closes the next prepare cycle after an ITB tag is received; provided a Restore Control Unit instruction and effective address is not present at \$C time. Resetting of the ITS tag flip-flop is accomplished when a final effective address for an operand is obtained, and a Restore Control Unit instruction is not present. What this means is that for ITB modification the segment tag register specifies the ABR containing the new pointer and is not changed until the instruction is executed and two new instructions are brought into the instruction register in the Control Unit.

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Spec. No. M50EB00107

Cont. on Sh. 10-98 Sh. No. 10-97

TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR

10.2.2.4 - contd

Therefore the ITE tag flip-flop is reset after the first prepare cycle following the WFM cycle since it is only used to switch the internal base to the ZBRI bus for the first prepare cycle. The ITS tag flip-flop on the other hand is only reset when a final effective address is present, since the pointer in the TBR must be present on ZBRX to obtain the final address.

10.2.2.5 General Base Operations

When an instruction is being processed by the Control Unit that involves changing the Base Frame registers, or effecting operations related to the Base Frame, then strobe \$BORY is received from the Interface Frame initiating a general base operation (GBO). Strobe \$BORY generates strobe \$B, the internal strobe for a general base operation, which in turn sets a GBO flip-flop. From this point on the specific operations performed by the Base Frame are dependent on the instruction being executed. Base Frame instructions are listed on G.E. drawing 43D139962. Generally speaking, the following actions occur:

- 1) \$BORY is received, generating \$B and setting the GBO flip-flop.
- 2) The proper control points are turned on for the specific instruction (see Base Frame "Spec Chart" 43D139962).
- 3) Control of the strobes for the various registers is determined by the specific instruction, Master/Slave processor mode and lock base bit conventions on the ABRs.

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PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh. 10-99 Sh. No. 10-98

TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR

10.2.2.5 - contd

- 4) If the instruction involves loading any of the ABRs (specifically ADB_n , EAB_n , EAP_n , LBR_n , $LDCF$, or TSB_n) then a fault strobe ($\$FLT$) is generated if the Master/Slave lock base conventions are not met (trying to load an ABR in Slave mode when the lock base bit is set).
- 5) The generation of a strobe $\$BC$ indicating that base operations are complete is sent to the Control Frame. Again, the generation of $\$BC$ is dependent on the specific instruction. Strobe $\$BC$ is used to generate a $\$C$ closing out the current cycles in Control and Base Frames.

In general, refer to the "Spec Chart" for the specific operation involved, and the description of the instructions in Part I of this EPS. The detailed discussion in paragraph 10.3 for some representative instructions indicate the specific actions that occur.

10.2.3 OPERATION OVERLAP

In discussing each basic operating cycle the reader may have gotten the impression that the cycles were distinctly separated from one another; such is not the case. As an example, consider the various cycles that take place for an instruction and operand fetch that involves a general base instruction.

A strobe $\$C$ is received from the Control Frame to initiate appending for an instruction (PI), the contents of the PBR are put on the ZBRZ bus to the IF Frame, a second strobe $\$C$ is generated, and the instruction word is fetched. When the Control Frame is going for an operand fetch the next $\$C$ that initiates a PA cycle ultimately results in the contents of an external ABR_m or the TBR being put on the ZBRX bus to the IF Frame. However, if the instruction fetched

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PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh.10-100 Sh. No.10-99

TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR

10.2.3 - contd

during the previous PI cycle involved a Base Frame operation and no RI or IR modification was involved, then the Control Frame stops and the Interface Frame issues a strobe \$BORY to the Base Frame to start a general base operation. When a general base operation is started, the append flip-flop outputs are inhibited (the actual inhibit varies with the EAB_n and EAP_n instructions), but not reset. Only the second \$C closing the PA cycle can reset the append flip-flop. With the generation of the \$BC that indicates that a base operation is complete, the inhibits are removed. The Base Frame then returns to a "normal" appending for operands cycle until the next \$C to close the current PA cycle resets the append flip-flop. This strobe \$C is immediately after a \$BC is sent to the Control Frame.

Operations within the Base Frame for general base operations may involve multiple access to memory before completion of the specific operation. In these cases the core location to go to, or fetch data from is formed prior to the Interface Frame issuing a strobe \$BORY. The pointer on the ZBRX bus is strobed into the address register in the Interface Frame (via the RS-adder) concurrent with the receipt of a \$BORY. This pointer was selected as soon as a \$C is received from the Control Frame as previously explained. When any modification is specified in the original or indirect word, then strobe \$BORY is not received until the final address fetch. What this means is that a general base operation cannot be started unless the Control Frame is in the cycle for a final address fetch. Fig. 10.2.3 illustrates the various cycles and how they overlap showing only relationships not actual timing, and using \$C as a reference.

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COMPUTER EQUIPMENT DEPARTMENT
PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh. 10-101 Sh. No.10-100

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

10.2.3 - contd

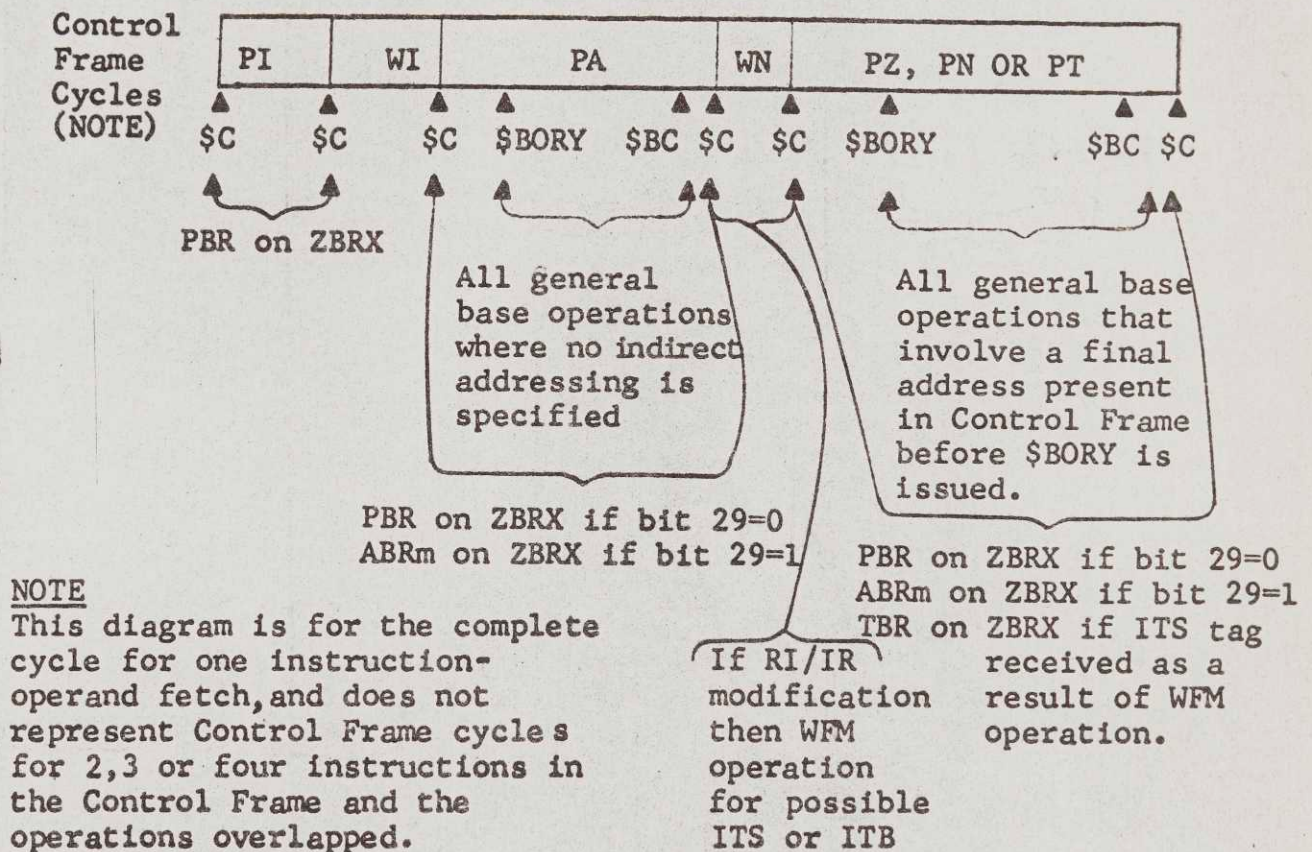


Fig. 10.2.3 Base Frame Operating Cycles in Relation to Control Frame Cycles.

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PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh.10-102 Sh. No.10-101

TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR

10.2.4 STROBE GENERATION

Strobe generation within the Base Frame may be generalized into two categories: external and internal. The external strobes received are from the Control Frame to initiate normal appending operations for instructions and operands (\$C, \$PIN); and from the Interface Frame to initiate and control general base operations (\$BORY, \$DA, \$DS). Internal strobes (\$B) to sequence operations within the Base Frame are only used during general base operations. The internal strobes are generated as a function of one or all of the external strobes from the Interface Frame (\$BORY, \$DA, \$DS) and the specific Base Frame instruction being executed. The one exception is strobe \$DA which is used to set the ITS or ITB flip-flops when in WFM cycle.

10.2.4.1 External Strobe Utilization

The five external strobes are utilized as follows.

- 1) Strobe \$C -- reamplified and used to initiate or terminate the normal appending cycle for instructions and operands, and if an RI/IR modifier is specified by the tag of the instruction word, set the RI/IR flip-flop in preparation for a WFM cycle.
- 2) Strobe \$PIN -- reamplified and used to set the WFM flip-flop in anticipation of the receipt of an ITS or ITB modifier in the even indirect word of a pair pulled from memory as a result of RI/IR modification to an even memory address.
- 3) Strobe \$BORY -- used to initiate the internal \$B chain for general base operations. \$BORY is never received from the Interface Frame except when a final effective address is present in the Interface Frame.

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GENERAL ELECTRIC COMPANY
COMPUTER EQUIPMENT DEPARTMENT
PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh.10-103 Sh. No.10-102

TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR

10.2.4.1 - contd

- 4) Strobe \$DA -- delayed to obtain \$DA Δ to compensate for pulse versus d-c propagation delay in the data lines from memory. Strobe \$DA Δ with a small compensating delay is used to strobe the ITB and ITS flip-flops for WFM cycles and initiate an internal \$B for general base operations. When executing the LDCF and ADB n instructions, \$DA Δ is delayed approximately 250 nanoseconds further to allow the BS-adder in the Control Frame to stabilize before initiating a \$B.
- 5) Strobe \$DS -- received from the Interface Frame as a result of double precision store operations effecting the base frame registers and the increment counter. Strobe \$DS's signify that data is stored in the Data-Out Register in the Interface Frame and initiate a \$B as does \$BORY and \$DA.

10.2.4.2 Internal Strobe Utilization

The internal strobe chain consists of a gated-amplifier delay line loop that is initiated by \$BORY + \$DA Δ + GBO + \$DS + GBO to generate \$B $_{10}$, \$B $_{11}$, \$B $_{13}$, and \$B Δ for use throughout the Base Frame during general base operations. Any one of the three strobes mentioned can generate one set of strobe \$B's (\$B $_{10}$, \$B $_{11}$, \$B $_{13}$, and \$B Δ). For instructions TSB n , LDCF, CAM, EAB n , EAP n , or a load base fault, a feedback loop is enabled and additional \$B's are generated to finish the various operations required. The \$B's are used to step the increment counter, generate (subject to restriction) \$ABR0-17,18-21,23,22; \$PBR; \$TBR; \$ITB; \$ITS; \$BRY; \$FLT and \$DP throughout the base frame. The only difference between \$B's is for the compensating delay required for circuit timing.

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GENERAL ELECTRIC COMPANY
COMPUTER EQUIPMENT DEPARTMENT
PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh. 10-104 Sh. No. 10-103

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

10.2.5 INCREMENT COUNTER

Many of the instructions classified as general base instructions involve more than one specific operation. To keep track of the number of the specific operation, an increment counter is used. This counter is a serial binary counter that is incremented every time $\$B_{13} \cdot GBO \cdot \overline{\$SBC}$ is true. The parallel outputs of the increment counter are decoded for counts of 0, 1, 2, 5, 7, and 31. Counts of 0, 1, 5, 7, and 31 are used for instructions that take 0, 2, 6, 8, and 32 steps respectively. The increment counter is not incremented with the first or last $\$B_{13}$ received, and only contains the number of operations that have been completed. The different instructions by number of operations are:

- 1) One step - LBRn, EABn, ADBn, SBRn, LDBR, SDBR, CAM
- 2) Two step - EAPn, LDCF, RTD, STCD, STPn, SAZ, TSBn
- 3) Six step - SCU, RCU
- 4) Eight step - LDB, STB
- 5) Thirty-two step - SAM

When the final $\$SBC$ is generated to complete the general base operations cycle, the GBO flip-flop is reset resetting the increment counter.

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GENERAL ELECTRIC COMPANY
COMPUTER EQUIPMENT DEPARTMENT
PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh.10-105 Sh. No. 10-104

TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR

10.2.6 LOAD BASE FAULT DETECTION

Fault detection circuits are included for those instructions that involve changing an address base register: ADBn, EAB, EAP, LBRn, LDCF, and TSBn. No fault is generated for the LDB instruction. Generation of the fault is a function of the selected ABR, a general base operation, the specific instruction and the Master/Slave lock base bit restrictions (all load base instructions may only be executed in Master mode of if $ABR_{22} = 0$). If an attempt is made to change the specified ABR when not in Master mode, and the lock base bit (ABR_{22})="1", then a ϕ Set FLT level is generated which inhibits the generation of a \$BC and permits the generation of a \$FLT on receipt of the next $\$B_{13}$.

10.2.7 EVEN AND ODD SEGMENT TAG REGISTERS (ESTR And ϕ STR)

The even and odd segment tag registers as the names imply are used to hold the segment tag and bit 29 of the instruction word for the even (ESTR) and odd (ϕ STR) instructions in the Y- and C-registers of the Control Frame. In addition, if an ITB modifier is received as a result of a WFM Base Frame operation, the new segment tag (designating ABR 0 through 7) is strobed into ESTR or ϕ STR. The strobes are received concurrent with the strobes for the Y- and C-registers in the Control Frame for normal appending on instructions, and for an RCU instruction. Strokes for the ITB modifier received tag are generated internal to the Base Frame as a result of the \$DA received during the WFM cycle. With ITB modification a "1" is forced into $ESTR_3$ or ϕSTR_3 to simulate bit 29 = 1 of the instruction word.

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PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh.10-106 Sh. No.10-105

TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR

10.2.8 DATA IN (ZDI) SWITCH

All data from all eight possible Memory Controllers to the Processor is received at Ports A-H of the Base Frame for distribution to other areas within the Processor. Port selection signals from the Interface Frame determine which port is enabled at which specific time. Associated with the ZDI switch is a 18 bit buffer for direct operands from the Control Frame to the OU. This is because data distribution of the direct operand for DU, or DL modification is also on the ZDI bus to the Register Frame of the OU.

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PHOENIX, ARIZONA

Cont. on Sh. 10-107 Sh. No. 10-106

10.3 DETAILED OPERATION (see GE drawings 43D1060212, sheet 9, and 43D163422)

Appending for Instructions (PI) takes place whenever the Control Frame generates DSPILB (ϕ Set PI) and QSCOLB ($\phi\phi$) on the input lines to the Base Frame. Appending takes place whether or not the Processor is in the Absolute or Append mode of operation. The decision on whether or not to use the information present on the DX_F(ZBRX) bus is a function of the Interface Frame and the Control Frame. Whether or not to use the information present on the DN_F(ZBRI) bus is a function of the Base Frame. Refer to the timing diagram (Fig. 10.3.1.).

The sequence of events that take place begins with the presence of DSPILB ($\bar{c}$ Set PI) from the Control Frame prior to the receipt of QSCOLB ($\$C$). When $\$C$ is received, flip-flop EPIOF (PI) is set. The set output of the PI flip-flop is the BRXPOF ($\bar{c}$ PBR₀₋₁₇/ZBRX₀₋₁₇) control level that places the contents of the Procedure Base Register (PBR) on the ZBRX bus to the Interface Frame via the ZDO switch, and blocks the control level generation for the eight address Base Registers; specifically, BRXOF ($\bar{c}\$EX$). Since by definition the Procedure Base Register contains the address of the base of the Procedure Segment, and all instructions will be contained in the Procedure Segment, only PBR₀₋₁₇ is required of the Base Frame during PI cycles and address appending. When the second $\$C$ is received from the Control Frame the PI flip-flop is reset and the control level (BRXPOF) to turn on the PBR/ZBRX switch is removed.

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GENERAL ELECTRIC COMPANY
COMPUTER EQUIPMENT DEPARTMENT
PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh.10-108 Sh. No.10-107

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

DSPILB(ϕ Set PI)

EPIOIF (PI)

QSC01B(ϕ C)

QPI01F(PI)

BRXPOF(ϕ PBR₀₋₁₇/ZBRX)

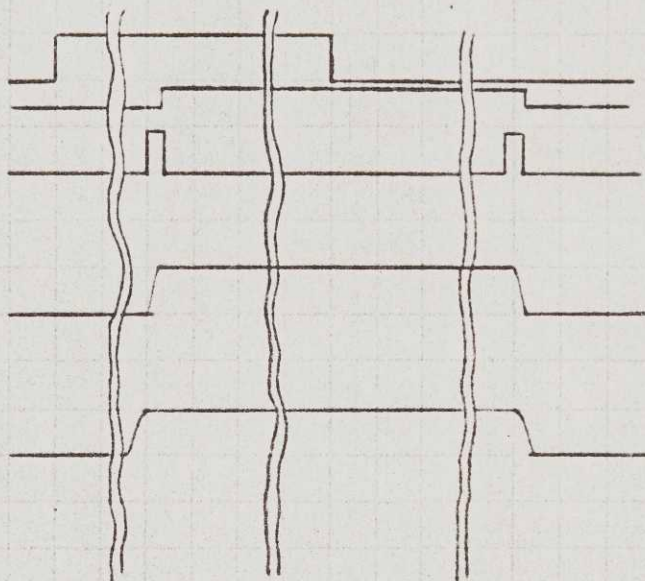


Fig. 10.3.1 Appending Instructions (PI),
Timing Diagram

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Spec. No. M50EB00107

Cont. on Sh.10-109 Sh. No.10-108

TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR

10.3.2 APPENDING OPERANDS (PA, PZ, PN, PT)

Address appending for operands is essentially the same for PA, PZ, PN, or PT cycles. As in appending for instructions, the Base Frame goes through the appending process whether the Processor is in Absolute or Append mode of operation. Refer to the timing diagram (Fig. 10.3.2) during the following discussion.

Control level DAPD1F ($\bar{c}$ Set PA+PZ+PN+PT), resulting from levels sent from the Control Frame in conjunction with QSC01B(\$C), set the EAPDF flip-flop indicating that appending is required. With the EAPDF flip-flop set, the even or odd segment tag register is switched to the one of eight decoders for both internal and external base register selection. Which segment tag register is switched is determined by the EICOF(IC₁ and IC₂) flip-flops. When register ($\emptyset$ STR) is selected; reset causes the even segment tag register (ESTR) to be selected.

10.3.2.1 Internal Base Selection

Selection of an internal base is accomplished when the selected segment tag register at DBI_F is decoded to pick one of the eight address base registers that has been designated an internal base by having its internal/external base bit (bit 21) set to 0. Control level BRN_OF which selects the register is not generated unless F+21OF (complement of bit 21 of the ABR designated by the segment tag register) indicates that the selected register is internal. The selected base register is put on the ZBRI bus to the Control Frame and ultimately the BS-adder, via the ZEROS switch. This switch is only open during the PA cycle of an appending operation with bit 29 of the instruction word set, for an ITB modifier during an appending operation, and for EABn and EAPn instructions during general base operations. At other times, 0's are sent to the BS-adder in the Control Frame instead of the selected internal base.

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Spec. No. M50EB00107

Cont. on Sh.10-110 Sh. No.10-109

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROROTYPE PROCESSOR

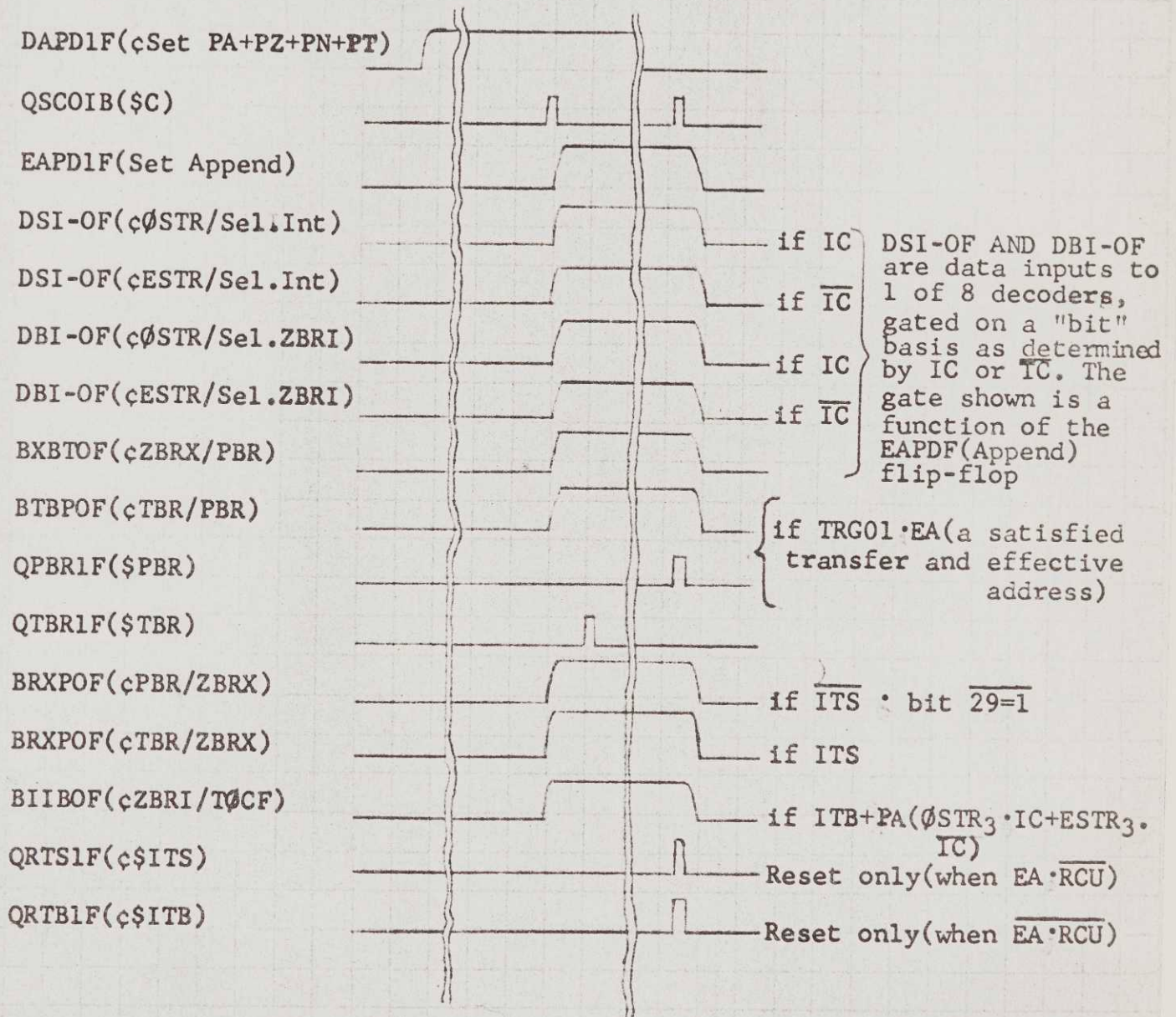


Fig. 10.3.2 Appending Operands (PA, PZ, PN, PT),
Timing Diagram

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Spec. No. M50EB00107

Cont. on Sh.10-111 Sh. No.10-110

TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR

10.3.2.2 External Base Selection

The output of the selected tag register (ESTR or OSTR) at DSI_1F is decoded by the one of eight octal to decimal decoder to select one of the eight ABR's (control points DRX_1F). If the selected ABR contains an external base, as signified by a 1 in bit 21 (F_211F) then level BEXTOF is generated and the (BXXX1F) input becomes one of the enable inputs to one of the two ABR selection gates associated with the ABR that generates BRXOF ($\bar{c}SEX$)--the control of ABR₀₋₇ to ZBRX. In this particular case, ($\bar{c}TBR_{0-17}/ZBRX_{0-17} + \bar{c}PBR_{0-17}/ZRX_{0-17}$)(BXXX1F)(DRX_1F), for the register selected, generates ($\bar{c}SEX$). The complement of bit 21 (0), of the register selected is used to generate level BNNNOF which inhibits the selection of another ABR via the NAND gate associated with the DXB_1F (ZXBN) bus. Bus ZXBN is the internal base bus that is decoded for the selection of the associated external base if an internal base is specified by the segment tag register. The philosophy here is that an internal base designated by the segment tag register must specify in bits 18-20 of its control field, the associated, or linked external base. If an external base is specified by the segment tag register no associated internal base can be specified and none will be put on the ZXBN bus.

If bit 21 of the ABR selected by DRX_1F is 0, indicating that an internal base is specified by the segment tag register, bits 18-20 of the selected register are switched on the ZXBN bus, BNNNOF is enabled and BXXX1F disabled. The NAND gate associated with the selection of an external base when specified by the segment tag register is now disabled. When bit 21 of the selected ABR is 1 indicating an external base then $\bar{c}SEX$ is a function of ($\bar{c}TBR_{0-17}/ZBRX_{0-17} + \bar{c}PBR_{0-17}/ZBRX_{0-17}$)(BNNNOF)(ZXBN₀₋₂), the

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PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh.10-112 Sh. No.10-111

TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR

10.3.2.2.- contd

NAND gate output that is associated with internal/external base selection. When performing the base instructions STB and SBRn with the GBO flip-flop set, BXXX1F is permanently enabled and BNNNOF disabled to force all base registers, when selected by the one of eight decoder, on the ZBRX bus regardless of whether the ABR's are designated internal or external.

The output of the selected external base register (or the PBR during periods when bit 29 of the instruction word = 0) on the ZBRX bus is gated to the input of the Temporary Base Register by control level BXBTOF. The data is settled by the time QTBR1F (\$TBR) strobes ZBRX₀₋₁₇ into the TBR (approximately 290 nanoseconds after \$C). In addition to ZBRX₀₋₁₇ being strobed into the TBR it is placed on the DD__OF (ZDO) switch bus to the Interface Frame. Control of BXB00F for the ZBRX portion of the ZDO switch during PA, PZ, PN, and PT appending operations is dependent on BSN01B ("Snapshot 0") from the Control Frame, that is, when a "snapshot" is taken as the result of a recognized fault ZBRX is not sent to the Interface Frame.

Transfer of Control

When a satisfied transfer of control has been determined by the Control Frame, both BEAC1B (EA) and BZDC1B (TRG01) are present in the Base Frame. This causes BTBPOF (¢TBR₀₋₁₇/PBR₀₋₁₇), the control point for placing TBR into PBR, to be enabled. Concurrent with the reception of the next \$C from the Control Frame, QPBR1F (\$PBR) is generated strobing the contents of TBR into PBR; \$PBR occurs after the new external base had been strobed into the TBR. After PBR has been loaded with the new external base the normal instruction address preparation sequence for PI is started by the Control Frame.

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PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh.10-113 Sh. No.10-112

TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR

ITS Modifier

If an ITS modifier is detected as the result of a previous WFM Base Frame operation; EITS1F(ITS). EAPD1F(Append). EGB00F(GB0) cause BRXT0F (ϕ TBR0-17/ZBRX0-17) to switch the TBR onto the ZBRX bus and inhibit the selection of an external base from the eight ABR's. Level ϕ TBR0-17/ZBRX0-17 generation is dependent on the append level generated by (PA+PZ+PN+PT).\$C received from the Control Frame; and consequently places TBR0-17 on the ZBRX bus only in the time interval between \$C's. The TBR had been loaded previously with the new segment base pointer from ZDI0-17 during the WFM Base Frame cycle.

ITB Modifier

When an ITB modifier is detected as the result of a previous WFM Base Frame operation, the even or odd segment tag register contains the tag to the new external ABR. As a result, the external base is selected in the normal manner as previously described for PA, PZ, PN, and PT operand fetches.

10.3.2.3 ITS and ITB Reset

Reset of the EITBF(ITB) flip-flop is accomplished when (RCU.EA)(PA+PZ+PN+PT)(\$C11) is satisfied at the end of the prepare cycle for an operand where an ITB modifier is specified. The first \$C11 received that started Base Frame operations does not reset the ITB flip-flop since the PA, PZ, PN, PT(EAPDF) flip-flop input is not present till after the first \$C11. This is due to built in delay from \$C11 time to the receipt of the PA, PZ, PN, PT level received at the ITB flip-flop reset input.

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PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh.10-114 Sh. No10-113

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROROTYPE PROCESSOR

10.3.2.3 - contd

The EITSF (ITS) flip-flop is reset in the same manner as the ITB flip-flop but when (RCU·EA) ($\$C_{11}$) is satisfied. This condition exists only when the final effective address (EA) for the operand is prepared by the Control Frame and no RCU instruction has been decoded by the Control Frame.

Differences in the resets are because in ITB modification the new external base tag has been strobed into the applicable segment tag register, and base selection is performed normally for the first prepare (PA) cycle. The ITB flip-flop level must be "up" in anticipation of an internal base being specified by the new segment tag register (and consequently, ABR) contents. The level indicating an ITS modifier, on the other hand, must be "up" to allow the ϕ TBR/ZBRX control level to keep the contents of the TBR on the ZBRX bus until a final effective address is prepared; TBR containing the new address pointer as previously specified.

10.3.3 WAIT FOR MODIFIERS (WFM) OPERATION

The third specific operation that the Base Frame performs is to prepare for the receipt of an ITS or ITB modifier in an even indirect word of a even odd pair pulled as a result of RI/IR modification, and to load the received data present on the ZDI lines from memory into the applicable segment tag register (ITB modification), or temporary Base Register (ITS modification). See timing diagram (Fig. 10.3.3) during the following discussion.

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

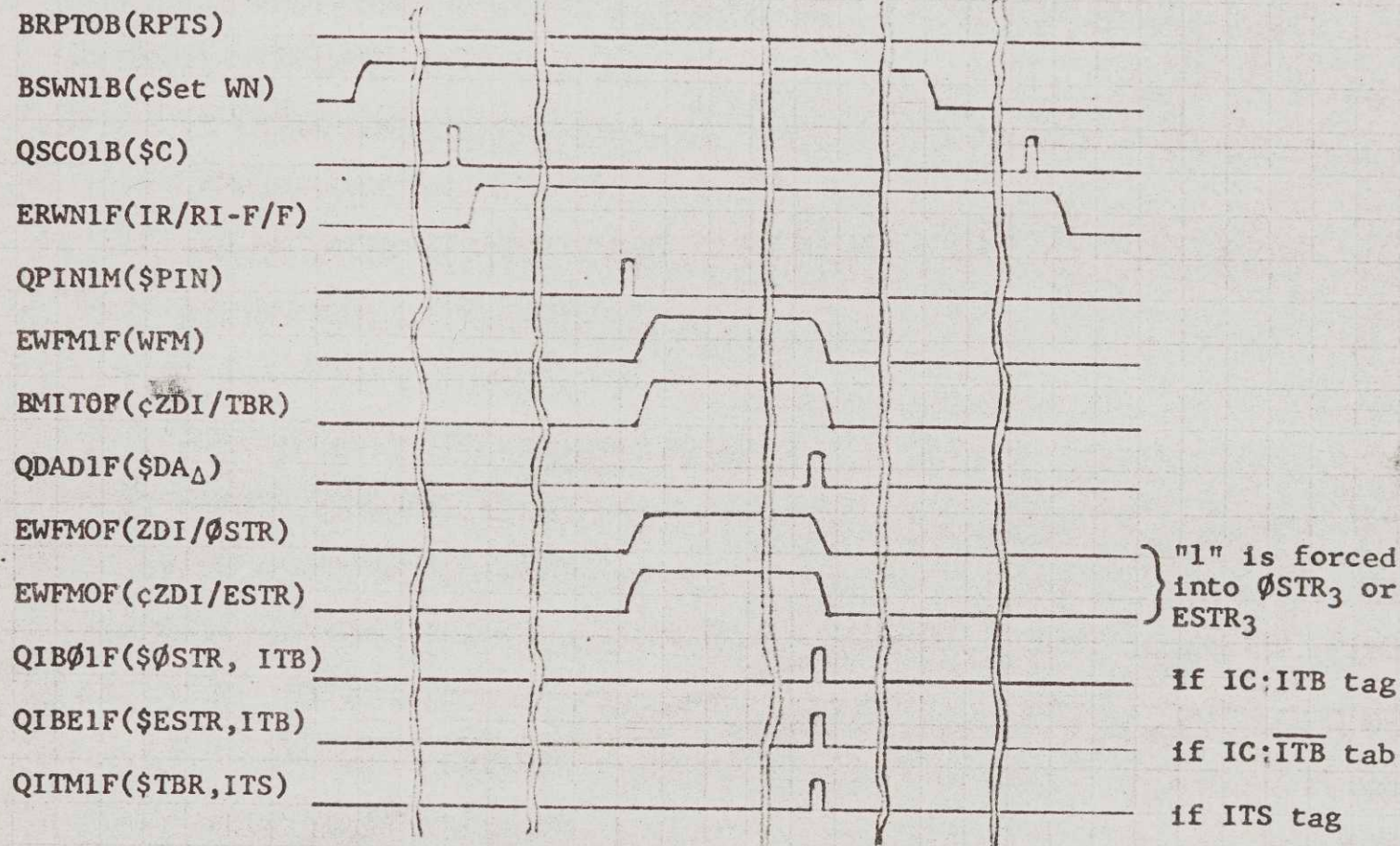


Fig. 10.3.3 Wait For Modifiers (WFM)
Operations, Timing Diagram

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Spec. No. M50EB00107

Cont. on Sh.10-116 Sh. No.10-115

TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR

10.3.3 - contd

When the Control Frame sends (BSWN1B)(DW131B)(MB170B) (BRPT0B) representing ϕ Set WN, ZI13, BS17, and RPTS respectively to the Base Frame, it indicates that it is going to ask for an even indirect word that is the result of an RI/IR modification tag in the instruction or indirect word. With the foregoing levels from the Control Frame the next ϕ C sets the ERWNF (RI/IR) flip-flop. ERWN1F supplies the enable to the EWFMF (WFM) flip-flop and WFM is set upon receipt of the next QPIN1M(ϕ PIN) from memory indicating that a Processor interrupt is acknowledged. Concurrent with the setting of WFM, control levels BMIT0F (ϕ ZDI0-2 OSTR0-2,1/OSTR3; ϕ ZDI0-2/ESTR0-2,1/ESTR3) are generated. When QSDA1M(ϕ SDA) is received from the Interface Frame indicating that data is on the ZDI lines for approximately 250 nanoseconds, QDAD1F(ϕ SDA Δ) is generated. ϕ SDA Δ is approximately 90 nanoseconds after ϕ SDA, and is used to set either the EITBF (ITB) or EITSF (ITS) flip-flops and reset the WFM flip-flop.

The ITB flip-flop is set when ZDI30-35 indicates an ITB tag in the even indirect word, WFM is set, IC or IC is up, and ϕ SDA Δ is received. WFM is present long enough after ϕ SDA so that the ITB flip-flop may be set. IC and IC determine whether QIB01F(ϕ OSTR ITB) or QIB1F (ϕ ESTR ITB) generates QITB1F setting the ITB flip-flop and resetting the ITS flip-flop; IC for ϕ OSTR ITB, IC for ϕ ESTR ITB. The ITS flip-flop is reset whenever ITB is set to eliminate the possibility of both ITS and ITB being set at the same time. This could occur if an ITS modifier was followed by an ITB before the ITS had a chance to reset. If an ITS modifier is detected on ZI30-35 at ϕ SDA Δ time the ITS flip-flop will be set and QITM1F(ϕ TBR ITS) generated.

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COMPUTER EQUIPMENT DEPARTMENT
PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh.10-117 Sh. No.10-116

TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR

10.3.3 - contd

For ITB modification OSTR is strobed if (IC)(ITB tag), ESTR is strobed for (IC) (ITB tag), and the applicable segment tag register has the new segment tag. A "1" is forced into OSTR₃ or ESTR₃ when the new ITB modifier is received to indicate in later appending operations that base has to be selected using the segment tag registers.

For ITS modification, \$TBR, ITS strobes the data on ZDI₀₋₁₇ into the TBR. The TBR is used as the address pointer to the external base for ITS modification as mentioned previously.

10.3.4 GENERAL BASE OPERATIONS

The GE-645 Instruction Set contains 19 op codes (68 instructions) that directly affect operations that are peculiar to the Base Frame. Whenever these instructions are decoded by the Control Frame and a start pulse is received from the Interface Frame, the Base Frame enters the general base operation mode of operation. When the specific instruction execution is complete, a finish pulse is sent to the Control Frame to indicate that the Base Frame is complete.

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Spec. No. M50EB00107

Cont. on Sh.10-118 Sh. No.10-117

TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR

10.3.4.1 Add to Base_n (ADB_n) (See timing diagram Fig. 10.3.4.1)

The receipt of QBOR1M (\$BORY) from the Interface Frame indicates that a general base operation (GBO) is to be started. \$BORY generates QABR1F (\$B) the general base strobe used throughout the Base Frame. Strobe \$B·BCBCOF(̄CSBC) sets the GBO state flip-flop sending EGB01F to all circuits concerned with Base Frame operations. Level EGB01F is present during all base frame operations and is reset with the final \$B₁₃ that generates QZBC1F(\$BC), the finish pulse for base frame operations.

When the GBO flip-flop is set, the decoded ADB_n instruction on the DW_B (ZI) lines from the Control Frame and GBO cause BADSOF(̄cZI_{2,7,8}/Sel Int), BADIOF(̄cZI_{2,7,8}/Sel ZBRI), BIIB0F(̄cZBRI/toCF) and BBSBOF(̄cBS0-17/ABR0-17) control levels to be generated. This switches the designated code for the effected ABR (as derived from the op code on ZI) to the one of eight decoders, opens the switch for the internal base bus to the Control Frame and switches the output of the BS-adder in the Control Frame to all eight ABR's (0-7). The decoded DSI₁F bits are used to generate BIN_{OF}(̄c\$INT₁) which controls the selection of the strobe for the selected ABR. DBI₁F bits are used to select the internal ABR₀₋₁₇ that is sent to the BS-adder in the Control Frame as previously explained. The ABR effected is not checked for internal or external base bit restrictions since the ADB_n instruction allows an internal or external base to be specified.

When QSDA1M(\$DA) is received from the Interface Frame QDAD1F(\$DA_Δ) is generated and subsequently generates QABR1F(\$B₁₃). Generation of QAB₁F(\$ABR₀₋₁₇) is dependent on (\$B₁₃)·(GBO)·(̄c\$INT₁)·BSL₁F (Master = 1 + Lock bit = 0). In other words the strobe for the applicable ABR is generated after the output of the BS-adder has had time to settle and the Processor is in Master mode or the lock base bit (ABR_{n22}) for the selected register is "0."

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COMPUTER EQUIPMENT DEPARTMENT
PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh.10-119 Sh. No.10-118

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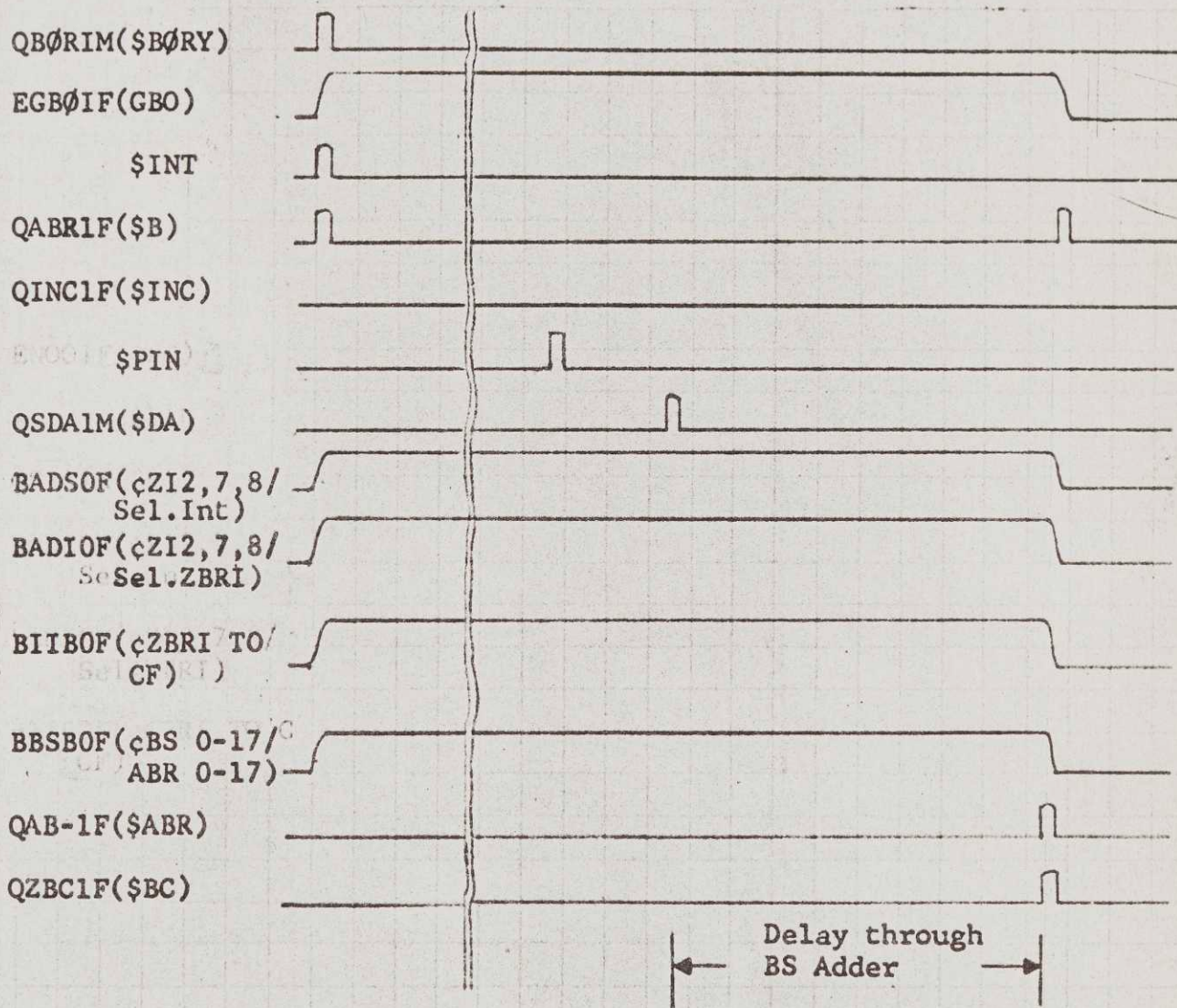


Fig. 10.3.4.1 Add to Base n (ADBn), Timing Diagram

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Spec. No. M50EB00107

Cont. on Sh.10-120 Sh. No.10-119

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

10.3.4.1 - contd

Concurrent with the generation of \$ABR₀₋₁₇, \$BC is generated indicating that Base Frame operations are complete. However, \$BC is only generated if no "Fault" occurred in the selection of one of the ABR's (ϕ \$INT₋)--there was no attempt to change the selected ABR when the ABR was locked against change and the Processor was not in Master mode. Level BFLT_{OF} (ϕ SetFLT) will always enable the \$BC circuits unless a Fault has occurred.

10.3.4.2 Clear Associative Memory (CAM) (See timing diagram Fig. 10.3.4.2)

The Clear Associative Memory Instruction is used only to reset the empty/full bit and initialize the usage count bits in each Associative Register. Strobe \$BORY from the Interface Frame generates \$B₁₃ which sets the GBO flip-flop and eventually sends BCAM_{1F} (Reset Associative Memory) to the Associative Memory. A second \$B₁₃ is generated as a result of the recirculation loop in the \$B chain being enabled by the BYCF_{1B}(Y) term input to the second section of the \$B chain that generates QIBD_{1F}.

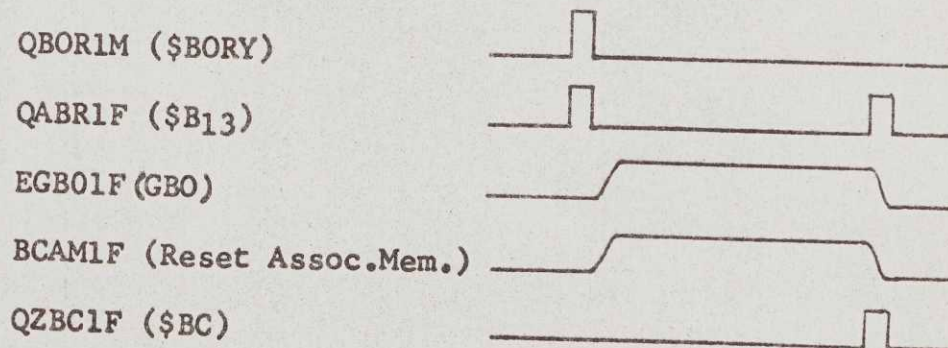


Fig. 10.3.4.2 Clear Associative Memory (CAM),
Timing Diagram

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PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh.10-121 Sh. No.10-120

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

10.3.4.3 Store Associative Memory (SAM) (See timing diagram
Fig. 10.3.4.3)

The SAM instruction operation within the Base Frame is primarily concerned with keeping track of the number of registers stored by the IF frame and generating \$BC to indicate that operations are complete.

Strobe \$BORY received from the Interface Frame generates \$B₁₃, sets the GBO flip-flop generating BSAM1F (SAM-GBO to the Associative Memory) and then generates QSBDF (\$B_Δ). Strobe \$B_Δ is used in conjunction with EN000F-EN050F(INCO) · BBRY1F (enable for all stores) to generate QBRY1F(\$BRY) indicating that the Base Frame is ready. The term INCO is tied to the 20 position of the increment counter (EN01_F - EN05_F) indicating that the circuitry is prepared to count beginning with the even word location. When the Interface Frame issues \$INT, QDST1M(\$DS) is received, generating another \$B₁₃ and QDPB1F(\$DP). Strobe \$DP is a function of INCO (the 20 position of the increment counter which has been incremented one count by \$B₁₃) and indicates to the Interface Frame that this strobe is for the second half of a double-precision store for the odd word. The Interface Frame turns the \$DP around and sends another \$DS to the Base Frame thereby incrementing the increment counter to two and generating another \$BRY. As before, \$BRY indicates that the Base Frame is ready for the next store. However, the Interface Frame will have to wait until it has gained control of the memory and stored both words of data, as signified by a \$DA received from the memory, before issuing another \$INT and subsequent \$DS to the Base Frame.

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 PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh. 10-122Sh. No.10-121

TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR

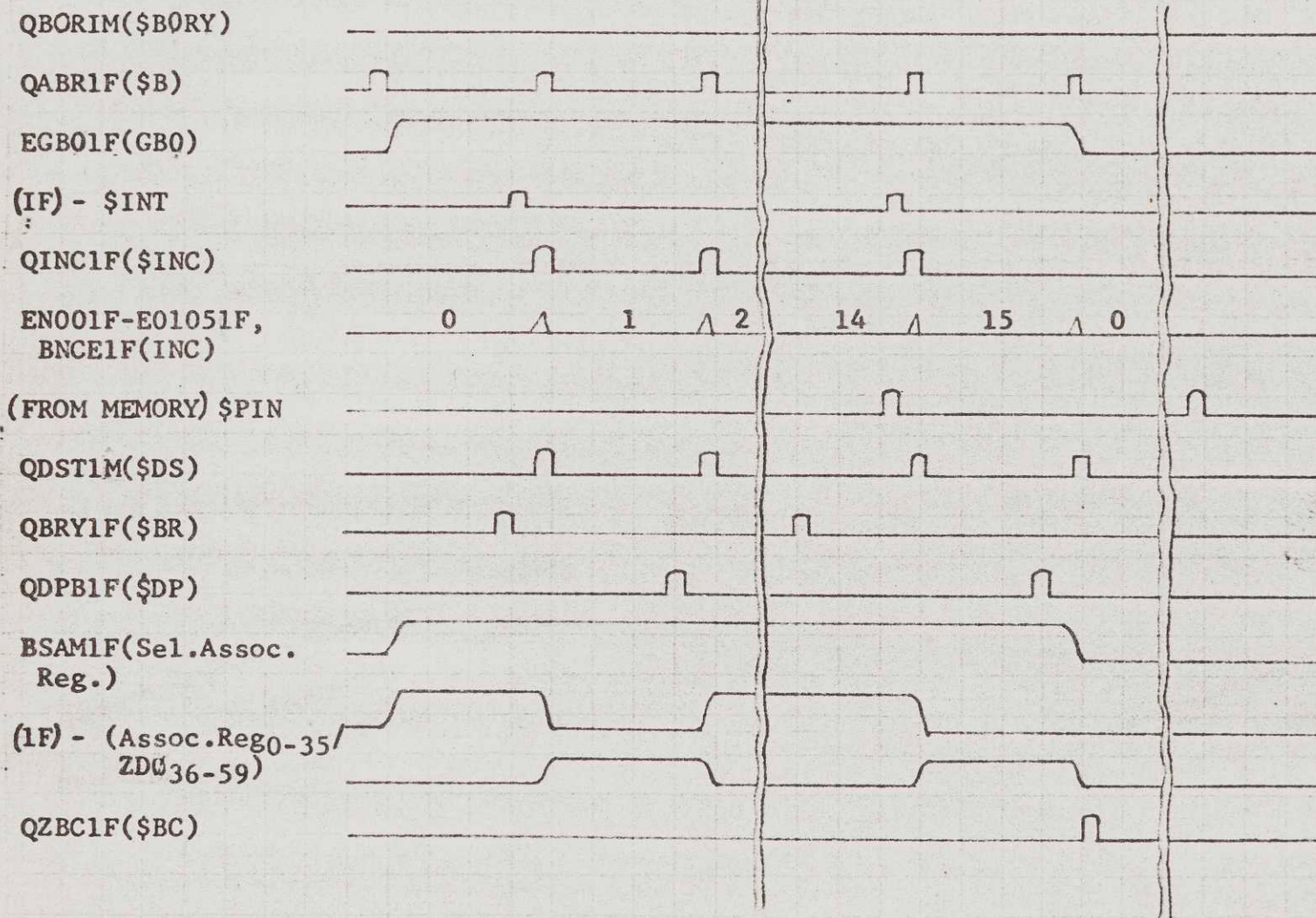


Fig. 10.3.4.3 Store Associative Memory Instruction (SAM), Timing Diagram

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Cont. on Sh.10-123 Sh. No. 10-122

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

The above procedure is repeated for sixteen double-precision stores and 31 counts of the increment counter. With a count of 31 in the increment counter BCB1F(ç\$BC). BFLT0F(çSet FLT) are enabled so that the next \$B₁₃ that is generated as result of the last \$DS from the Interface Frame, causes \$BC and resets the GBO flip-flop indicating that base operations are complete. The last \$BRY is not generated since the removal of GBO from the \$B circuits prevents generating the last \$B_Δ in addition to resetting the increment counter.

The operation performed by the Base Frame for the SAZ instruction is identical to the SAM instruction except for the following: BSAZ1F (SAZ·GBO) is sent to the Associative Memory instead of BSAM1F and only one double-word store is made before \$BC is generated; strobe \$BC now being a function of an increment count of 1·SAZ rather than 31·SAM.

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PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh. 10-124 Sh. No. 10-123

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

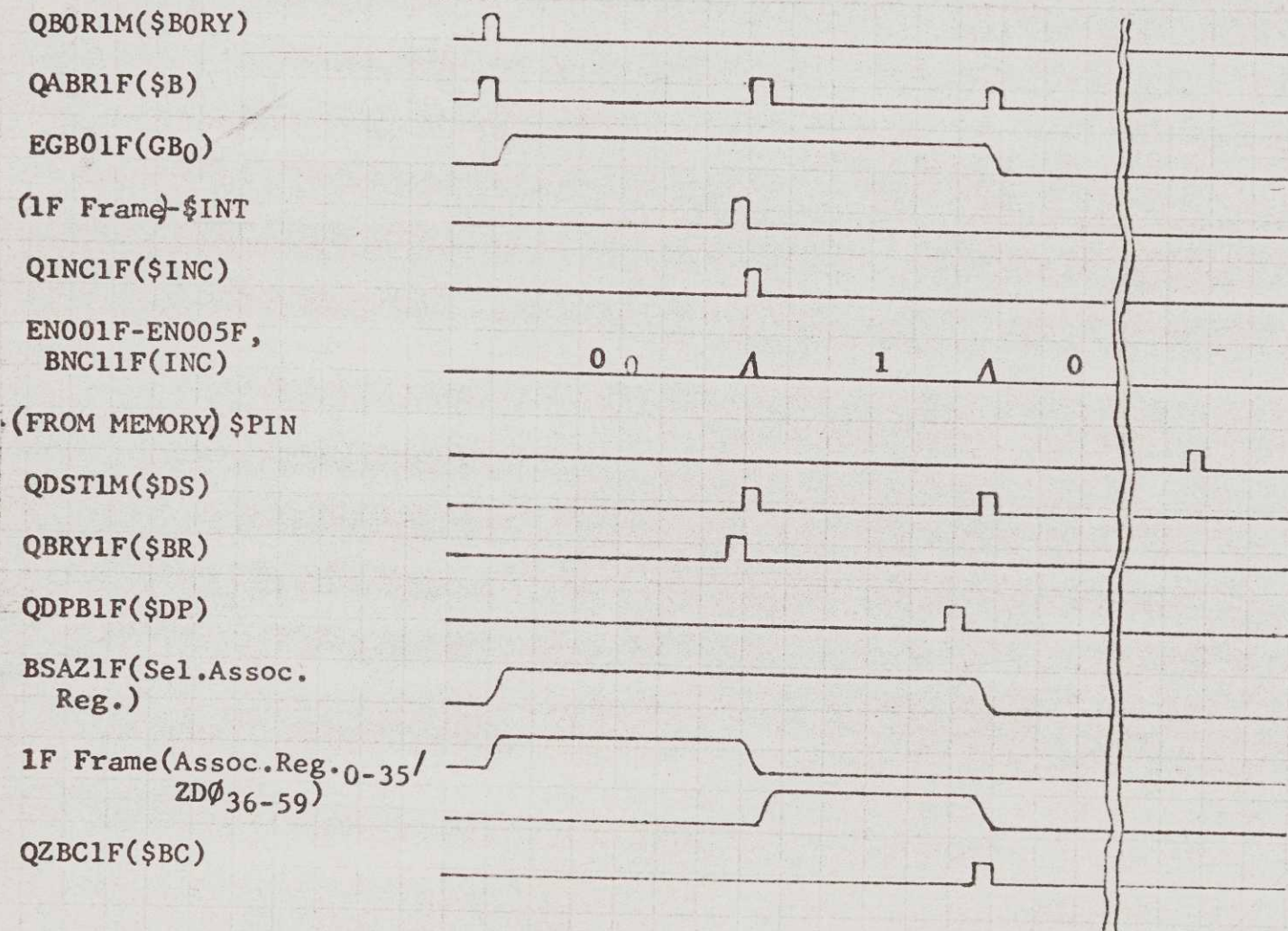


Fig. 10.3.4.4 Store Associative Memory Zero (SAZ), Timing Diagram

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Cont. on Sh.10-125 Sh. No. 10-124

10.3.4.5 Effective Address to Basen(EABn) (See timing diagram, Fig. 10.3.4.5)

The EABn instruction involves strobing the new effective address in the BS-adder into the selected internal ABR. If an internal base must be added the segment tag register contains the designation of the base that is sent, (if internal) to the BS-adder.

Receiving \$BORY generates \$B₁₃, sets the GBO flip-flop, inhibits BAPIIF (append for ESTR and OSTR/Sel. Int) continues to allow BAPZIF (append to ESTR and OSTR/Sel ZBRI) and enables control points BEBPOI (ZI,4,7,8/Sel Int) and BBSBOF (¢BS₀₋₁₇/ABR₀₋₁₇). In addition, if the Control Frame is in the PA cycle of the EABn instruction with bit 29 of the instruction word = "1," or an ITB modifier was received, BIIBOF (¢ZBRI/toCF) is enabled indicating that an internal base must be added before strobing the selected internal ABR with the new effective address. Decoding of ZI_{4,7,8}/Sel Int. determines the BIN_OF (¢\$INT_) level that controls \$ABR₀₋₁₇ for the selected register. The output of the applicable segment tag register (OSTR or ESTR) for the EABn instruction as determined by IC or IC selects the internal base to be sent to the BS-adder via the ZBRI/to CF switch. The data from the BS-adder is settled when \$ABR₀₋₁₇ is generated by the second \$B₁₃ from the \$B chain; QIBDIF recirculating to generate the second \$B₁₃. Strobe \$ABR₀₋₁₇ is only generated if the Master = "1" or lock bit (ABRn₂₂) = "0" conventions are met and occurs approximately 180 nanoseconds after the first \$B₁₃ generated by \$BORY. As a result of the second \$B₁₃, \$BC is generated, the GBO flip-flop is reset and the enables to all the applicable control points are removed.

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PHOENIX, ARIZONA

Spec. No. M50EB00107
Cont. on Sh. 10-126Sh. No.10-125

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

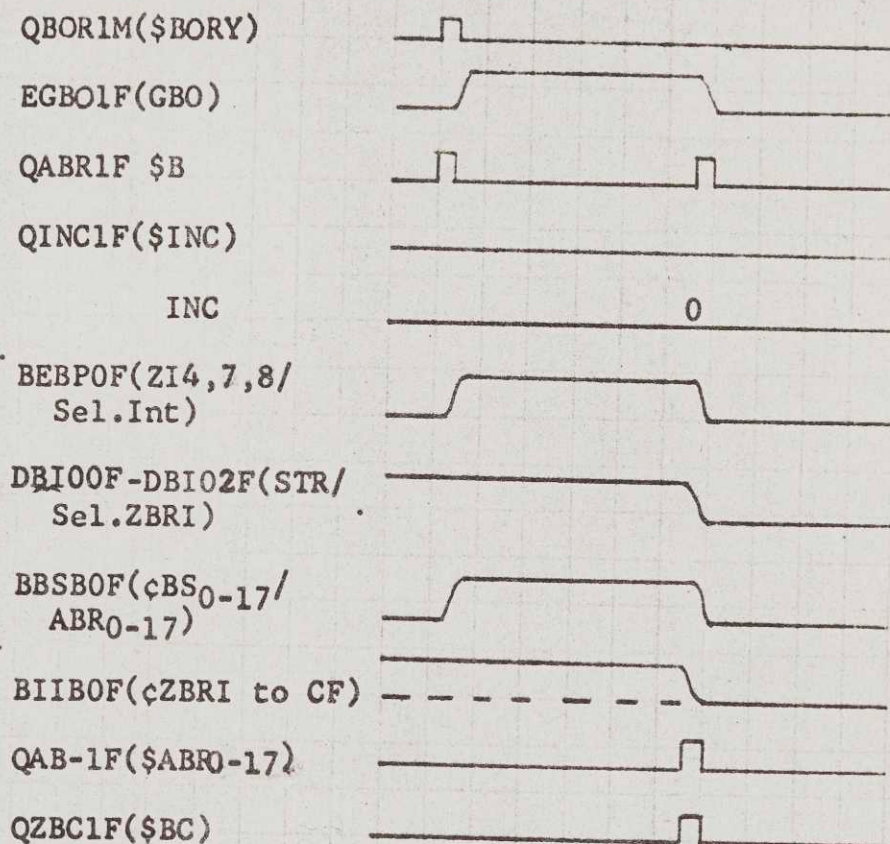


Fig. 10.3.4.5 Effective Address to Base n.
(EABn), Timing Diagram

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Spec. No. M50EB00107

Cont. on Sh.10-127 Sh. No.10-126

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

10.3.4.6 Effective Address to Pair_n (EAP_n) (See timing diagram
Fig. 10.3.4.6)

The EAP_n instruction involves strobing the effective address into the designated internal ABR and strobing the pointer from the TBR into the linked external ABR designated by bits 18-20 of the internal ABR. If the ABR designated by the EAP_n instruction contains an external base, then the pointer from the TBR is strobed into the same base as designated by the EAP_n instruction.

Strobe \$BORY initiates base frame operations by setting the GBO flip-flop, turning on control points BEBPOF(ζ ZI_{4,7,8}/Sel Int), BBSBOF(ζ BS₀₋₁₇/ABR₀₋₁₇), enabling the \$B₁₃ input to the increment counter and (if in the PA cycle of the EAP_n instruction with bit 29 of the instruction word = "1" or an ITB modifier received) BIIBOF(ζ ZBRI/to CF). Bits 4,7,8 of ZI are decoded to pick the designated register to be strobed. When an EAP_n instruction is detected, the ζ \$INT_{level}(BIN00F) which controls the strobe selection is forced on whether the designated base is internal or external. The segment tag for the EAP_n instruction is decoded from OSTR or ESTR as determined by IC or IC to select the internal base that is sent to the BS-adder in the Control Frame.

By the time that QAB_{1F}(\$ABR₀₋₁₇) is generated as a result of the second \$B₁₃ from the recirculating \$B chain, the BS-adder input to the ABR designated by the EAP_n instruction is stable. Strobe \$ABR₀₋₁₇ for the selected register is a function of the Master/Slave mode, lock base bit (BSL01F) restrictions, and an increment count of "0." The \$B₁₃ that generates \$ABR₀₋₁₇ also advances the increment counter to "1," terminates level ζ BS₀₋₁₇/ABR₀₋₁₇, and enables BTBBOF (ζ TBR₀₋₁₇/ABR₀₋₁₇) in preparation for putting the pointer in the TBR into the linked external base designated by bits 18-20 of the selected internal base.

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Spec. No. M50EB00107

Cont. on Sh.10-128 Sh. No.10-127

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

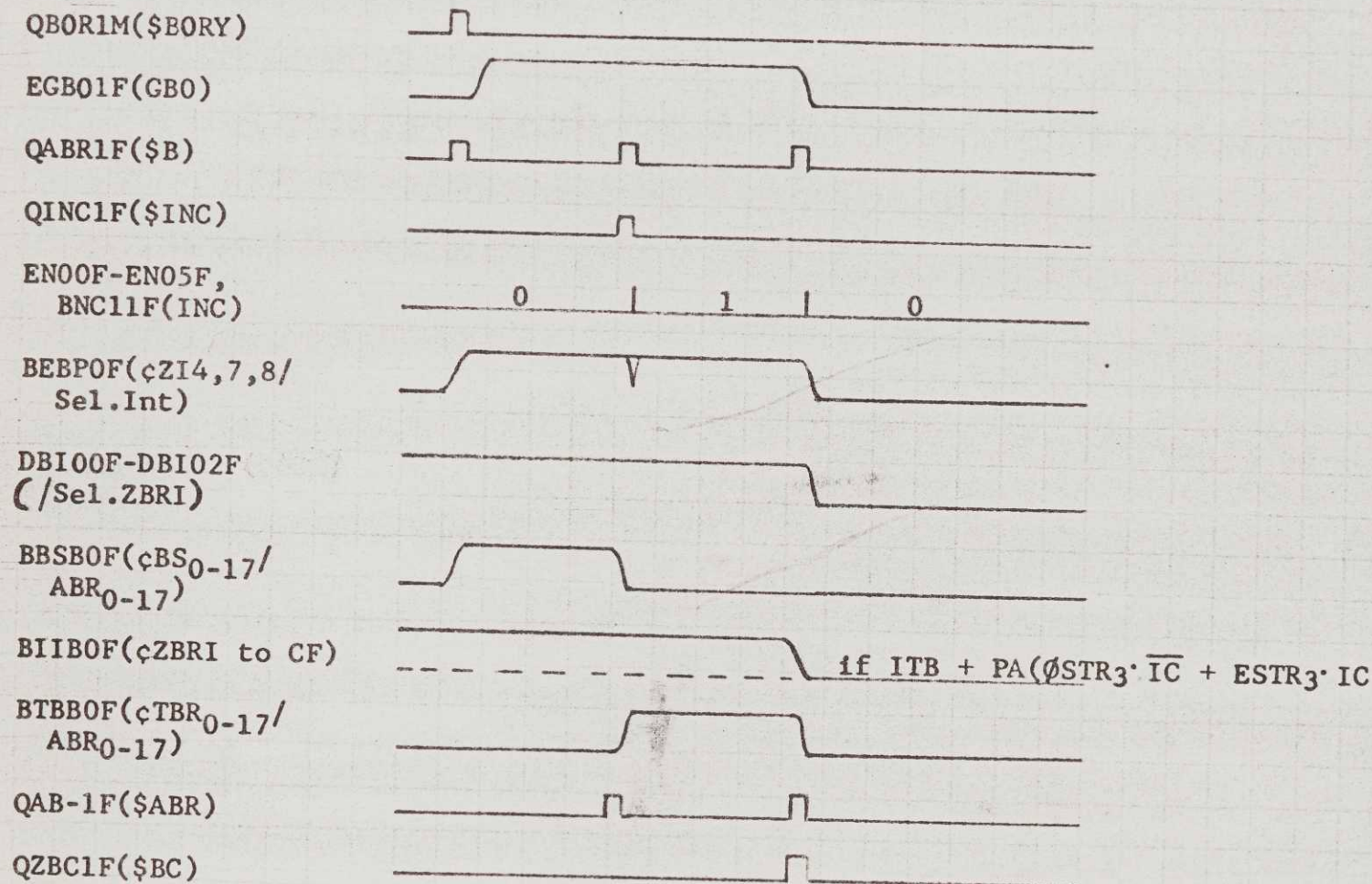


Fig. 10.3.4.6 Effective Address to Pair n
(EAPn), Timing Diagram

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Spec. No. M50EB00107

Cont. on Sh.10-129 Sh. No.10-128

TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR

10.3.4.6 - contd

Selection of the ABR to be strobed with the pointer from the TBR depends on whether the original ABR was internal or external. If the original ABR was internal the external base is decoded from bits 18-20 of the designated internal base that was dumped on the ZXBN bus, and the 5-wide NAND gate associated with the linked external ABR generates BRX-OF ($\text{c}\$EX_$). Level ($\text{c}\$EX_$) in addition to the decoded EAPn instruction, an Increment Count of "1," and BSL01F generates BAB_OF, which controls the strobe for the external register designated by bits 18-20 on the ZXBN bus. If the original ABR selected by the EAPn instruction was external, then the 3-wide gate associated with $\text{c}\$EX_$ generation and the original ABR designated by the one of eight decoder, is enabled.

The receipt of the third $\$B_{13}$ from the $\$B$ loop generates $\$ABR_{0-17}$ for the proper ABR: the linked external ABR if the original ABR was internal; the EAPn designated ABR if the original ABR was external. Concurrent with the third $\$B_{13}$, the GBO flip-flop is reset, $\$BC$ is generated (assuming the Master/Slave lock base conventions were met and no fault was generated), all control point enables are removed, and the increment counter is reset to zero.

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Spec. No. M50EB00107

Cont. on Sh.10-130 Sh. No.10-129

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

10.3.4.7 Load Base Register n (LBRN) (See timing diagram
Fig. 10.3.4.7)

When performing an LBRn base operation the Base Frame in a sense interrupts a normal append operations sequence as soon as the Interface Frame has strobed the appended address for the "operand" into its Address Register and issued a \$INT for a final address to memory. Strobe \$BORY is received generating \$B₁₃ when a \$INT is initiated by the Interface Frame and sets the GBO flip-flop. Setting the GBO flip-flop inhibits all control points concerned with Address Appending for operands, and enables BLSROF ($\bar{c}ZI_{6,7,8}/Sel\ Int$) and BMIBOF (ZDI_{0-23}/ABR_{0-23}). Decoding of $ZI_{6,7,8}$ picks the affected register through the generation of $\bar{c} \$INT$. Level $\bar{c} \$INT$ is forced on whether the selected ABR is internal or external and controls the selection of QAB-1F ($\$ABR_{0-17}$). Strobe QAC-1F($\ABR_{22}) is a function of $LBR \cdot GBO \cdot \bar{c} \$INT \cdot BMST1B$ (Master mode) and the next \$B₁₃. Similarly, strobe QAD-F($\$ABR_{18-21,23}$) is a function of $LBR \cdot GBO \cdot \bar{c} \$INT \cdot BSL-IF$ (Master = 1+ Lock = 0) and the next \$B₁₃.

Receipt of QSDA1M(\$DA) from the Memory generates \$DAΔ and subsequently \$B₁₃, \$ABR₀₋₁₇, \$ABR₂₂, and \$ABR_{18-21,22}. Strobe \$DAΔ is not delayed as long as for the ADBn or LDCF instructions since the extra delay in those cases was for the BS-adder in the Control Frame to stabilize. Strobe \$BC is generated in the usual manner as previously explained, provided no lock base fault ($\bar{c}$ Set FLT) occurred. After \$BC signals Base Frame complete, the append operations cycle is closed out in the normal manner upon the arrival of the next \$C.

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PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh.10-131 Sh. No.10-130

TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR

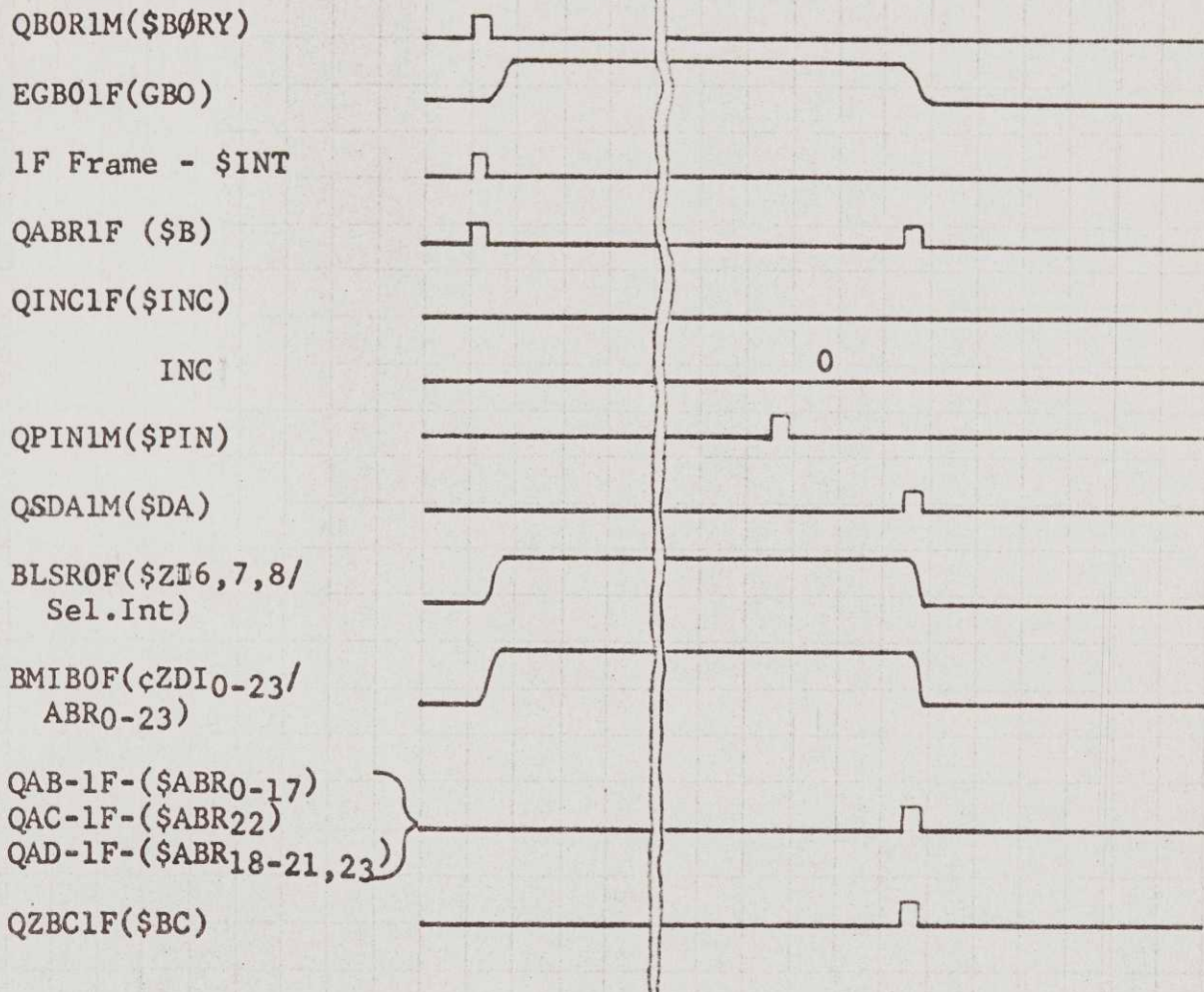


Fig. 10.3.4.7 Load Base Register n (LBRn),
Timing Diagram

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Spec. No. M50EB00107

Cont. on Sh.10-132 Sh. No.10-131

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

10.3.4.8 Load Base Registers (LDB) (See timing diagram
Fig. 10.3.4.8)

The sequence of operations for the LDB instruction is almost identical to that of the LBRn instruction, with the following exceptions: increment counter bits 3-5($2^2 - 2^0$) are routed to the one of eight decoders to successively select the eight ABR's; no fault signal is sent to the Control Frame if an attempt is made to load the ABR's in Slave mode with ABR22 = "1," but the affected ABR will not be changed. Strobe \$BC is generated when the increment count reaches 7 and the next \$B13 arrives (eight operations complete).

10.3.4.9 Load Descriptor Segment Base Register (LDBR)
(See timing diagram Fig. 10.3.4.9)

When an LDBR instruction is recognized by the Control Frame, and the Processor is in Master mode, QBOR1M(\$BORY) is received from the Interface Frame generating \$B11 and setting the GBO flip-flop. Data to load the DSBR comes over the ZDI lines from memory, and are strobed into the DSBR when \$DA from Memory generates \$B11. Strobe \$BC is generated at \$B13 time in the usual manner. No fault signal generation is a function of the LDBR instruction in the Base Frame load register fault detection circuitry, since the Processor fault logic makes a determination prior to the execution of the LDBR instruction. In conjunction with execution of the LDBR instruction a CAM*GBO (reset to Associative Memory) is generated.

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GENERAL ELECTRIC COMPANY
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PHOENIX, ARIZONA

Spec. No. M50EE00107

Cont. on Sh. 10-133Sh. No. 10-132

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GE-645 PROTOTYPE PROCESSOR

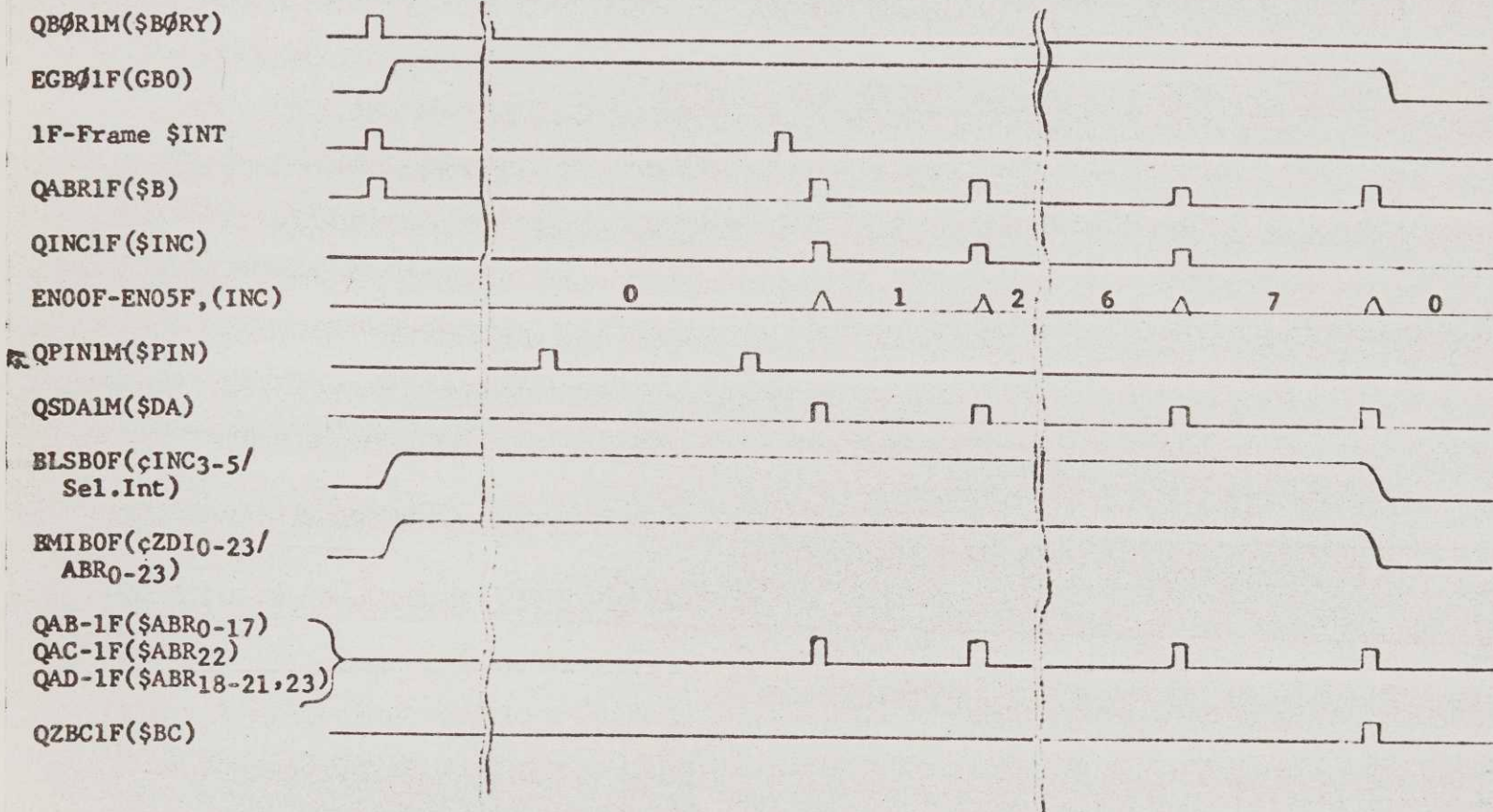


Fig. 10.3.4.8 Load Base Registers (LDB),
Timing Diagram

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Spec. No. M50EB00107

Cont. on Sh. 10-134 Sh. No. 10-133

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GE-645 PROTOTYPE PROCESSOR

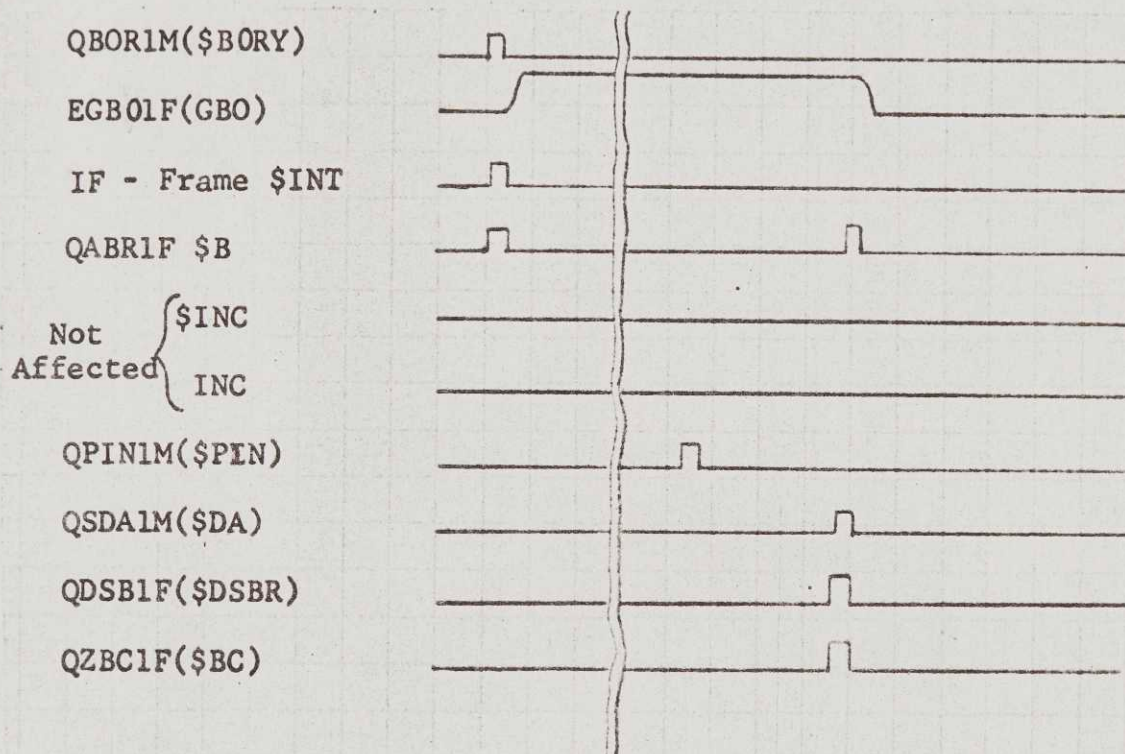


Fig. 10.3.4.9 Load Descriptor Segment Base Register (LDBR), Timing Diagram

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PHOENIX, ARIZONA

Cont. on Sh.10-135 Sh. No.10-134

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

10.3.4.10 Load Control Field (LDCF) (See timing diagram Fig. 10.3.4.10)

For this instruction the effective address in the BS-adder in the Control Frame is interpreted as three 6-bit characters: character 1 contains the ABR designation, (BS₀₋₂ for ABR_n, BS₃₋₅ for ABR_m), character 2 the new information for ABR_n, character 3 the new information for ABR_m. Strobe \$BORY generates \$B₁₃ setting the GBO flip-flop resulting in control points BLD00F(¢BS₀₋₂/Set Int, BS₆₋₁₁/ABR_n₁₈₋₂₃) being turned on. When \$DA is received from the Memory signifying that data is on the lines to the Control Frame, \$DA_Δ is generated (delayed approximately 250 nanoseconds after \$DA to allow time for the BS-adder to settle) and generates \$B₁₃. Bits 0-2 of the BS-adder are then decoded to select the proper ABR to be loaded with new control field information, and enable ¢\$INT₋ to the ABR strobe circuits. Strobe \$B₁₃ causes the generation of strobes for ABR₀₋₁₇, ABR₂₂, ABR_{18-21,23} if the Processor is in Master mode or the selected base is not locked against change when the Processor is in Slave mode. Though strobes for the entire 24 bits are present, only the control field data(bits 18-23)are present.

The \$B₁₃ that generated \$ABR₀₋₂₃ (three strobes) advances the increment counter to "1" thereby removing BLD00F and enabling BLDIOF (¢BS₃₋₅/Set Int, ¢BS₁₂₋₁₇/ABRm₁₈₋₂₃). When the increment count reaches "1" the internal \$B₁₃ loop is enabled by (LDCF)(INC=1) to generate another \$B₁₃; generating \$ABR₁₈₋₂₃ as before, but for the new ABRm specified by BS₃₋₅ and for the new data from BS₁₂₋₁₇. This same \$B₁₃ generates \$BC and resets the GBO flip-flop. With this particular instruction if an attempt is made to load control fields with the ABR's designated locked against change then strobe QFLT1F(\$FLT) will be generated, one strobe for each ABR attempted, though only the first one is sufficient for the Processor fault logic.

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PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh.10-136 Sh. No. 10-135

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

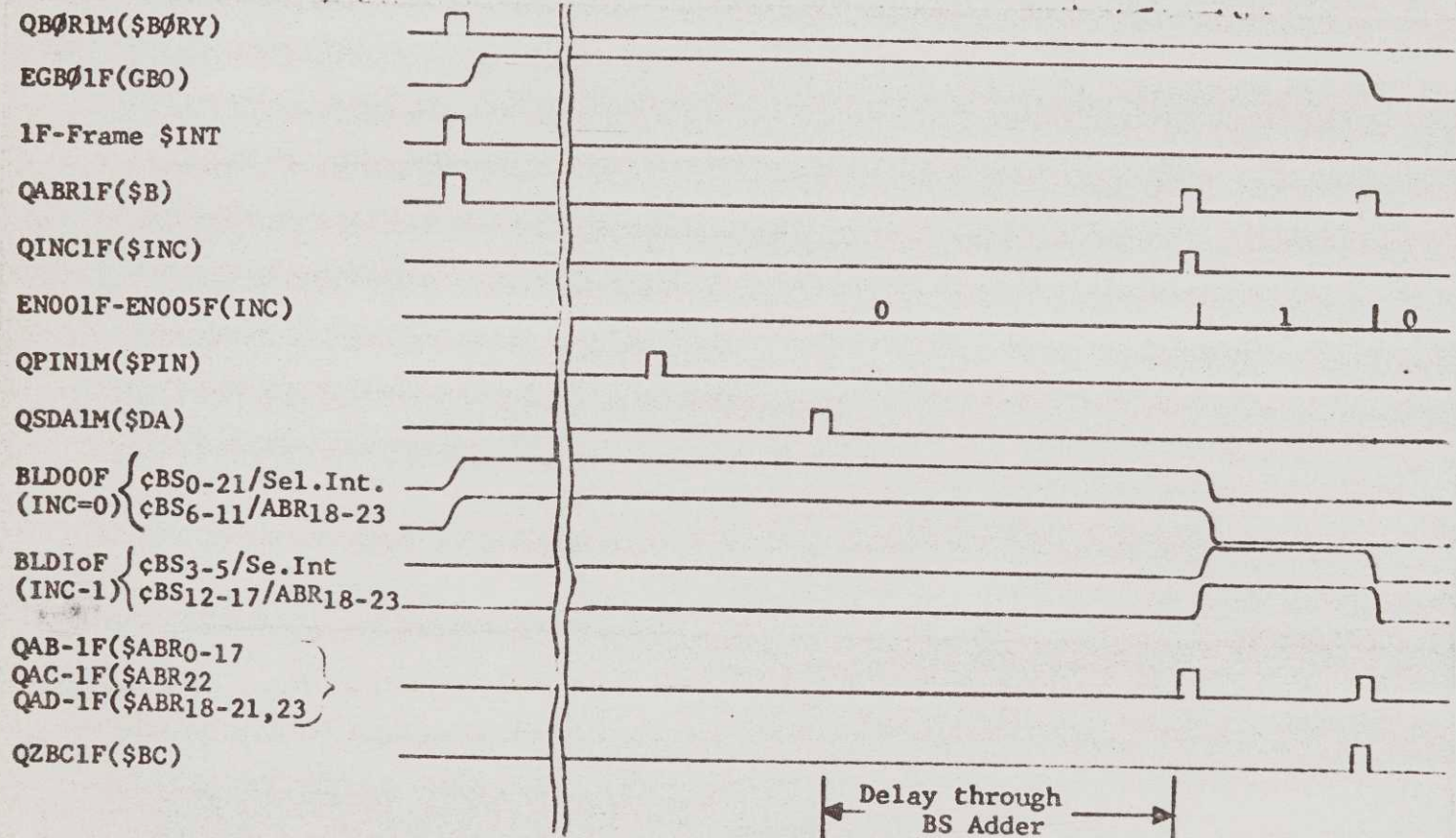


Fig. 10.3.4.10 Load Control Field (LDCF),
Timing Diagram

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Spec. No. M50EB00107

Cont. on Sh. 10-137 Sh. No. 10-136

TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR

10.4 PROCESSOR POWER ON/OFF SEQUENCING (See 43D163422 sheet 22)
 (To be supplied at a later date.)

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Spec. No. M50EB00107

Cont. on Sh.10-138 Sh. No.10-137

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

10.5 PROCESSOR FAULT LOGIC

10.5.1 GENERAL DESCRIPTION

The fault logic circuitry for the Processor detects the conditions which will result in one of 32 defined Processor faults and causes a trap to the memory cell (two consecutive memory locations; even - odd) in the Processor Fault Vectors corresponding to the particular fault. In performing this function the fault logic circuitry does the following:

- 1) Anticipates that a fault condition may occur and sets a number of preliminary flags or flip-flops to help define the fault should it occur.
- 2) Detects the conditions which will result in a fault.
- 3) Depending on the type of fault detected and fault priority, waits until the optimum time before starting any actions.
- 4) When conditions are suitable, initiates a "snapshot" sequence to save the status of the Processor and the conditions that caused the fault. The term "snapshot" in this case indicates exactly what takes place; a picture of the Processor with the conditions which caused the fault safestored in the Processor internal registers.

As a result of the "snapshot" sequence, Processor flags and registers are saved awaiting an SCU instruction as the first instruction of the fault vector pair for the particular fault detected. The "snapshot" saves the following in the registers indicated:

- a) Temporary Base register saved in the Data out register, bits 0-17.

b) Appending Unit status flags saved in the Data out register bits 18-31 as follows (the bits indicate control of a register or that a flag is set):

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PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh. 10-139 Sh. No. 10-138

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

10.5.1 - contd

- b) Appending Unit status flags saved in the Data out register bits 18-35 as follows (the bits indicate contents of a register or that a flag is set):

<u>Bit Position</u>	<u>Name</u>
18-21	OSTR ₀₋₃ register
22-25	ESTR ₀₋₃ register
26	ITS tag
27	ITB tag
28	not used ("0")
29	PEO flag
30	ITR-indirect tally not equal to Tally Runout Indicator
31	not used ("0")
32	not used ("0")
33	DSPTW fetch
34	SDW fetch
35	PTW fetch

- c) Computed address existing during the last address preparation cycle saved in the Data out register, bits 36-53 (this is the effective address).
- d) Control Frame status flags saved in the Data out register, bits 54 - 71 as follows (the bits indicate contents of a register or that a flag is set):

<u>Bit Position</u>	<u>Name</u>
54	PI flag
55	PNO flag
56	not used ("0")
57	XDE flag

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PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh.10-140 Sh. No.10-139

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

10.5.1 - contd

<u>Bit Position</u>	<u>Name</u>
58	XDO flag
59	IC flag ("0" is even instruction. "1" is odd instruction).
60	MASF flag
61	EA level ("1" indicated operand fetch; "0" indicates indirect fetch)
62	MSY flag ("1" indicates Master mode; "0" indicates Slave mode)
63	PA flag
64	PZ flag
65	PT flag
66 - 71	CT register

- e) The ICT address of the faulting instruction is saved in the ICTA register.
- f) The contents of the Y- and C-registers are saved in the I-register and reflect any address modification for operand address preparation that had taken place prior to the "snapshot" sequence.
- 5) Initialize the Control, Base and Interface Frames with a WF level and the Operations Unit with a strobe \$ABORT. Both signals being generated as a result of the "snapshot" sequence.
- 6) Initiate the actions to enable the Control Unit to "brute-force" and XED instruction into both the Y- and C-registers with an address corresponding to the fault detected and processed by the fault logic.
- 7) Wait until the first of the XEDed instructions if an SCU, or until the XED instruction are executed without a fault, then reset the fault logic for detecting a trouble fault.

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PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh.10-141 Sh. No.10-140

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

10.5.1.1 Fault Descriptions

The 32 Processor faults fall into distinct groups for recognition and priority of service. These groups are designated Group I through Group VI, with the faults in Group I having the highest priority and Group VI the lowest priority. Within each group, the faults are mutually exclusive (no two can exist at one time) with the exception of Parity (which takes priority over Group III faults) and Group VI faults. For faults in Group VI, Shutdown has the highest priority followed by Timer Runout, and then Connect. External interrupts even though they are considered as Group VI faults, have the lowest priority of service. Interrupts will not be honored if any fault in Groups I through Group VI is detected before the Processor enters a WC cycle for an execute interrupt command response from the Memory Controller.

A summary of the various processor recognized faults is listed in Table 10.5.1.1.

10.5.1.2 Fault Detection and Recognition

Each of the 32 recognized Processor faults results in the same processor response, but causes a different fault vector address depending on the fault being serviced. However, the detection of the fault, and the subsequent recognition of the fault for service, are distinctly different for each fault condition. Table 10.5.1.2 lists the different groups of faults and the conditions under which the faults in each group are detected and recognized.

Table 10.5.1.1 Summary of Recognized Processor Faults

Fault Group	Fault Code	Fault Name	Fault Category	Fault Description
I	74	Startup	Manual	Processor initialized after POWER ON pushbutton depressed resulting in a DIS state. Then fetch two instructions from Startup fault vector.
	66	Execute	Manual	EXECUTE pushbutton depressed results in fetching two instructions from the Execute fault vector, or loading the Maintenance Panel INSTRUCTION switch setting into both instruction registers.
II	76	Trouble	Hardware	A Trouble fault occurs if a fault is encountered during a "brute forced" XED instruction for a fault or external interrupt or during the execution of the SCU instruction as the first instruction of the fault vector designated by the XED address.
	72	Operation Not Complete	Hardware	Any one of the following: (1) Addressed Memory Controller not connected to Processor, (2) Memory Controller does not respond to Processor, (3) Processor has not generated memory access or had a direct operand for a 1-2 milliseconds and is not in a DIS state, (4) RAR cycle is closed out by Memory Controller without receiving data from Processor, (5) Memory does not acknowledge data from Processor for DP store or RAR cycle, (6) Programming rules violated leading to undefined operation.

COMPANY CONFIDENTIAL

GENERAL ELECTRIC COMPANY
COMPUTER EQUIPMENT DEPARTMENT
PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh.10-142 Sh. No.10-141

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

COMPANY CONFIDENTIAL

GENERAL ELECTRIC COMPANY
COMPUTER EQUIPMENT DEPARTMENT
PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh.10-143 Sh. No. 10-142

TITLE:ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

Table 10.5.1.1 Summary of Recognized Processor Faults (contd)

Fault Group	Fault Code	Fault Name	Fault Category	Fault Description
III	64	Divide Check	Program	Division cannot be complete as defined by the instruction.
	62	Overflow	Instruction Program	Any arithmetic overflow that is not masked by the Overflow Mask indicator.
IV	30	Parity	Hardware	Any one of the following parity errors that are not masked by the Parity Mask indicator (except parity on SDWs or PTWs which are independent of the Parity Mask): (1) Single-precision reads; (2) Double-precision reads, either word; (3) Read-alter-rewrite cycles with parity on read, the rewrite cycle is completed with correct parity (4) Instruction or indirect word (5) Operand for Operations Unit is executed with bad parity then the Parity fault is recognized.
	32	Illegal Memory Command	Instruction Program or Hardware	Processor has issued a connect command to a masked Memory Controller channel.
	70	Lockup	Instruction Program or Hardware	No recognition of external interrupts for 1-2 milliseconds and the Processor is not in a DIS state. Lockup is disabled on "repeat" instructions.

Table 10.5.1.1 Summary of Recognized Processor Faults (contd)

Fault Group	Fault Code	Fault Name	Fault Category	Fault Description
V	26	Illegal Descriptor	Operating System	Bits 30-35 of the last SDW or PTW are undefined.
	24	Illegal Procedure	Instruction or Program	Generally programming violations: (1) GE-645 privileged instructions in slave - LDBR, SDBR, SAM, ZAM, CAM, SCU, RCU, LACL (2) GE-645 semi-privileged instructions in slave and base is locked - EAPn, EABn, TSBn, LDCF, ADBn, LBRn (3) Undefined operation codes including the all zero code (4) Out of bounds address or pointer (5) Access restrictions on the segment or page Processor is attempting to access.
	22	GE-635 Compatibility	Instruction or Program	Traps instructions in the GE-635 repertoire not included in the GE-645 - LBAR, SBAR
	60	GE-635/645 Compatability	Instruction or Program	Attempted to execute GE-635/645 privileged instructions in Slave instead of Master mode - SMIC, RMCM, SMCM, CIOC, LDT, DIS, TSS
	2,10, 12,16	MME1-4	Instruction or Program	Programmed fault defined by instruction operation code and address.
	4	Derail	Instruction or Program	Programmed fault defined by instruction operation code.
	20, 34, 36	Fault Tag 1-3	Instruction or Program	Programmed fault in instruction or indirect word tag for an IT modification, causes an immediate fault, F1 is for GE-635 programs; F2, F3 are for GE-645 programs.

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GENERAL ELECTRIC COMPANY
COMPUTER EQUIPMENT DEPARTMENT
PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh.10-144 Sh. No.10-143

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

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 COMPUTER EQUIPMENT DEPARTMENT
 PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh.10-145 Sh. No.10-144

TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR

Table 10.5.1.1 Summary of Recognized Processor Faults (contd)

Fault Group	Fault Code	Fault Name	Fault Category	Fault Description
V	40,42, 44,46, 50,52, 54,56	Directed Faults 0-7	Operating System	Defined by bits 30-31 of an SDW or PTW as to the type of Directed Fault, for example, missing page from a data segment.
VI	0	Shutdown	Manual	Power will be turned off to the Processor approximately 1 milli-second after the POWER OFF pushbutton is depressed.
	6	Timer Runout	Hardware	This fault is generated when the contents of the Timer Register reaches zero and the Processor is in Slave mode. If the Processor is in Master mode the Timer Runout fault is not recognized until a return to the Slave mode.
	14	Connect	Instruction or Program	A Connect pulse from another active device is received via the Memory Controller
		External Interrupts	Hardware	A device has set an interrupt cell in the Memory Controller resulting in an interrupt present request received at a Processor port.

The fault vector address is received from the Memory Controller in response to an execute command sent from the Processor in response to an external interrupt

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COMPUTER EQUIPMENT DEPARTMENT
PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh.10-146 Sh. No. 10-145

TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR

10.5.1.2 - contd

Detection means exactly that; a fault condition has been detected. Recognition occurs when the fault logic initiates a "snapshot" sequence leading to the "brute forced" XED instruction with the proper fault address.

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Spec. No. M50EB00107

Cont. on Sh.10-147 Sh. No.10-146

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

Table 10.5.1.2 Groups I through VI Fault Detection and Recognition

Fault Group	When Detected	When Recognized
I	Manually initiated from Processor Maintenance Panel	The Processor is initialized and faults unconditionally upon detection.
II	The <u>Trouble</u> fault is detected any time that a fault occurs during the formulation and execution of an XED instruction for a fault or external interrupt, or the execution of the SCU instruction which is the first instruction of the vector designated by the XED instruction.	As soon as the Trouble fault is detected the new XED instruction is formed with the address of the Trouble fault vector. A second "snapshot" sequence is not performed.
	<u>Operation not Complete</u> is detected if no strobe \$R is generated by the Control Unit for 1-2 milliseconds; the time interval being determined by a 1-kc oscillator in the Control Unit. No \$R from the Control Unit implies any one of the six conditions listed in Table 10.5.1.1.	As soon as recognized, a "snapshot" and fault sequence is initiated with a fault address corresponding to the Operation not Complete fault vector.

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GENERAL ELECTRIC COMPANY
COMPUTER EQUIPMENT DEPARTMENT
PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh.10-148 Sh. No.10-147

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

Table 10.5.1.2 - contd

Fault Group	When Detected	When Recognized
III	<u>Divide Check</u> and <u>Overflow</u> are detected by the Operations Unit during the execution of an instruction	As soon as recognized and the Memory Controller has responded to the last access request.
IV	The faults in this group (Parity, Illegal Memory Command and Lock-up) are detected after the address preparation cycle that caused the fault. Parity and Illegal Memory Command are detected when an illegal action code is received from the Memory Controller about 0-400 nanoseconds after the Memory Controller has acknowledged the last access request. The Lockup fault is detected from 1-2 milliseconds after an external interrupt request is present and has not been acknowledged.	These faults are recognized as soon as all previous operations have been executed and the Memory Controller has acknowledged the last access request.

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PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh.10-149 Sh. No.10-148

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

Table 10.5.1.2 - contd

Fault Group	When Detected	When Recognized
V	These faults are detected during the address preparation cycle in the Control Unit that generates the fault.	Recognition of these faults takes place after the completion of any instructions currently being executed. Any access to memory for an indirect word or operand for the current instruction being prepared is inhibited.
VI	These faults are detected in the beginning of any address preparation cycle for an operand or indirect word. (Approximately the first 225 nanoseconds into the cycle).	These faults are recognized as soon as the Processor has completed all pending operations provided the Processor is not in Master mode and the interrupt inhibit bit of the current instruction being prepared is not set. Timer Runout is not recognized if the Processor is in Master mode, until a return to Slave mode.

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Spec. No. M50EB00107

Cont. on Sh.10-150 Sh. No.10-149

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

10.5.2 FAULT DETECTION

10.5.2.1 Group I Faults (See 43D163422 sheet 21)

Since the faults in Group I are manually initiated, detection is a matter of converting the manually initiated contact closures to a logic level indicating the presence of the fault.

Startup - When the POWER ON switch is depressed, the power sequencing logic for applying a-c power to all d-c power supplies, initializes the processor to a DIS state by generating a STOP signal for the fault sequence initiation logic in the Base Frame. During the initialize phase, the PSUF flip-flop is set by the sequence initialize logic and remains set until the Processor is initialized and a DIS instruction is forced into the Y- and C-registers. During the PA cycle for the DIS instruction PSUF still set forces a fault sequence for a Startup fault. To recap slightly; detection of the Startup fault is accomplished when the PSUF flip-flop is set by the initialize logic for power on sequencing.

Execute - Detection of the Execute Fault is discussed in detail in paragraph 9.3.12.1.

10.5.2.2 Group II Faults

Trouble (see 43D163422 sheet 17) - The Trouble fault is recognized during the address preparation and execution of an XED instruction for a fault, or during the execution of an SCU instruction as the first instruction of the fault vector pair. This time interval is determined by the set and reset conditions for the WFTB flip-flop. The WFTB flip-flop is set by the strobe \$C that strobes the "brute forced" XED instruction for the particular fault detected into the Y- and C-instruction registers. Termination of the interval is accomplished by the XEded instruction in the fault vectors being successfully loaded into the Y- and C-register (no illegal actions from memory). If an SCU instruction is the first instruction of the fault vector, WFTB is not reset until the SCU instruction is successfully executed.

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GENERAL ELECTRIC COMPANY
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PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh.10-151 Sh. No.10-150

TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR

10.5.2.2 - contd

When WFTB is set, any illegal action from memory, Operation not Complete fault or Illegal Procedure fault sets the TRBL flip-flop initiating a sequence for the Trouble fault. The TRBL flip-flop is reset when a \$C is generated to strobe the XED instruction designating the Trouble fault vector into the Y- and C-registers.

Operation Not Complete (see 43D163422 sheet 21) - This fault is defined by the state of the MSFF flip-flop which determines the start of the 1-2 milli-second interval to detect Operation not Complete:

- 1) MSFF is set by a 1-kilocycle pulse from the Control Unit.
- 2) The PONC flip-flop is set with the next 1-kilocycle pulse from the Control Frame unless a \$R is issued for an interrupt and MSFF is reset.
- 3) PONC being set initiates an Operation not Complete fault.
- 4) PONC is reset as soon as a \$C is issued that results in the XED instruction for a fault being strobed into the Y- and C-registers.

10.5.2.3 Group III Faults

The Group III faults are detected by the Operations Unit during the process of trying to execute an instruction. As a result, the Fault Logic receives one of two levels (FOLF, DVDK) from the Control Unit and generates a GP3 level (BP031F) to start a fault sequence. The flip-flops for holding the FOLF and DVDK levels are contained in the Control Unit. These flip-flops are reset when the XED instruction for the particular fault is strobed into the Y- and C-registers.

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PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh.10-152 Sh. No.10-151

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

10.5.2.4 Group IV Faults

Parity (see 43D163422 sheets 19 and 20). Detection of a parity fault is more difficult than other Processor faults due to the many possible conditions that can cause the fault. In addition, the illegal action strobe from the Memory Controller for a parity error comes approximately 400 nanoseconds after the data is on the lines to the Processor. This means that the Control Unit can be approximately 250 nanoseconds into the next address preparation cycle for an instruction, indirect word or operand before any indication that a parity error has occurred. For these reasons, two-time intervals designated as "windows" are set up to determine where the parity error has occurred, should one occur. Detection of the parity error takes place during the second "window" sequence.

The first window sequence is determined by any one of the following conditions being true:

- 1) RFO
- 2) RFI
- 3) $WI_2 \cdot \overline{RCU}$
- 4) $PI (XDE \cdot SPI)$

RFO (Request for Operand) is a flag set whenever a \$INT to memory is issued for an operand. Resetting of RFO is accomplished by a \$PIN signifying that the Memory Controller has responded to the \$INT.

RFI (Request for Instruction) is a flag set whenever a \$INT to memory is issued for a nonbuffer filling instruction (indirect word SDW, PTW) that is, instructions that are not going into the I-register. Other cases are where an EX or EXI function is generated, an XED instruction in the Y-register is being executed, or a double PI cycle is being executed because of an RCU instruction or access violation. These other cases are defined by the term PI (XDE + SPI).

$WI_2 \cdot \overline{RCU}$ is a term that represents cases where a PI cycle is started to fill the I-register. This includes fetching of the SDW or PTW before the final fetch for the instruction pair.

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GENERAL ELECTRIC COMPANY
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PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh.10-153 Sh. No.10-152

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

10.5.2.4 - contd

$PI(\overline{XDE} \cdot \overline{SPI})$ - is a term which represents the case of parity occurring within a PI cycle as distinguished from the case of parity as the result of a PI cycle.

The first window sequence is necessary to define the different possible cases where parity can occur. These different cases must be defined so certain areas of the Processor can be allowed to proceed or be stopped prior to initiating the fault sequence.

The second window sequence is set to detect the parity fault should one occur. This sequence is defined by any one of the following conditions being true:

- 1) PNO
- 2) PNI
- 3) PNB
- 4) BFPI ($PI(\overline{XDE} \cdot \overline{SPI})$)

PNO (Parity for Operand) is a flag set when the memory has acknowledged an interrupt and the RFO flag was set: ($\$PIN \cdot RFO$.) Reset of PNO occurs with a strobe illegal action ($\$IAL$)-delayed 103 nanoseconds-as a result of a parity error.

PNI (Parity for Instructions) is the flag set when RFI was set at the time that an interrupt was acknowledged by the memory: ($\$PIN \cdot RFI$.) Reset is the same as PNO.

PNB (Parity as a result of buffer filling instructions) is set whenever $WI_2 \cdot RCU$ is true at $\$PIN$ time. Reset is the same as PNO² and PNI.

BFPI this level when true indicates that any parity error should it occur, will take place within a PI cycle started to fill the I-register.

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PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh.10-154 Sh. No.10-153

TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR

10.5.2.4 - contd

Detection of parity errors is possible now that the second window sequence is entered. At this time look at sheet 20 of the logic diagrams and the inputs to the PEO, PEI, PFI, and PWP flip-flops. Any one of these flip-flops becoming set will initiate a fault sequence resulting in a Parity fault vector address. Setting of each flip-flop is a function of a \$IAL (Illegal Action) from the Interface Frame and the PNO, PNI, PNB, BFPI levels in the second window sequence. The way the second window sequence is defined, the only \$IAL that can occur is for a parity error. One other flag is set to further define parity; SEP. The SEP flag is set if PEO was set at the time the Operations Unit started a GS cycle for executing a new operand, after the operand that caused the parity fault was completed.

As stated before, the fault sequence initiation for the Parity fault varies depending on what kind of Parity fault is detected. Paragraph 10.5.3 covers fault sequence initiation.

Illegal Memory Command (see 43D163422 sheet 20) - The Illegal Memory Command fault is generated any time there is an illegal action strobe received from the Interface Frame as a result of a CIOC instruction to a channel masked off in the Memory Controller.

Lockup (see 43D163422 sheet 21) - A Lockup fault is recognized if no \$R is issued (implying no \$INT to memory) for 1-2 milliseconds and an external interrupt or Group VI fault is present. When an external interrupt or Group VI fault is present:

- 1) The IRP flip-flop is set on the next \$C and this indicates an interrupt is present.
- 2) The next 1-kilocycle pulse from the Control Unit sets the LSFF flip-flop unless IRP is reset before the 1-kilocycle pulse arrives. Measuring the time interval for detecting Lockup begins when LSFF is set.

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PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh.10-155 Sh. No.10-154

TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR

10.5.2.4 - contd

- 3) Unless LSFF and IRP are reset before the next 1-kilocycle pulse from the Control Unit arrives, PLUF will set and a Lockup fault routine will be initiated. Resetting of IRP and LSFF is dependent on a \$C resetting IRP; implying that no interrupt is present that is not recognized.

10.5.2.5 Group V Faults

Illegal Descriptor (see 43D163422 sheet 14) - Detection of this fault is checked by the Interface Frame whenever an SDW or PTW is brought in from memory. The Interface Frame checks the descriptor field for an illegal descriptor code, and if one is detected, sends a strobe \$ICF to the fault logic, setting the FID flip-flop. FID set results in a fault sequence being initiated.

Illegal Procedure (43D163422 sheets 10, 11, 12, 14) - The Illegal Procedure fault is generated primarily because of programming violations detected during the execution of a program. There are five cases to be considered:

- 1) GE-645 privileged instructions trying to be executed in Slave mode.
- 2) GE-645 semi-privileged instructions trying to be executed in Slave mode when the Address Base Register designated by the instruction is locked against change.
- 3) Undefined operation codes, including the all zero operation code.
- 4) A Pointer or an address out of bounds.
- 5) Access restrictions on the location being accessed. These restrictions are defined by the descriptor field of the SDW or PTW used to develop the address for the location to be accessed.

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GENERAL ELECTRIC COMPANY
COMPUTER EQUIPMENT DEPARTMENT
PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh. 10-156 Sh. No. 10-155

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

10.5.2.5 - contd

Case 1: The PIF flip-flop (sheet 12) is set whenever any GE-645 instructions that are privilege instructions, are decoded and the Processor is not in Master mode. PIF is set by the \$C (delayed approximately 288 nanoseconds) that started the PA cycle for the instruction, and reset when the wait for trouble (WFTB) flip-flop is reset.

Case 2: Lock base faults are detected in the Base Frame any time that an Address Base Register is about to be changed, the base register has its "lock-base bit" set, and the Processor is not in Master mode. When detected, \$LBF is received by the fault logic and sets the LBF flip-flop (sheet 14). LBF set results in a level to start a fault sequence. Reset of LBF is concurrent with the reset of the wait for trouble flip-flop.

Case 3: The illegal operation codes are detected during the PA cycle for the particular instruction. As with other program type faults, the \$C that started the PA cycle during which the fault was detected, is delayed approximately 288 nanoseconds to give the instruction decodes time to settle before setting any flags. Should a faulty operation code be detected, the FOC flip-flop (sheet 11) is set resulting in a fault sequence being started.

Case 4: Any out of bounds address for a pointer indirect word or operand is detected by the boundary comparator in the Interface Frame. As a result a strobe \$OBF is received by the fault logic to set the OOB flip-flop (sheet 14) and initiate a fault.

Case 5: Access violations for access restrictions write-permit, or class conventions are detected by the Interface Frame and a strobe \$AVF is sent to the fault logic. This results in the AVF flip-flop (sheet 14) being set and initiating a fault sequence.

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GENERAL ELECTRIC COMPANY
COMPUTER EQUIPMENT DEPARTMENT
PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh.10-157 Sh. No.10-156

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

10.5.2.5 - contd

GE-635 Compatibility, GE-635/645 Compatibility, Master mode entry 1-4, Derail, Fault Tag 1-3 (See 43D163422 sheet 12). All these faults are classified as program faults and are lumped together as far as the decodes are concerned. The net result is that the PRF flip-flop is set at \$CA time if a fault is detected. However, as far as defining the different faults are concerned, the fault addresses are different. This is accomplished by developing the different fault addresses required, using specific decode levels from the program faults decode networks that is, CF1, CF2, FLT, MMD, etc. The combination of the various decode levels and the PRF flip-flop initiate the fault sequence and develop the correct fault address.

Directed Faults 0-7 (see 43D163422 sheet 14) - The Directed Faults are detected by the Interface Frame at the same time that the descriptor field of an SDW or PTW is checked for an Illegal Descriptor fault. If a directed fault is detected then a \$DF is generated and sent to the Base Frame fault logic to set the DF flip-flop. Determination of which Directed fault is detected, is developed during the formulation of the fault address encode. The Interface Frame sends the code for the particular fault that was detected. Initiation of the fault sequence is started by the DF flip-flop "setting."

10.5.2.6

Group VI Faults (see 43D163422 sheet 16) - Group VI faults (Shutdown, Timer Runout and Connect) are honored anytime a higher priority fault has not occurred. The setting of the PSHUF, PTROF, or PCON flip-flops will eventually result in the GP6 flip-flop being set with a strobe \$IPR, and initiating a fault sequence. The reset input logic to the PSHUF, PTROF and PCON flip-flops serves two purposes: prevents any one of the individual flip-flops from being reset until a fault is generated for the particular fault detected; results in establishing a priority for the fault address encoded during the formulation of the XED instruction for the Group VI fault detected.

COMPANY CONFIDENTIAL

GENERAL ELECTRIC COMPANY
COMPUTER EQUIPMENT DEPARTMENT
PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh.10-158 Sh. No.10-157

TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR

10.5.2.6 - contd

Group VI fault priority is determined by the fault code address which is generated, rather than the priority logic which leads to starting the fault sequence.

There is a special case for Group VI faults and terminate conditions for "repeat" instructions. Before a terminate condition is serviced, the Processor must not have started another fault sequence for Group VI faults. Assuming this condition is true; the GP6 flip-flop will be reset and the terminate condition serviced by the Processor. If any action had started for servicing a Group VI fault, the GP6 flip-flop will be reset for terminating a "repeat" instruction providing: the GSF flip-flop is set indicating the Interface Frame is stopped; or the CSR flip-flop is set indicating the Control Frame is stopped; or SSI from the Interface Frame is present indicating that a \$INT has been issued and it is safe to start servicing a terminate condition. Terminate must be serviced prior to the beginning sequence for a fault or at the end of the sequence, but before the fault is generated. This is so the state of the various sections of Processor logic concerned is known. If a higher priority fault occurs at the same time as a Group VI fault and terminate condition, the GP6 flip-flop is reset by the term RS6 and the higher priority fault is serviced. However, the term TERM is included in the RS6 equation and would normally reset GP6 for a terminate condition. To prevent this, GP6 is inhibited from being reset by RS6 for a terminate condition. For the repeat terminate condition, signals GSF + CSR + SSI collector reset GP6.

10.5.3 FAULT SEQUENCE INITIATION

A fault sequence to service a detected fault condition is initiated on a priority basis depending on the fault group and type of fault in that group. The logic string for priority determination is shown at the top of 43D163422 sheet 14, and the inputs to the SABT level generation on sheet 15. The string of logic on sheet 14 is primarily to generate the reset terms

COMPANY CONFIDENTIAL

GENERAL ELECTRIC COMPANY
COMPUTER EQUIPMENT DEPARTMENT
PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh.10-159 Sh. No.10-158

TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR

10.5.3 - contd

(RS3, RS41, etc.) for lower priority faults, while the actual priority logic for initiating the fault sequence is shown on sheet 15. Fault priority for Groups I through V is determined by the input logic configuration to the SABB and SFF level generation network and is of the "brute force" type variety; the higher priority overriding the lower priority faults to start a fault sequence and resetting any lower priority faults. Group VI faults are not reset by higher priority faults being serviced, and will eventually initiate a fault sequence. Resetting of the Group VI fault circuitry is entirely dependent on the fault being serviced.

10.5.3.1 SABB and SFF Level Generation (see 43D163422 sheet 15)

Two levels are generated as the result of a detected fault: SABB and SFF. Level SFF stops various portions of the Processor in anticipation of servicing the fault, and level SABB initiates the "snapshot" and "brute-forced" XED sequence for the fault.

An examination of the inputs for SABB generation shows that the presence of a particular fault will generate SABB under the following conditions:

- 1) A particular fault is detected or a fault group level is generated (DF or GP3, etc.)
- 2) Faults below Group III generally require TMCH = 0 before a fault sequence can be initiated thus indicating that the Operations Unit has completed all operations pending.
- 3) The PRSF flip-flop has set indicating the Interface Frame and/or Control Frame has stopped in a condition to start a meaningful fault sequence. Group II and Group I faults do not require PRSF to be set. PRSF can also be set by any one of the appending faults which does not result in a strobe from the Control Unit and Interface Frame to set PRSF (BSPLOF on sheet 14).

COMPANY CONFIDENTIAL

GENERAL ELECTRIC COMPANY
COMPUTER EQUIPMENT DEPARTMENT
PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh.10-160 Sh. No.10-159

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

10.5.3.1 - contd

- 4) The PIN flip-flop in the Control Unit is reset indicating a memory cycle has just been completed or has not yet started.
- 5) The Processor is not halted.
- 6) None of the STOP ON FAULT switches is activated.

When SABT is generated, a "snapshot" sequence for the fault is initiated. In addition to generating SABT to initiate the "snapshot" sequence, a level designated SFF is generated to stop certain areas of the Control Unit and Interface Frame in the proper state for the "snapshot" sequence. Level SFF can be generated without SABT for those cases where any one of the four STOP ON FAULT switches on the Maintenance Panel are set. This results in the Processor stopped just prior to entering the "snapshot" sequence.

10.5.3.2 Snapshot Counter (see 43D163422 sheet 18)

Generation of the "snapshot" sequence begins with SABT generating a pulse to set the PSN flip-flop. The same pulse is also started down a delay line of approximately 324 nanoseconds. As a result of SABT, the PSN, SNO, SN1 and WF flip-flops are set at intervals of approximately 324 nanoseconds. When SNO resets, a SSNO is generated for the first "snapshot" pulse. When SN1 resets, an SSN1 is generated which performs the second half of the "snapshot" sequence. Setting of WF results in the majority of all Processor circuits (except the Operation Unit which is initialized by SABT) being initialized. When WF resets, SABT is generated which regenerates a SC in the Control Frame, starting a prepare cycle for the "brute forced" XED instruction for the fault.

10.5.3.3 Fault Address Encode (see 43D163422 sheet 13)

The fault address for the particular fault is developed from a logic network for each of the five bits of the address; FA_A being the most significant bit and FA_E

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GENERAL ELECTRIC COMPANY
COMPUTER EQUIPMENT DEPARTMENT
PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh.11-1 Sh. No.10-160

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

10.5.3.3 - contd

being the least significant. A trailing zero is assumed in the fault address. The various levels $FA_A - FA_E$ are strobed into a fault code register concurrent with a $\$C \cdot WF$ which occurs at the end of the "snapshot" sequence. The contents of the fault code register are saved to be stored by an SCU instruction.

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GENERAL ELECTRIC COMPANY
COMPUTER EQUIPMENT DEPARTMENT
PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh. 11-2 Sh. No. 11-1

TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR

11.0 ASSOCIATIVE MEMORY UNIT
 DETAILED OPERATION

In order to implement paging, relocation, and protection of user programs the GE-645 operating system generates and maintains Descriptor Segment and Page Tables. Each time a user program attempts to access memory these tables must be referenced to obtain the absolute core location and to determine the users access rights. This procedure requires two or three memory accesses prior to an instruction or an operand fetch. In order to reduce this overhead, an Associative Memory consisting of 16 hardware registers is provided. It accepts as a reference either the effective base register (pointer), or the pointer and page number, and produces the page table location, or the block location of the page respectively. Each register has a Usage Counter (4 bits) that indicates the recency of its use with respect to the other registers. To supplement the above actions the GE-645 instruction repertoire provides the operating system three instructions for controlling the Associative Memory.

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GENERAL ELECTRIC COMPANY
COMPUTER EQUIPMENT DEPARTMENT
PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh. 11-3 Sh. No. 11-2

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

11.1 FUNCTION

The Associative Memory is constructed around sixteen 60-bit Associative Registers (ARn). The breakdown of each register is as follows:

Bits 0-17	Address Field
Bit 18	Base Bit
Bits 19-26	Boundary/Page No. Field
Bits 27-35	Descriptor Field
Bits 36-53	Pointer Field
Bit 54	Empty/Full
Bit 55	Adjust Usage Count
Bits 56-59	Usage Counter

An Associative Register may contain either a Segment Descriptor Word (SDW) or a Page Table Word (PTW). The meanings of the above fields may vary depending upon which type word is stored in that register.

11.1.1 SDW

Address Field -- It is always modulo 64. If the segment is not paged the address is the base address of the segment. If the segment is paged the address is the base address of the Page Table.

Base Bit -- It must be a "1" (a "1" means that this is a SDW)

Boundary/Page No. Field -- This is the segment boundary. It contains the number of pages in the segment.

Descriptor Field -- Each bit has its own meaning.

27 if a "1" the segment consists of 64 word pages, and if a "0" it consists of 1024 word pages.

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GENERAL ELECTRIC COMPANY
COMPUTER EQUIPMENT DEPARTMENT
PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh.11-4 Sh. No.11-3

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

11.1 - contd

- 28 if a "1" the segment is not paged, and if a "0" it is paged.
- 29 not used.
- 30 if a "1" the information stored in that segment may be altered (that is, written into), and if a "0" it may not be altered by a slave procedure.
- 31 if a "1" this segment may be accessed (that is, read from) in Slave mode, and if a "0" it may be accessed only in Master mode.
- 32 not used.
- 33-35 contain a code that describe the type of segment as follows:
 - 001 - Data--This segment contains only data and may not be accessed to obtain instructions.
 - 011 - Procedure Only--This segment is to be only self accessed or accessed by Master Procedure.
 - 010 - Procedure Slave--This segment may contain both data and instruction. There are no restrictions on access, other than the access and write permits.
 - 100 - Procedure Master--This segment is the same as Procedure Slave except that access is restricted to Master mode, and privileged instructions may be specified.

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COMPUTER EQUIPMENT DEPARTMENT
PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh. 11-5 Sh. No. 11-4

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

11.1.1 - contd

Pointer Field -- This is the SDW identification. It contains the location (page number and word number of the Descriptor Segment) relative to the Descriptor Segment Base Address from which the SDW was originally obtained.

Empty/Full -- If this bit is a "1" it indicates that the information in this register is valid, and if it is a "0" it indicates that the register has been cleared and the information in it is no longer valid.

Adjust Usage Counter -- This bit is used for internal control only. Whenever it is a "1" the Usage Counter of that register must be decremented by "1." When stored by SAM or SAZ it should appear as a "0."

Usage Counter -- This counter is used to keep track of the order in which the registers have been used. The last used register will have a count of 15, the next last used register will be 14, and on down to zero.

11.1.2 PTW

Address Field -- It is always modulo 64. If the page is a small page all 18 bits will be the base address of the page. If it is a large page bits 0-13 will be the base address of the page, which in effect makes the address modulo 1024.

Base Bit -- It must be a "0."

Boundary/Page No. Field -- This contains the page number of the page referenced by this PTW. It is part of the identification of this PTW.

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GENERAL ELECTRIC COMPANY
COMPUTER EQUIPMENT DEPARTMENT
PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh. 11-6 Sh. No. 11-5

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

11.1.2 - contd

Descriptor Field -- All bits in this field have the same meaning as for a SDW except bit 29. If bit 29 is a "1" information in this page has been altered (the page has been written into).

Pointer Field -- This, along with the Page No. Field is the identification of this PTW. It contains the location of the SDW that pointed to this PTW.

All other fields are the same for a SDW.

If the Associative Register contains a SDW (bit 18 = "1"), then bits 0-17 and 19-35 hold the SDW information and bits 36-53 hold the associative address. If the AR contains a PTW (bit 18 = "0"), then bits 0-17 and 27-35 hold the PTW information and bits 19-26 and 36-53 hold the associative address.

11.1.3 ASSOCIATIVE MEMORY CYCLES

In order to carry out its tasks, the Associative Memory must execute the following cycles:

Search ✓
Write ✓
Read ✓
Adjust Usage Counters ✓
Clear ✓

Search -- Any time the Control Frame attempts to obtain an instruction, an operand, or an indirect word from core memory, except in Absolute mode with bit 29 off, the Associative Memory will be interrogated to see if it contains the required SDW or PTW. The search cycle first determines if any of the 16 ARs contain a pointer supplied by the Base Frame. If it finds a match it determines if the match is with a SDW (bit 18 a 1) or with PTW (bit 18 a 0). If it is a PTW, it will compare the PTW page number with the page number supplied by the

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GENERAL ELECTRIC COMPANY
COMPUTER EQUIPMENT DEPARTMENT
PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh. 11-7 Sh. No. 11-6

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

11.1.3 - contd

Control Frame. If they are identical, the Associative Memory sends the PTW to the Interface Frame and tells it to use this information to fetch the instruction, operand, or indirect word. If the page numbers are not identical, it reverts to a SDW search. If the match is a SDW, it checks to see if the segment is paged. If the segment is not paged, the Associative Memory sends the SDW to the Interface Frame and tells it to use this information to fetch the instruction, operand, or indirect word. If the segment is paged, the Associative Memory sends the SDW to the Interface Frame and tells it to use this information to fetch the proper PTW. If a match is found, bit 54 is checked to see if the information is valid. If it is not valid, the match will be ignored. If a read out occurs, the information will remain on the data out lines until the Interface Frame signifies that it has received it. If the proper PTW or SDW is not found, the Associative Memory will notify the Interface Frame of this fact and terminate its cycle.

Write -- Any time the Interface Frame receives a PTW or a SDW from core memory and no Directed Fault is detected that word will be written into the Associative Memory along with the proper identification. The Associative Memory will start this cycle when notified by the Interface Frame, which will also indicate what kind of a word is to be stored. The Associative Memory will then select the AR with a usage count of zero. If the incoming word will be a SDW it will be stored in that AR along with the pointer from the Base Frame. If the incoming word will be a PTW it will be stored in that AR along with the pointer from the Base Frame and the page number from the Control Frame. In both cases the proper control bits will be set or reset. When the PTW or SDW is available the Interface Frame will notify the Associative Memory of this fact via a strobe. This strobe initiates the actual write operation. The Write Cycle is always followed by an Adjust Usage Counter Cycle.

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GENERAL ELECTRIC COMPANY
COMPUTER EQUIPMENT DEPARTMENT
PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh. 11-8 Sh. No. 11-7

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

11.1.3 - contd

Read -- A Read Cycle will be entered if a match is found during a Search Cycle, or if a Store Associative Memory (SAM) or Store Associative Memory Zero (SAZ) command is executed. If a match is found during a Search Cycle the Associative Memory will initiate the Read Cycle itself. It will place the contents of bits 0-35 of the selected AR on the data lines to the Interface Frame, and at the same time it will generate a Strobe Start Fetch. During a SAM or SAZ instruction the Base Frame initiates the Read Cycle by placing a "1" upon the proper command line, and at the same time it supplies the information as to which AR should be read. All 60 bits of the selected AR will be placed on the data out lines to the Interface Frame.

Adjust Usage Counters -- This cycle will be entered any time an AR is read out due to a match, or following any Write Cycle. During this cycle any AR that has a usage counter higher than the count of the AR that contains the matched word or the new word will have its count decremented by one. The active AR will have its count maximized (15).

Clear -- This cycle will be initiated by a CAM or LDBR instruction causing the Base Frame to place a "1" on the Clear command line. All 16 Empty/Full bits will be reset to "0," and all Usage Counters will be set to their initial values.

11.1.4 ASSOCIATIVE MEMORY INSTRUCTIONS

The GE-645 can execute three instruction that directly affect the Associative Memory. They are:

Store Associative Memory Zero (SAZ)
Store Associative Memory (SAM)
Clear Associative Memory (CAM)

All three instructions can only be executed in Master mode.

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GENERAL ELECTRIC COMPANY
COMPUTER EQUIPMENT DEPARTMENT
PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh. 11-9 Sh. No. 11-8

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

11.1.4 - contd

Store Associative Memory Zero (SAZ) -- This instruction will cause the AR with a usage count of zero to be stored in the core location specified by the instruction (Y) and that location plus one (Y+1) as follows:

Y	0 - 35	AR	0 - 35
Y + 1	0 - 23	AR	36 - 59
Y + 1	24 - 35		Zeros

If the address requires appending the Associative Memory will be locked out so that its contents will not be altered before they are stored.

Store Associative Memory (SAM) -- This instruction will cause all 16 ARs to be stored in core memory. They will be stored by physical location, as determined by the initial usage count. ARO will be stored in Y and Y+1, AR1 will be stored in Y+2 and Y+3, ..., AR15 will be stored in Y+30 and Y+31. The bit placement will be the same as for the SAZ instruction. If the address requires appending the Associative Memory will be locked out so that its contents will not be altered before they are stored.

Clear Associative Memory (CAM) -- This instruction will clear out the Associative Memory by resetting all Empty/Full bits to 0 and setting all Usage Counters to their initial value.

11.1.5 INTERFACE SIGNALS

The Associative Memory receives signals from the Base Frame, Control Frame, and Interface Frame. It sends signals to the Interface Frame. (See Fig. 11.1.)

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GENERAL ELECTRIC COMPANY
COMPUTER EQUIPMENT DEPARTMENT
PHOENIX, ARIZONA

Spec. No. CM50EB00107

Cont. on Sh. 11-10 Sh. No.11-9

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

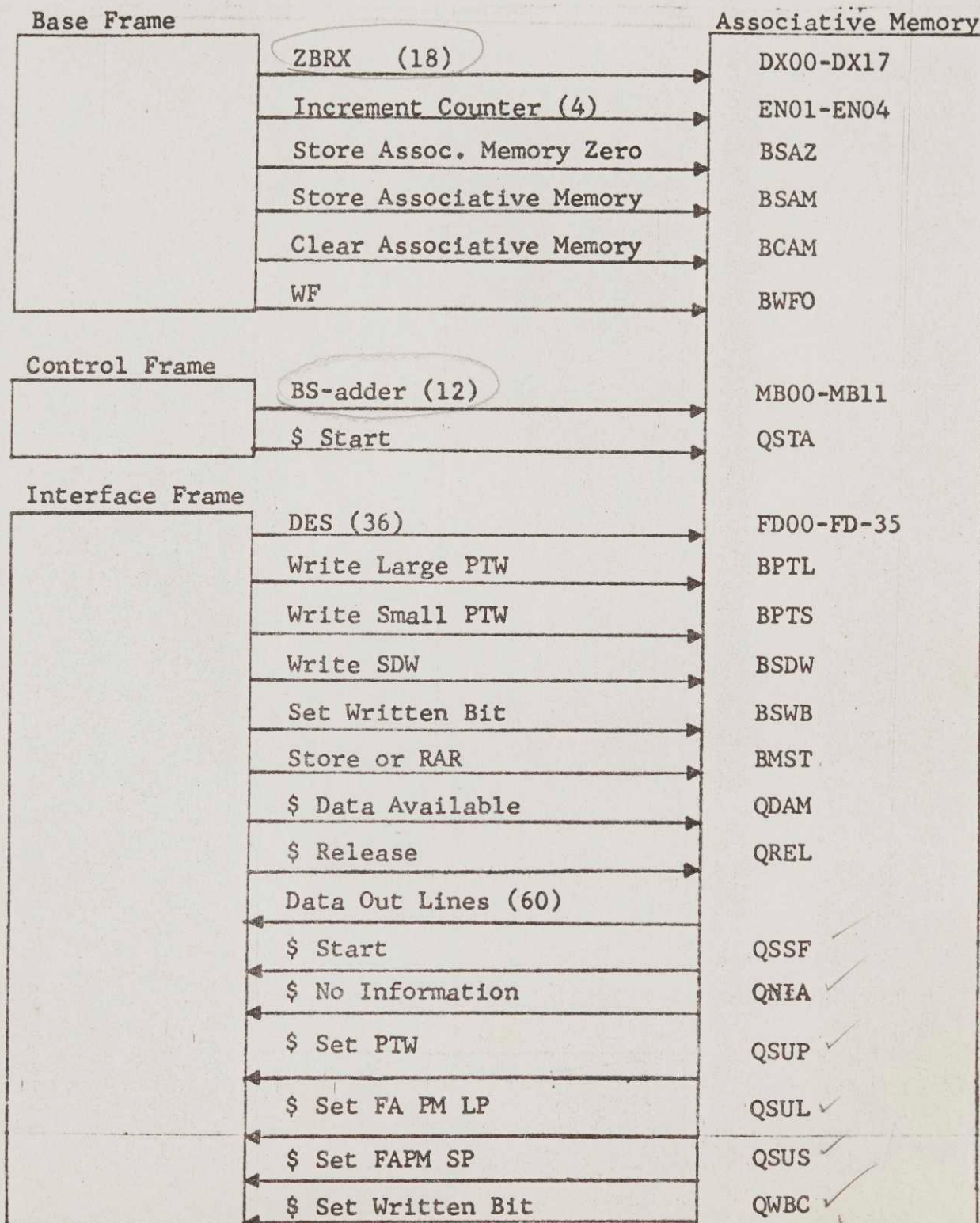


Fig.11.1.5 Associative Memory Interface Signals

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Spec. No. M50EB00107

Cont. on Sh. 11-11 Sh. No. 11-10

TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR

11.1.6 MANUAL OPERATION

The operation of the Associative Memory can be modified by switches on the Maintenance Panel. If the Test Enable Signal is true and the TEST CLOCK switch is in the FAST position the three delay lines that produce QP111, QP221, and QP331 will be shortened. If the Test Enable signal is true and the SF ENABLE switch is in the STEP position the operation of the search cycle is interrupted. It will stop just before the generation of QP111, or QP221, or QP331. Depressing the SF STEP switch will generate the required pulse and the search cycle will continue up to, but not including the next pulse. To return to normal operation the SF ENABLE switch must be returned to normal and the SF STEP depressed once.

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GENERAL ELECTRIC COMPANY
COMPUTER EQUIPMENT DEPARTMENT
PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh.11-12 Sh. No. 11-11

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

11.2 THEORY OF OPERATION

In order to understand the operation of the Associative Memory, an understanding of the philosophy of segmentation, paging, and how it is implemented in the GE-645 is required. This discussion assumes that the reader has this knowledge. The operation of the Associative Memory can be divided into four parts. These parts will be taken up separately in this order: Interface, Basic Operating Cycles, Instructions, and Manual Operation.

11.2.1 INTERFACE

The Interface between all affected frames in the Processor and the Associative Memory are listed by EDA mnemonic in Tables 11.2.1 and 11.2.1a.

COMPANY CONFIDENTIAL

GENERAL ELECTRIC COMPANY
COMPUTER EQUIPMENT DEPARTMENT
PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh. 11-13 Sh. No. 11-12

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

Table 11.2.1

Associative Memory Inputs

Mnemonic

Description

Base Frame

BCAMF (CAM)	➤ CLEAR ASSOC.MEMORY
BSAMF (SAM)	STORE ASSOC.MEMORY
BSAZF (SAZ)	STORE ASSOC.ZERO
DXOOF-DX17F (ZBRXO-17)	BASE REGISTER EXTERNAL BUS
ENO1F-ENO4F (INCL-4)	INCREMENTOR REGISTER
EWFOF (WF)	WF ABORT F/F

Control Frame

MBOOB-MB11B (BSO-11)	ADDRESS BASE ADDER
QSTAB (\$	START ASSOC.MEMORY PULSE

Interface Frame

BMSTM	DECODE FOR STORE OR RAR CYCLES TO ASSOC.MEMORY
■ BPTLM (WPTWL)	WRITE PTW LARGE
■ BPTSM (WPTWS)	WRITE PTW SMALL
■ BSDWM (WSDW)	WRITE SDW
ESWBM	
FDOOM-FD35M (DESO-35)	36-BIT DESCRIPTOR REGISTER
QDAMM (\$DAAM)	DATA AVAILABLE PULSE
QRELM (\$RELEASE)	RELEASE PULSE

Maintenance Panel

SQS1T	TEST CLOCK SWITCH
SQS1T	TEST CLOCK SWITCH
SQS2T	TEST CLOCK SWITCH
SQS2T	TEST CLOCK SWITCH
SSSET	ENABLE STEP SWITCH
SSSET	ENABLE STEP SWITCH
SSSTT	STEP SWITCH
SSSTT	STEP SWITCH
STSTT	TEST SWITCH
STSTT	TEST SWITCH

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GENERAL ELECTRIC COMPANY
COMPUTER EQUIPMENT DEPARTMENT
PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh.11-14 Sh. No. 11-13

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

Table 11.2.1a

Associative Memory Outputs

Mnemonic

Description

Interface Frame

DC30E-DC35E (ZADS30-35)	ASSOC. REG. DESCRIPTOR BUS
BA55E (ZAU55)	ASSOC. REG. ADJUST USAGE BIT BUS
BE54E (ZEF54)	ASSOC. REG. EMPTY/FULL BIT BUS
BU56E-BU59E (ZSUC56-59)	SELCTD. USAGE COUNTER BUS
DAOOE-DA17E (ZASMO-17)	ADDRESS MOD. 64 BUS
DB18E (ZBB18)	BASE BIT BUS
DB19E-DB26F (ZABD19-26)	BOUNDARY BUS
DC27E-DC29E (ZADS27-29)	ASSOC. REG. DESCRIPTOR BUS
DT36E-DT53E (ZPTR50-53)	ASSOC. POINTER BUS
QNIAE (\$NIA)	NO INFORMATION AVAILABLE PULSE
QSSFE (\$SF)	START FETCH PULSE
QSULE (\$SET FA PMLP)	SET UP FAPM (LP) FETCH PULSE
QSUPE (\$SET PTW)	SET UP PTW FETCH PULSE
QSUSE (\$SET FA PMSP)	SET UP FAPM (SP) FETCH PULSE
QWBCE (\$START WBC)	START WRITTEN BIT CYCLE

Maintenance Panel

EAUVE	ADJUST USAGE VALUE F/F
EPSHE	POINTER SEARCH F/F
EPSLE	PTW (LARGE) SEARCH F/F
EPSSE	PTW (SMALL) SEARCH F/F
ERELE	RELEASE F/F
ESCRE	STROBE COUNTER RELEASE F/F
ESDPE	SDW PRESENT F/F
ESDSE	SDW SEARCH F/F

Relay Box

BA55E (ZAU55)	ASSOC. REG. ADJUST USAGE BIT BUS
BE54E (ZEF54)	ASSOC. REG. EMPTY/FULL BIT BUS
BU56E-BU59E (ZSUC56-59)	SELCTD. USAGE COUNTER BUS
DAOOE-DA17E (ZASMO-17)	ADDRESS MOD. 64 BUS
DB18E (ZBB18)	BASE BIT BUS
DB19E-DB26E (ZABD19-26)	BOUNDARY BUS
DC27E-DC35E (ZADS27-35)	ASSOC. REG. DESCRIPTOR BUS
DT36E-DT53E (ZPTR50-53)	ASSOC. POINTER BUS

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GENERAL ELECTRIC COMPANY
COMPUTER EQUIPMENT DEPARTMENT
PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh. 11-15 Sh. No. 11-14

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

11.2.2 BASIC OPERATING

There are five basic operating cycles and a terminate condition.

- 1) Search Cycle initiated by the Control Frame ✓
- 2) Write Cycle initiated by the Interface Frame ✓
- 3) Read Cycle initiated by the Associative Memory or Base Frame
- 4) Adjust Usage Counters Cycle initiated by the Associative Memory
- 5) Clear Cycle initiated by the Base Frame
- 6) Termination

11.2.2.1 Search Cycle

Any time the Processor performs an appending operation on an address, the Associative Memory is searched to see if it contains the information necessary for this operation. There are ten possible combinations of matches or no matches. These are shown in Fig. 11.2.2.1 along with the pulses that will be generated and sent to the Interface Frame for each combination. Following the test on the Search Cycle are several sample timing diagrams.

The Control Frame prepares the address to be appended. When it determines that the address will be ready by the time it is needed it issues a QSTAL to the Associative Memory and a \$ Append to the Interface Frame. At this time the Base Frame will have placed the pointer on the DX00-DX17 (ZBRX₀₋₁₇) lines.

↑
segment #

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PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh.11-16 Sh. No.11-15

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

Table 11.2.2.1 Search Possibilities vs. Pulses
Generated and Sent to Interface Frame

Pointer Match	Non- paged SDW	Paged SDW Large	Paged SDW Small	PTW Large	PTW Small	QNIAl	QSUL1	QSUS1	QSUP1	QSSF1	
No						X					nothing
Yes Large Page						X	X				wrong large PTW
Yes Small Page						X		X			wrong small PTW
Yes	Yes									X	Non paged SDW
Yes		Yes					X		X	X	SDW-large no PTW
Yes			Yes					X	X	X	SDW-small no PTW
Yes		Yes		Yes			X			X	PTW large +SDW
Yes			Yes		Yes			X		X	PTW small +SDW
Yes				Yes			X			X	PTW large only
Yes					Yes			X		X	PTW small only.

No match

large paged

small paged

No PTW, but SDW

Some match

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Spec. No. M50EB00107

Cont. on Sh. 11-17 Sh. No. 11-16

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

11.2.2.1 - contd

QSTAl starts the Search Cycle by entering a delay line, from which it will emerge as QP111 in 216 nanoseconds. During this interval of time the pointer search is accomplished. The information on the DX00-DX17 lines is compared with each Associative Register (A through S), bits 36 through 53. If any ARs pointer matches DX00-DX17 and its Empty/Full bit is a "1" a level will come true that will switch that AR onto the data-out lines and will cause BGMA1 to become true. In the case where more than one AR has a match the output of the matching ARs will be ORed together on the data out lines.

QP111 when it emerges from the delay line will do the following:

- 1) Reset EPSH if there is a match with a paged SDW or a PTW.
- 2) Set ESDP if there is a match with a SDW.
- 3) Send a QSSF1 pulse to the Interface Frame if there is a match with a nonpaged SDW.
- 4) Send a WSUL1 pulse to the Interface Frame and set EPSL if there is a match with a large paged SDW or a large PTW.
- 5) Send a QSUS1 pulse to the Interface Frame and set EPSS if there is a match with a small paged SDW or a small PTW.
- 6) Send a QNIA1 pulse to the Interface Frame if there is no match.

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Spec. No. M50EB00107

Cont. on Sh.11-18 Sh. No.11-17

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

11.2.2.1 - contd

QP111 will enter another delay line if there is a match with a paged SDW or a PTW. It will emerge in 234 nanoseconds as QP211. If a QNIA pulse was generated the Associative Memory will wait until the Interface Frame has obtained the required SDW and upon signal it will enter a Write Cycle. If a QSSF1 pulse was generated a Read Cycle will be entered.

During the interval of time between QP111 and QP211 the PTW search is performed. The exact nature of this search will depend upon whether it is looking for a large or small PTW.

EPSL set (search for large PTW)

pages In this case DX00-DX17 is compared against bits 36-53 of all ARs and MB00-MB07 is compared against bits 19-26 of all ARs. If a match exists, the Empty/Full bit is a "1," and the Base bit is a "0" a level will come true that will switch that AR onto the data out lines and BGMA1 will come true. *(pointer)*

QP211 when it emerges from the delay line will do the following:

- 1) Send a QSSF1 pulse to the Interface Frame if a match is found and either the operation is not a Write or RAR or the Written bit of the PTW is a "1."
- 2) Send a QSUP1 pulse to the Interface Frame, set ESDS, reset EPSL, and reset EPSS if there is no match, but there is a SDW present.
- 3) Send a QWBC1 pulse to the Interface Frame if there is a match, the operation is a write or RAR, and the Written bit is a "0."

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PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh.11-19 Sh. No.11-18

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

11.2.2.1 - contd

- 4) Send a QNIA1 pulse to the Interface Frame if there is no match and there is no SDW present.

QP211 will enter another delay line if there is no match, but there is a SDW present. It will emerge in 216 nanoseconds as QP311.

EPSS set (search for small PTW)

In this case DX00-DX17 is compared against bits 36-53 of all ARs and MB04-MB11 is compared against bits 19-26 of all ARs. If a match exists, the Empty/Full bit is a "1," and the Base bit is a "0" a level will come true that will switch that AR onto the data out lines and BGMA1 will come true.

QP211 when it emerges from the delay line will do the same things as when EPSL is set.

In either case if a QNIA1 was generated the Associative Memory will wait until the Interface Frame has obtained the required SDW and upon signal it will enter a Write Cycle. If a QSSF1 was generated a Read Cycle will be entered.

During the interval of time from QP211 to QP311 a SDW search will be performed. Because of the conditions required to enter this portion of the search cycle it is known that a match will be made. The problem is to find the AR that contains the right SDW. This is done by comparing DX00-DX17 against bits 36-53 of all ARs. A match will exist with one AR that also has its Empty/Full bit a "1" and its Base bit, a "1," which will cause a level to come true switching that AR onto the data out lines, and BGMA1 will come true.

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COMPUTER EQUIPMENT DEPARTMENT
PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh.11-20 Sh. No.11-19

TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR

11.2.2.1 - contd

QP311 when it emerges from the delay line it will send a QSSF1 to the Interface Frame and the Read Cycle will be entered. This completes the Search Cycle.

There is a special case dealing with the Written bit. Any time a page in core memory is written into by a store instruction or a RAR operation this fact is remembered by setting the Written bit to a "1" in both the PTW in core memory and the PTW in Associative Memory. This operation is necessary only on the first occasion of the page being written into. If a PTW with the Writtenbit a "0" is obtained from core memory for a store or RAR the Interface Frame will handle the setting of the Writtenbit of the PTW in core memory and will set the Writtenbit in the PTW before it is sent to the Associative Memory to be stored. When a PTW match is found in the Associative Memory the BMST1 line from the Interface Frame and the Written bit are checked. If the BMST1 line is a "1" and the Written bit is a "0" the Associative Memory will send a QWBC1 pulse to the Interface Frame. The Interface Frame will place a "1" on the BSWB1 line and then set the Writtenbit of the PTW in core memory. A "1" on the BSWB1 line will cause bit 29 (Written bit) of the AR containing that PTW to be set to a "1."

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PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh.11-21 Sh. No.11-20

TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR

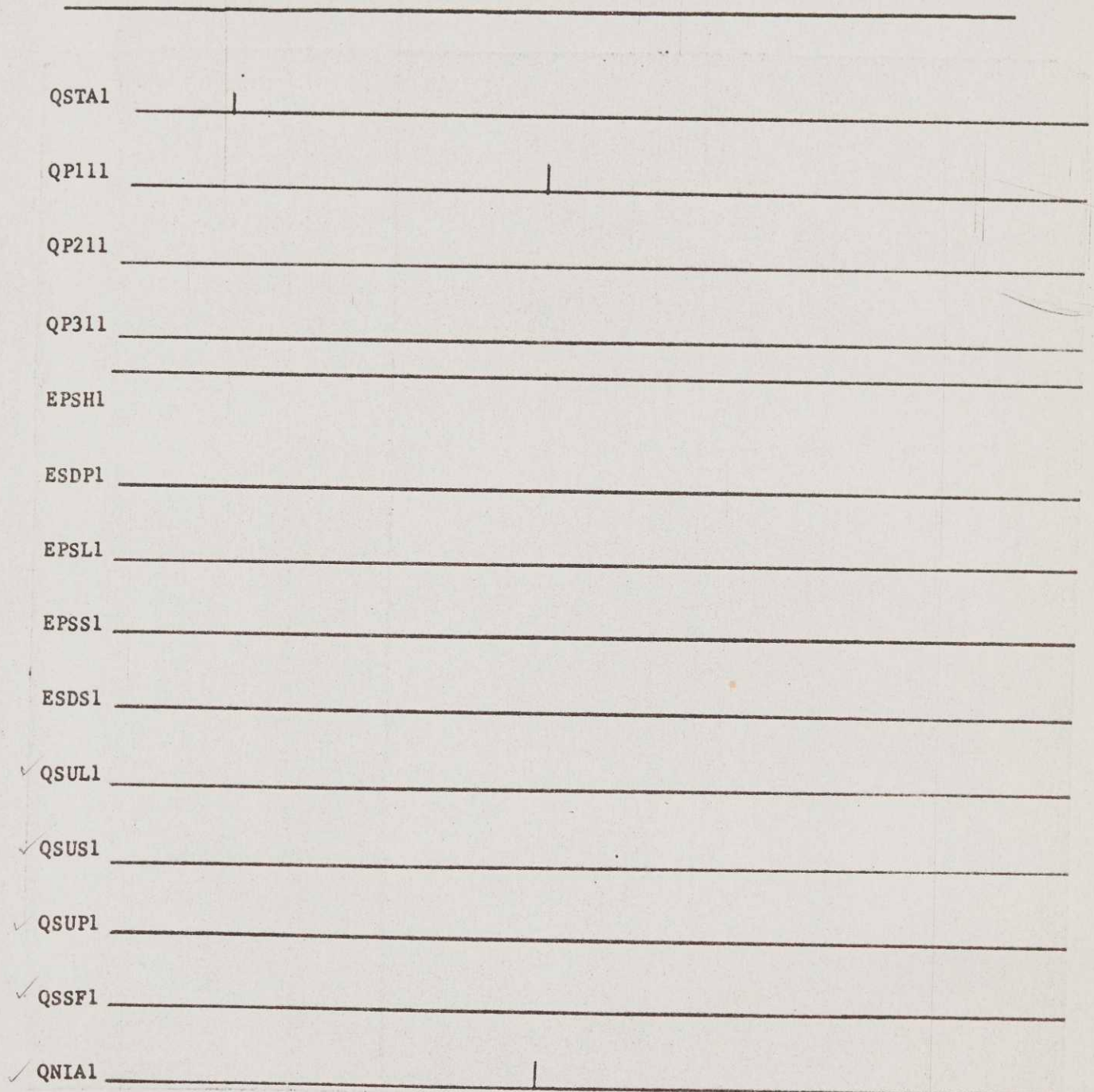


Fig. 11.2.2.1 No Match, Timing Diagram

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Spec. No. M50EB00107

Cont. on Sh.11-22 Sh. No.11-21

TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR

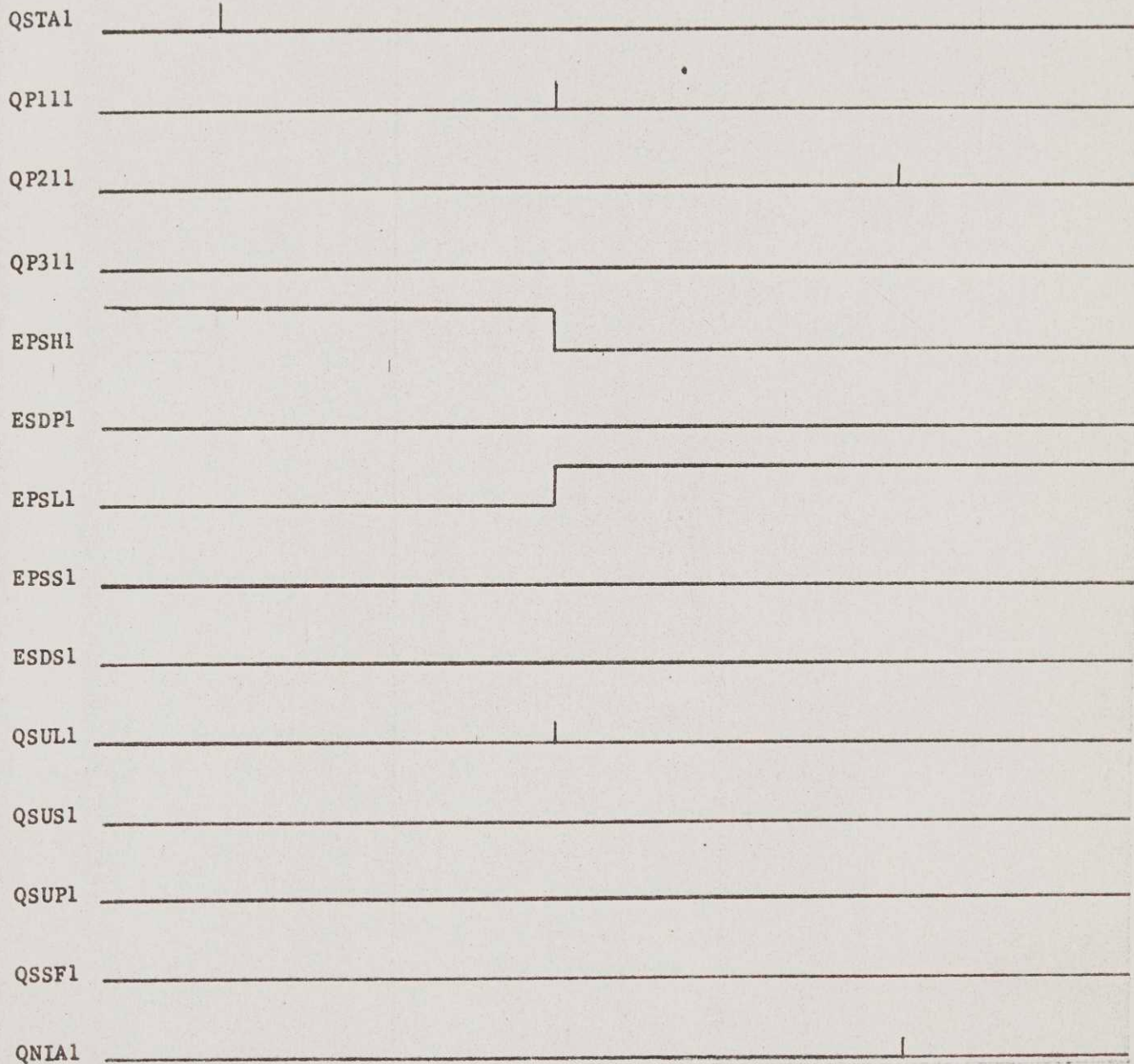


Fig. 11.2.2.1a Pointer Match for Large Page, No SDW or
PTW Match, Timing Diagram

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Spec. No. M50EB00107

Cont. on Sh.11-23 Sh. No.11-22

TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR

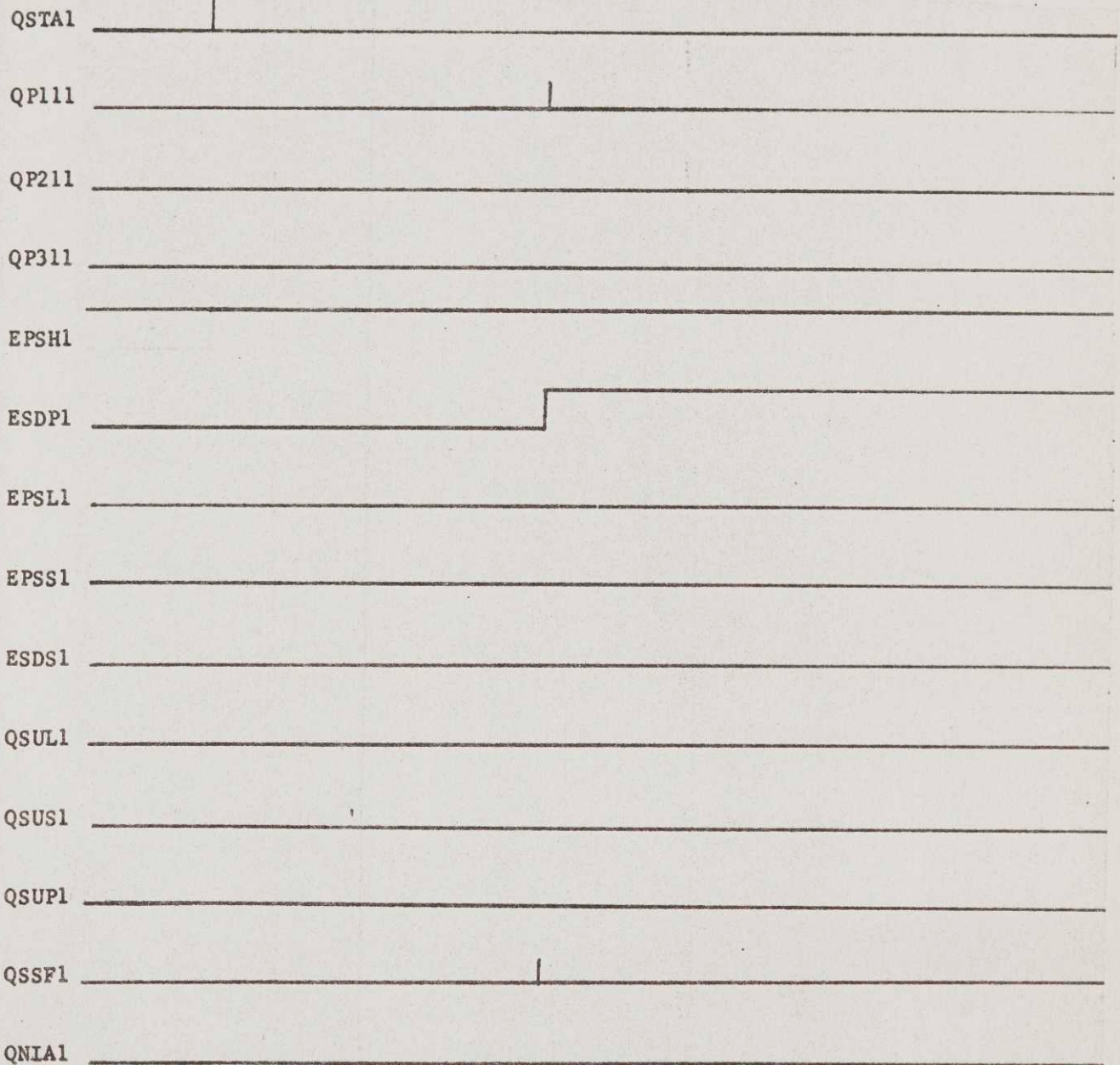


Fig. 11.2.2.1b SDW Match (nonpaged), Timing Diagram

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Spec. No. M50EB00107

Cont. on Sh. 11-24 Sh. No. 11-23

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

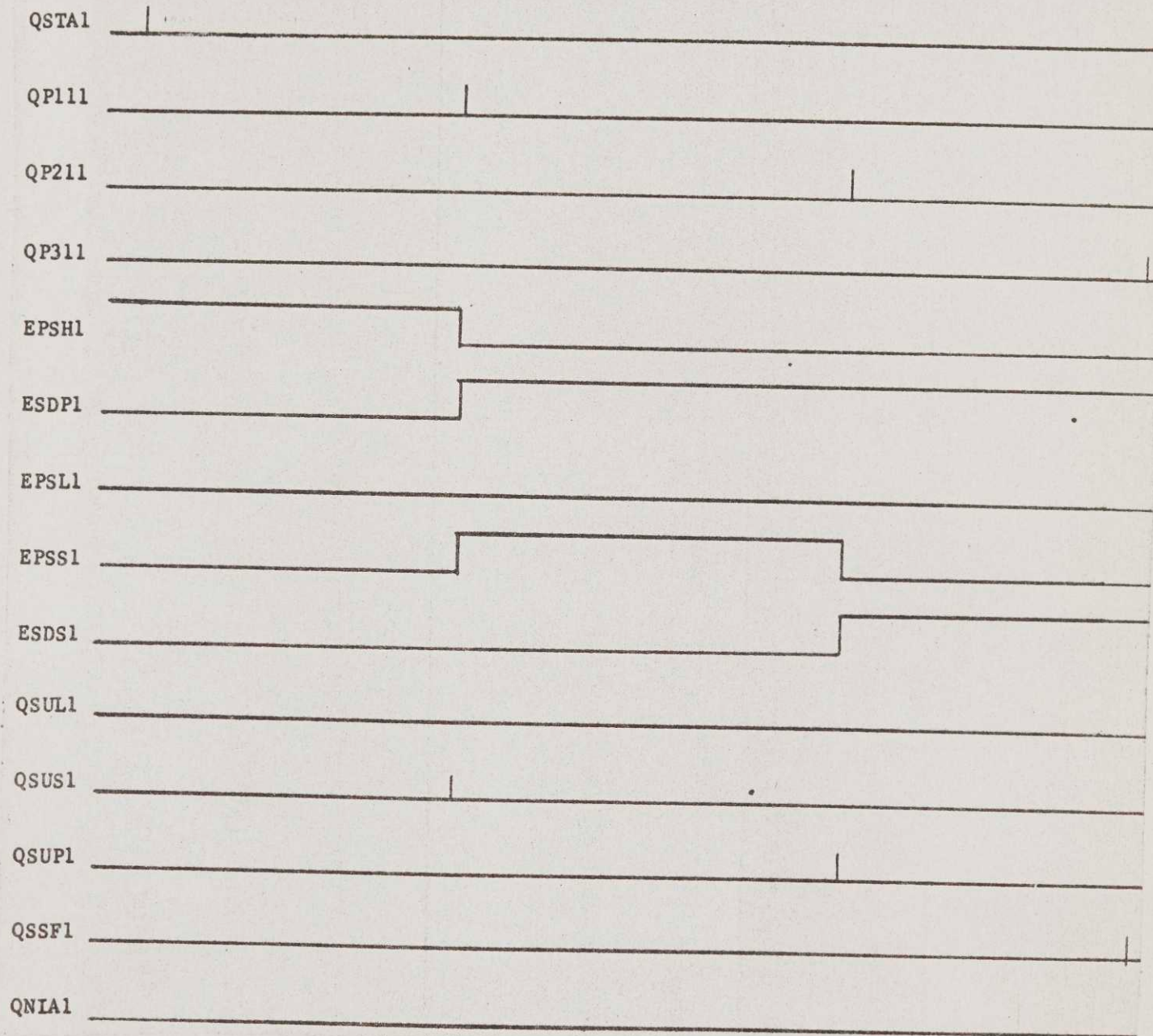


Fig. 11.2.2.1c Match SDW for Small Page, Timing Diagram

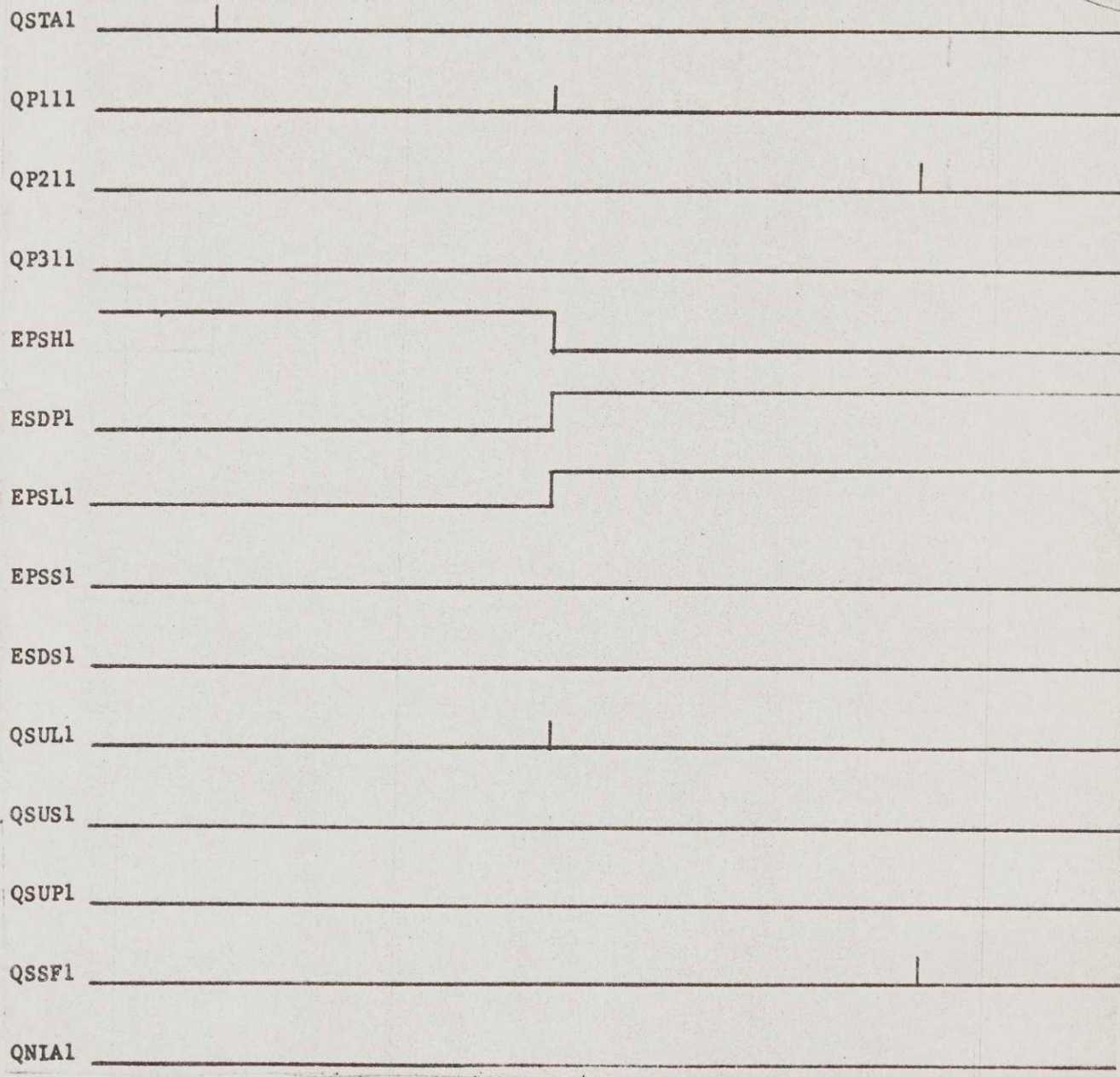
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Spec. No. M50EB00107

Cont. on Sh. 11-25 Sh. No. 11-24

TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR



NOTE - Written bit of PTW = "1"

Fig. 11.2.2.1d Match SDW for Large Page and PTW, Timing Diagram

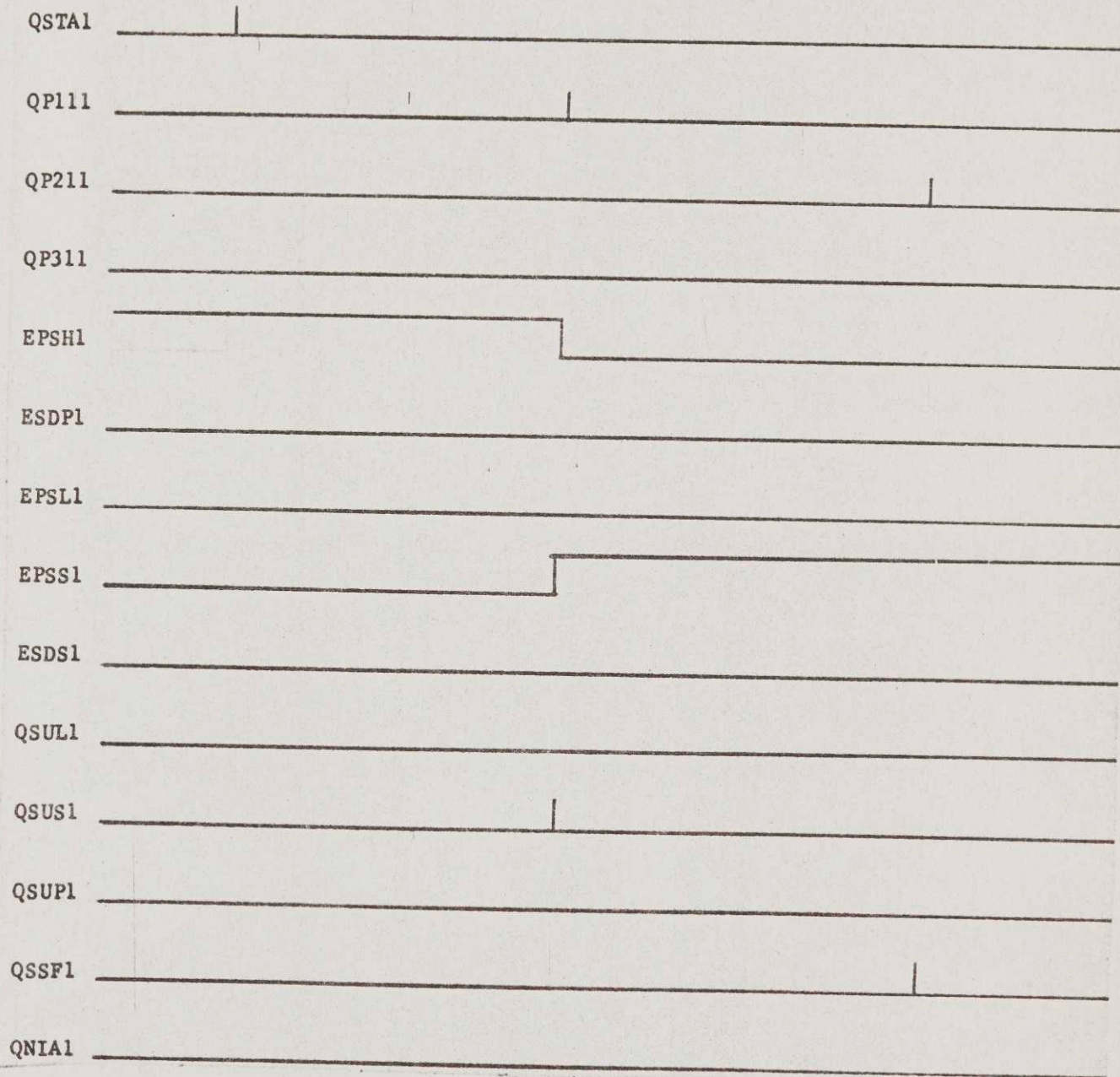
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Spec. No. M50EB00107

Cont. on Sh. 11-26 Sh. No. 11-25

TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR



— Fig. 11.2.2.1e Match PTW for Small Page No SDW, Timing Diagram

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PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh.11-27 Sh. No.11-26

TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR

11.2.2.2 Write Cycle

A Write Cycle will store a PTW or a SDW in the Associative Register that has a usage count of zero. The Interface Frame upon obtaining a SDW or a PTW from core memory will store it in the Descriptor Register, and will check the descriptor field for a Directed Fault. If there is no fault it will update the descriptor field and place a 1 on one of three command lines to the Associative Memory. The command line selected depends upon the type of word to be stored. The three command lines are:

- 1) BSDW1 - Write a SDW
- 2) BPTL1 - Write a large PTW
- 3) BPTS1 - Write a small PTW

To write into the Associative Memory the Interface Frame will place the contents of the Descriptor Register on the FD00-FD35 lines and a 1 on a command line. When a command line goes high the Associative Memory will switch the input lines to all 16 ARs as per Table 11.2.2.2. The Interface Frame will then place a pulse on the QDAM1 line, which will select the AR with a usage count of zero and issue a strobe to that AR only. This strobe will write the input information into the selected AR. The Adjust Usage Counters Cycle will be entered at this point.

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PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh.11-27 Sh. No.11-26

TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR

11.2.2.2 Write Cycle

A Write Cycle will store a PTW or a SDW in the Associative Register that has a usage count of zero. The Interface Frame upon obtaining a SDW or a PTW from core memory will store it in the Descriptor Register, and will check the descriptor field for a Directed Fault. If there is no fault it will update the descriptor field and place a 1 on one of three command lines to the Associative Memory. The command line selected depends upon the type of word to be stored. The three command lines are:

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PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh.11-28 Sh. No. 11-27

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

Table 11.2.2.2 Associative Register Bit Positions vs. Input Data Lines

Associative Reg. Bits	SDW	Large PTW	Small PTW
00-17 bit 18 19-26	FD00-FD17 1 FD19-FD26	FD00-FD17 0 MB00-MB07	FD00-FD17 0 BM04-MB11
27-35	FD27-FD35	FD27-FD35	FD27-FD35
36-53	DX00-DX17	DX00-DX17	DX00-DX17

11.2.2.3 Read Cycle

The purpose of the Read Cycle is to place the information contained in the selected Associative Register on the data out lines. This can happen during a Search Cycle, during a SAZ instruction, or during a SAM instruction.

Search Cycle -- If a match occurs during any one of the three parts of a Search Cycle, a signal indicating the AR that produced the match will come true. This match signal will produce the read out signal for the corresponding AR. During a Search Cycle only bits 0-35 and 54-59 are read out.

SAZ Instruction -- The SAZ signal is ANDed with the Usage Count Equal Zero level to produce the read out signal for that AR. All 60 bits of the AR are read out.

SAM Instruction -- The SAM signal allows the Increment Counter in the Base Frame to select the AR to be read out. A count of zero will read out of AR A, a count of one will read out of AR B, etc. All 60 bits of the selected AR will be read out.

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COMPUTER EQUIPMENT DEPARTMENT
PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh.11-29 Sh. No.11-28

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

11.2.2.3 - contd

In all cases the information will remain on the data out lines as long as the conditions that produced the read out exists.

11.2.2.4 Adjust Usage Counters Cycle

Any time an Associative Register is read out of because of a match during a Search Cycle or written into, the Usage Counters must be adjusted. There is a 4-bit Usage Adder for each AR. One set of inputs to each adder is always bits 56-59 of its corresponding AR. The other set of inputs is variable. When a Read or Write Cycle occurs, the signal that reads the AR onto the data out lines will also switch the complemented outputs of bits 56-59 of the data-out lines to the variable set of inputs to all 16 four-bit adders. At this time EAUV is reset causing a carry to be added to the least significant bit of all adders. The net result is that the usage count of the selected AR is subtracted from the usage count of all ARs. Only the ARs that have a count equal to or greater than the selected AR will have a carry out of their adder.

During a Search Cycle if a match is found, the AR that produced the match will be read out onto the data out lines and a QSSF1 pulse sent to the Interface Frame. At the same time a pulse will enter a delay line to emerge 90 nanoseconds later as ASAU1. From QSSF1 to QSAU1 the adders are performing the subtraction as indicated above. QSAU1 will set EAUV and will strobe the Adjust Usage Counter bits (55) of all ARs. Any adder that produced a carry will allow QSAU1 to set the Adjust Usage Counter bit of its corresponding AR. Therefore, the selected AR and all ARs that have a higher usage count will have their Adjust Usage Counter bit set. All other ARs will have their Adjust Usage Counter bit remain reset. QSAU1 will also enter a delay line to emerge 270 nanoseconds later as QSCT1.

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PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh.11-30 Sh. No.11-29

TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR

11.2.2.4 - contd

When EAUUV set it placed all ones on the set of variable inputs to all adders and removed the carry input to the least significant bit. EAUUV set will also cause the control lines for the adder of the selected AR to set that adder up for an OR operation instead of an ADD operation. The outputs of the adders will now be all ones (a count of 15) for the selected AR and the original count minus one for all other ARs. The output of each adder is routed back to its corresponding AR's Usage Counter. QSCT1 is used to strobe the Usage Counters. However, it will strobe only those Usage Counters that have their Adjust Usage Counter bit set. At the end of the Adjust Usage Counters Cycle the selected AR will have a count of 15, all ARs that had a count higher than the original count of the selected AR will have a count one less than their original count, and all other ARs will be unchanged. QSCT1 will also reset EAUUV and set ESCR.

During a Write Cycle a QDAM1 pulse will be received when the data to be written is available. This pulse also enters the delay line to produce a QSAU1 pulse. The read out signal is developed for the selected AR (the one with a usage count of zero) to switch its usage count onto the data out lines. From this point on the Adjust Usage Counters Cycle proceeds as described above for the Search Cycle.

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GENERAL ELECTRIC COMPANY
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PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh.11-31 Sh. No.11-30

TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR

11.2.2.5 Clear Cycle

The purpose of the Clear Cycle is to initialize the Associative Register. This cycle is initiated by the Base Frame placing a "1" on the BCAM1 line. This will unconditionally reset all 16 Empty/Full bits, and it will unconditionally set the proper count in each of the Usage Counters (0000 in the Usage Counter for AR A, 0001 in the Usage Counter for AR B, 0010 in the Usage Counter for AR C, etc.). This cycle is ended when the Base Frame removes the "1" from the BCAM1 line.

11.2.2.6 Termination

The Associative Memory is started by a QSTAl pulse. This pulse will also reset EREL and ESCR in the terminate logic. When a OSCT1 pulse is generated at the end of an Adjust Usage Counters Cycle ESCR will set. When the Interface Frame has finished with the Associative Memory it issues a QREL1 pulse, which will set EREL. These two events are asynchronous and either can occur first. Using two flip-flops ensures that both units have completed their Associative Memory operation before the Associative Memory logic is initialized. ESCR set will unconditionally reset all Adjust Usage Counter bits. When both flip-flops are set they will produce a reset signal, which will reset EAUUV, ESDP, EPSL, EPSS, ESDS, and set EPSH. This initializes the control logic and the Associative Memory is now ready to start another cycle.

In the case where a paged SDW is found but not the PTW the Associative Memory will go through an Adjust Usage Counters Cycle when the SDW is read out and again when the PTW is written into an AR. The termination must wait until completion of the second Adjust Usage Counters Cycle. The first QSCT1 will set ESCR clearing the Adjust Usage Counter bits, but the QDAM1 pulse for the PTW Write Cycle will reset it. The second QSCT1 pulse will again set ESCR, and now the Associative Memory is ready to terminate.

After turn on, and at other times, it may be desirable to initialize the Associative Memory. During turn on, if the stop switch is activated, or during any fault the Control Frame will go through an Abort Cycle. During this cycle

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Spec. No. M50EB00107
Cont. on Sh. 11-32 Sh. No. 11-31

TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR

11.2.2.6-contd

a WF signal will be produced. WF will unconditionally reset EDIS and unconditionally set EREL and ESCR, which will initialize the Associative Memory control logic.

11.2.3 ASSOCIATIVE MEMORY INSTRUCTIONS

There are three instructions that deal directly with the Associative Memory: SAZ, SAM, and CAM.

11.2.3.1 SAZ (157)

When this op code is decoded the Base Frame will place a "1" on the BSAZ1 line. This level checks the usage count of all the ARs. A usage count of zero and BSAZ1 will produce two read out levels for the corresponding AR. One read-out level will switch bits 0-35 and 54-59 onto the data out lines. The other read-out level will switch bits 36-53 onto the data-out lines until the Base Frame removes the "1" from the BSAZ1 line. The Adjust Usage Counter Cycle will not be entered. This completes the SAZ instruction.

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PHOENIX, ARIZONA

Spec. No. M50EB00107
Cont. on Sh.11-33 Sh. No.11-32

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

11.2.3.2 SAM (557)

When this op code is decoded the Base Frame will place a "1" on the BSAM1 line. At the same time it will send the count in its Increment Counter minus the least significant bit. This counter will be initially set to zero and will be stepped each time a word is stored in core memory. Since each AR requires two memory words the data on the data out lines will be changed on every other memory cycle. The affects of BSAM1 and the Increment Counter on the data out lines is shown in Table 11.2.3.2. As in the SAZ instruction, two read-out levels are produced for each AR to switch all 60 bits onto the data out lines. When the last AR has been stored in core memory the Base Frame will remove the "1" from the BSAM1 line ending the SAM instruction. The Adjust Usage Counters Cycle will not be entered.

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GENERAL ELECTRIC COMPANY
COMPUTER EQUIPMENT DEPARTMENT
PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh.11-34 Sh. No.11-33

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

Table 11.2.3.2 Increment Counts vs. Register Stored for the
SAM Instruction

Increment Counter					DATA OUT LINES
To Assoc. Mem.				Not to A.M.	
EN04	EN03	EN02	EN01	EN00	
0	0	0	0	0	Associative Register A
0	0	0	0	1	Associative Register A
0	0	0	1	0	Associative Register B
0	0	0	1	1	Associative Register B
0	0	1	0	0	Associative Register C
0	0	1	0	1	Associative Register C
0	0	1	1	0	Associative Register D
.	.	.	.	.	.
.	.	.	.	.	.
.	.	.	.	.	.
1	1	1	1	1	Associative Register S

NOTE

EN00 is the 2 degree position of the Increment Counter in the
Base Frame and is not sent to the AM.

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PHOENIX, ARIZONA

Spec. No. M50EB00107
Cont. on Sh. 11-35 Sh. No. 11-34

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

11.2.3.3 CAM (532)

When this op code is decoded the Base Frame will place a "1" on the BCAM1 line. This will cause the Associative Memory to perform the Clear Cycle as described under Basic Operating Cycles.

11.2.4 MANUAL OPERATION

Test Check -- The delay lines for QP111, QP221, and QP331 are controlled by a level BCDYO. When BCDYO is at + 6 volts there will be a normal delay. If the TEST ENABLE switches are in TEST and the SF TEST CLOCK switch is in the FAST position BCDYO will go to ground and all three delay lines will be shortened.

Step -- If the TEST ENABLE switches are in TEST and the SF ENABLE switch is in the ENABLE position the operation of the Search Cycle will be interrupted. The QSTAL pulse will set EPSH and enter the delay line for QP111 as in normal operation. However, it will also set EDIS, which places an inhibit on the output of the three delay lines. The operation of the Search Cycle will proceed normally, but QP111 will not be generated. This cycle will remain in this state until the SF STEP switch is depressed. Depressing the SF STEP switch will generate a QPTM1 pulse, which samples the various states in which the Search Cycle can hang up. In this case EPSH and DEIS set will allow QPTM1 to generate a QP111 which will perform its normal functions. However, if a QP221 is required, the Search Cycle will hang up with either EPSL or EPSS set. Depressing the SF STEP switch will generate a QPTM1. EDIS set and EPSL or EPSS set will allow QPTM1 to generate a QP221, which will perform its normal functions.

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PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh.12-1 Sh. No.11-35

TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR

11.2.4 - contd

However, if a QP331 is required the Search Cycle will hang up with ESDS set. Depressing the SF STEP switch will generate a QPTM1. EDIS and ESDS set will allow QPTM1 to generate a QP331, which will perform its normal functions. If a Search Cycle is ended by a QSSF1 or QNIA1 pulse the Processor operation will continue normally until another Search Cycle is entered. To resume normal operation of the Associative Memory the SF ENABLE switch must be returned to NORMAL, and the SF STEP switch depressed. This will produce a QPTM1 pulse, which will generate the required QP pulse and reset EDIS removing the inhibit from the delay lines.

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PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh. 12-2 Sh. No. 12-1

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

12.0 OPERATIONS UNIT DETAILED OPERATION

12.1 GENERAL

This section describes the functional organization of the Operations Unit (OU) of the Processor. The basic timing cycles required and generated in the operation unit for carrying out all operation unit functions involved in instruction execution are described. The conditions for initiating each timing cycle are also described. The instructions requiring OU action are divided into groups according to the function performed and timing cycles required. The major portion of this section is devoted to describing special hardware contained in the OU.

12.1.1 FUNCTIONAL STATEMENT

The operations unit performs the primary function of arithmetic operation. The OU includes the necessary registers and hardware for performing arithmetic and related functions.

The operations unit primarily consists of the following functional elements:

- a) Two registers "O" and "C" which contain the operation codes for two successive instructions;
- b) Operation code decoding networks for generating control signals used in instruction performance;
- c) The "M" register, through which all data from memory passes on its way to the OU, and which holds the operand during multiple step arithmetic operations (multiplier during multiplication);

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COMPUTER EQUIPMENT DEPARTMENT
PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh.12-3 Sh. No.12-2

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

12.1.1 - contd

- d) The "N" and "H" registers which provide temporary operand storage during arithmetic operations;
- e) The S adder where operand addition is performed;
- f) The "A" and "Q" registers which may function separately as accumulator and quotient registers or in combination for double precision operations;
- g) The G counter which counts the iterations of iterative type operations such as multiplication;
- h) The exponent registers (ER & DR) and exponent adder (ES) used to store and add exponents in floating point operations;
- i) Index registers which are involved in various load, store, arithmetic and logical operations find their primary use in storing information for address modification, which is handled by the control unit;
- j) The indicator register, which is a collection of flip-flops indicating operation results, is also used for decision flags.
- k) The timer is a 24-bit decrementing counter which, when it has decremented to zero, indicates that the operation in process has exceeded the allowed time. A timer run out flag is set when the timer decrements to zero.

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PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh.12-4 Sh. No. 12-3

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

12.2 OU TIMING

There are 11 basic OU timing intervals or "G" cycles available for performing all of the OU functions. These minor cycles, when sequenced in a manner designated by a machine instruction, constitute a total timing sequence which permits the OU to execute its portion of an instruction.

The 11 "G" cycles are:

- GS - Setup or start cycle
- GO - General operate cycle
- GC - Single precision store, or the first half of a double precision store cycle.
- GT - Double precision store operation cycle
- GFT - Last half of a double precision store cycle
- GE - Floating point exponent comparison cycle
- GA - Mantissa alignment cycle
- GD1 - First divide operation cycle
- GD2 - Second divide operation cycle
- GN - Mantissa Normalization and/or Overshift Correction cycle
- GF - Final cycle

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PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh.12-5 Sh. No.12-4

TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR

12.2-contd

The duration of each of these 11 cycles is normally one of the three basic OU times (that is, fast, medium or slow). In special cases a cycle may have a variable wait time (T_M) terminating when a data store operation has been completed.

See paragraph 12.2.2 for a description of the OU Timing Pulse Generator.

Normally nonvariable duration cycles are:

GF Always of a slow time duration when not associated with a store instruction.

GN, GA Always of a fast time duration.

GE, GD1, GD2 Always of a slow time duration.

GFT, GT Always a T_M time duration.

All "G" Cycles are mutually exclusive except:

GS and GF which may overlap.

GC which occurs simultaneously with GS and GT for double precision stores, or simultaneously with GS and GF for single precision stores, or simultaneously with GS for all nonstore operation.

GFT which occurs simultaneously with GF for double precision stores.

For purposes of simplifying the explanations of the various "G" cycles and the OU sequences, all instructions have been categorized into 12 groups of instruction classes. When an instruction is shown having (R) or (X) in parenthesis, it is implied that a single mnemonic is used to represent a group of instructions which vary only by the register referred to. Usually, these are the A,Q,AQ, or X0-X7 registers.

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GENERAL ELECTRIC COMPANY
COMPUTER EQUIPMENT DEPARTMENT
PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh. 12-6 Sh. No. 12-5

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

12.2-contd

The instruction classes are:

1a) Normal load type instructions:

AD(R), ADL(R), AWC(R), ADE, SB(R), SBL(R), SWC(R),
NEG, NEGL, CMP(R), CNA(R), AN(R), CAN(R), OR(R),
TSX_n, RET, LD(R), LC(R), LDT, LDI, RMCM, LDE,
FLD, DFLD, SZN, EA(R), RPT, RPL, RPD, RSW, FSZN,
CMG, ADL, ER(R), RTD, LXL, RCU, RCCL.

1b) Slow store and read-alter-rewrite instructions:

AS(R), AOS, SS(R), ANS(R), ERS(R), STC2, STI,
STC1, ORS(R), STAC.

1c) Single precision fast store instructions:

ST(R), STCA, STCQ, STBQ, STBA, SMIC, STZ, STE,
FST, STT, SXL.

1d) Fast load instruction:

LREG

2a) Special fixed point compare instructions:

CMK, CWL

2b) Double precision store instructions:

STAQ, DFST, SMCM, LACL

2c) Safe store instruction:

SREG

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PHOENIX, ARIZONA

Spec. No. M50EB00107
Cont. on Sh. 12-7 Sh. No. 12-6

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

12.2 - contd.

- 3) Shifts and gray-to-binary conversion instructions:
ARS, LRS, QRS, ALR, ARL, LLR, LRL, QLR, QRL, GTB,
ALS, QLS, LLS.
- 4) Special floating point instructions:
FNO, FNEG
- 5) Normalized floating point multiply instructions:
FMP, DFMP
- 6) Fixed point multiply instructions:
MPF, MPY
- 7) Unnormalized floating point multiply instructions:
UFM, DUFM
- 8) Floating point compare instructions:
FCMP, DFCMP, FCMG, DFCMG
- 9) Normalized floating point addition and subtraction instructions:
FAD, DFAD, FSB, DFSB
- 10) Unnormalized floating point addition and subtraction instructions:
UFA, DUFA, UFS, DUFS

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PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh.12-8 Sh. No.12-7

TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR

12.2 - contd

11a) Binary coded decimal instruction:

BCD

11b) Floating point divide instructions:

FDV, DFDV

11c) Fixed point divide instructions:

DVF, DIV

11d) Inverse floating point divide instructions:

FDI, DFDI

12) Non-OU instructions:

STP, STB, LBR_n, LDCF, CAM, SAM, SBR_n, SCU, STCD,
TSS, TRA, TOV, TZE, TNZ, TMI, TPL, TRC, NOP,
CIOC, TNC, TTF, TEO, TEU, XEC, XED, DIS, DRL,
MME, ZOP, MME₂, MME₃, MME₄, ADB, LDB, SAZ, SDBR,
EAB, EAP, LDBR, TSB.

All of these groups of instructions, except 12,
cause a specific sequence of "G" cycles to be performed within the OU.

The material to follow will present the various "G"
Cycles (12.2.1), the OU Timing Pulse Generator
(12.2.2), and the OU Timing Sequences (12.2.3).

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PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh. 12-9 Sh. No.12-8

TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR

12.2.1 Basic "G" Cycles

12.2.1.1 GS-Setup or Start Cycle

Whenever a new instruction is to be processed by the OU, the first "G" cycle is always GS. GS starts on \$ SET GS when a new operation code has been strobed into the O-register, and terminates when the first general operation strobe \$ occurs. The GS cycle allows sufficient time for the operation code to be decoded and all necessary switches to be activated so that the first \$ strobe will cause the correct data to be strobed into the appropriate registers. During GS the operation code in the O-register is transferred to the C-register (on \$ START), and various indicators are reset as required.

The duration of the GS cycle may be considered to consist of two portions. The first portion is variable in time duration and is measured from \$ SET GS when a new instruction is accepted to \$DRDY when the operand for this instruction is accepted by the OU. The latter portion of GS is of medium time duration defined from \$ START (approximately \$DRDY time) to \$0.

GS is set independently of the type of instruction being processed (see 12.2.3), and may overlap the GF cycles of the preceding operation for instruction classes other than lc. To better define control variations in the generation of the GS cycle and also within the cycle, specific instruction sequences will be examined.

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PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh. 12-10 Sh. No.12-9

TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR

Case I: Startup or Operations Unit Not Busy State

This state is defined by no OU timing cycle being in process and the OU being initialized from the Startup Fault or automatically initialized via the completion of a prior instruction.

Upon receipt of a \$ ORY from the Control Unit indicating that the operation code for a new instruction is on the ZOR lines ready for processing the following sequence is initiated (refer to Fig. 12.2.1.1a).

- 1) \$ ORY sets the ORY (Operation Code Ready) flip-flop.
- 2) The ORY flip-flop being set together with the ORB (0-register Busy) flip-flop being initialized (ORB = 0) will generate a pulse (\$OR) which strobes the operation code on the ZOR lines into the 0-register.

This pulse also sets the ORB flip-flop and resets the ORY flip-flop.

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Spec. No. M50EB00107

Cont. on Sh.12-11 Sh. No. 12-10

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

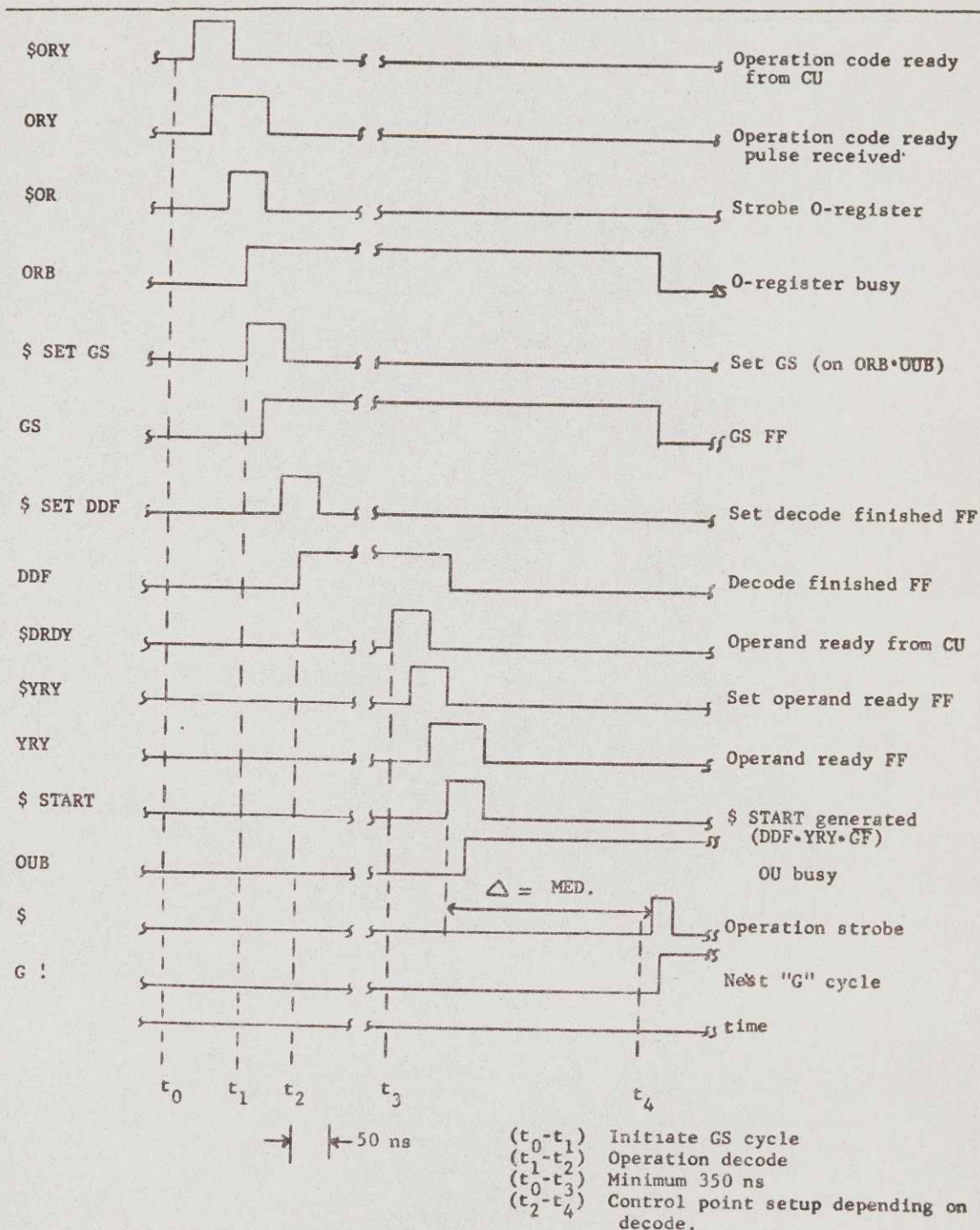


Fig. 12.2.1.1a Basic Control of the "GS" Cycle from Startup or OU Not Busy State

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PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh. 12-12 Sh. No. 12-11

TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR

12.2.1.1 - contd

- 3) The ORB flip-flop being set together with the OUB (Operations Unit Busy) flip-flop being initialized ($\overline{OUB} = 1$) will generate a \$ SET GS pulse which sets the GS cycle flip-flop, initiating the first portion of the GS interval.

The \$ SET GS pulse enters the DDF (Decode Delay) delay line exiting approximately 50 nanoseconds later. This delayed pulse (\$ SET DDF) sets the DDF flip-flop which assures that the operation code contained in the 0-register will have settled at individual control points sufficiently early with respect to the first pulse which will sample these points.

- 4) The GS flip-flop being set will gate the op code in the 0-register to the output of the V switch. This switch output is the central distribution point for operation code to all control points for OU timing intervals other than GF.
- 5) The OU is notified by the Control Unit that the operand for the instruction is ready on the ZDI lines by \$DRDY (Data Ready). This pulse will occur approximately 1 microsecond after \$ORY and 350 nanoseconds after \$ORY if the operand is a direct (no memory cycle required.)

This pulse results in the strobing of the operand on the ZDI lines into the M-register. \$DRDY also generates \$YRY which sets the YRY (Operand Ready) flip-flop signifying that the operand is in the M-register ready for processing.

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Spec. No. M50EB00107

Cont. on Sh.12-13 Sh. No.12-12

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROROTYPE PROCESSOR

12.2.1.1 - contd

- 6) The operation code being settled ($DDF = 1$), the operand being ready ($YRY = 1$) and the OU not in the process of finishing a prior instruction ($\overline{GF} = 1$) results in the generation of \$ START which terminates the first portion of GS and initiates the effective OU portion.

\$ START also sets the OUB flip-flop and strobes the contents of the O-register into the C-register, the secondary operation code register.

\$ START enters the OU pulse generator delay network (paragraph 12.2.2). It will exit in approximately 320 nanoseconds for all instructions as $\$0$, the first arithmetic pulse for the operation.

- 7) $\$0$ resets the GS cycle and sets the next timing interval required by the operation.

GS resetting gates the C-register into the V switch.

$\$0$ resets the ORB flip-flop freeing the O-register to receive the operation code for the next instruction.

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PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh. 12-14 Sh. No.12-13

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

12.2.1.1 - contd

CASE II: Overlapped Pair of Nonstore Instructions
(Fig. 12.2.1.1b)

To optimize execution time, the Control Unit normally pulls a pair of instructions when executing an instruction fetch. To take advantage of the availability of this pair, the Operations Unit may start processing the odd (second) instruction prior to completion of the even (first) instruction.

\$ SET GS and \$ START control for the even instruction is as explained in Case I. The following illustrates GS control for the odd instruction:

- 1) When \$YRY is generated for the even instruction, it is returned to the Control Unit where upon receipt of this pulse the \$ORY pulse for the odd instruction is generated and transmitted to the OU together with the operation code for the instruction.
- 2) \$ORY sets the ORY flip-flop which was reset on the \$ OR of the even instruction.
- 3) Upon completion of the GS cycle for the even instruction the ORB (O-register Busy) flip-flop is reset. Thus, as in Case I, $(ORB)(ORY) = 1$ will generate a \$ OR pulse which strobes the new operation code on the ZOR lines into the O-register.

\$OR sets the ORB flip-flop and resets the ORY flip-flop.

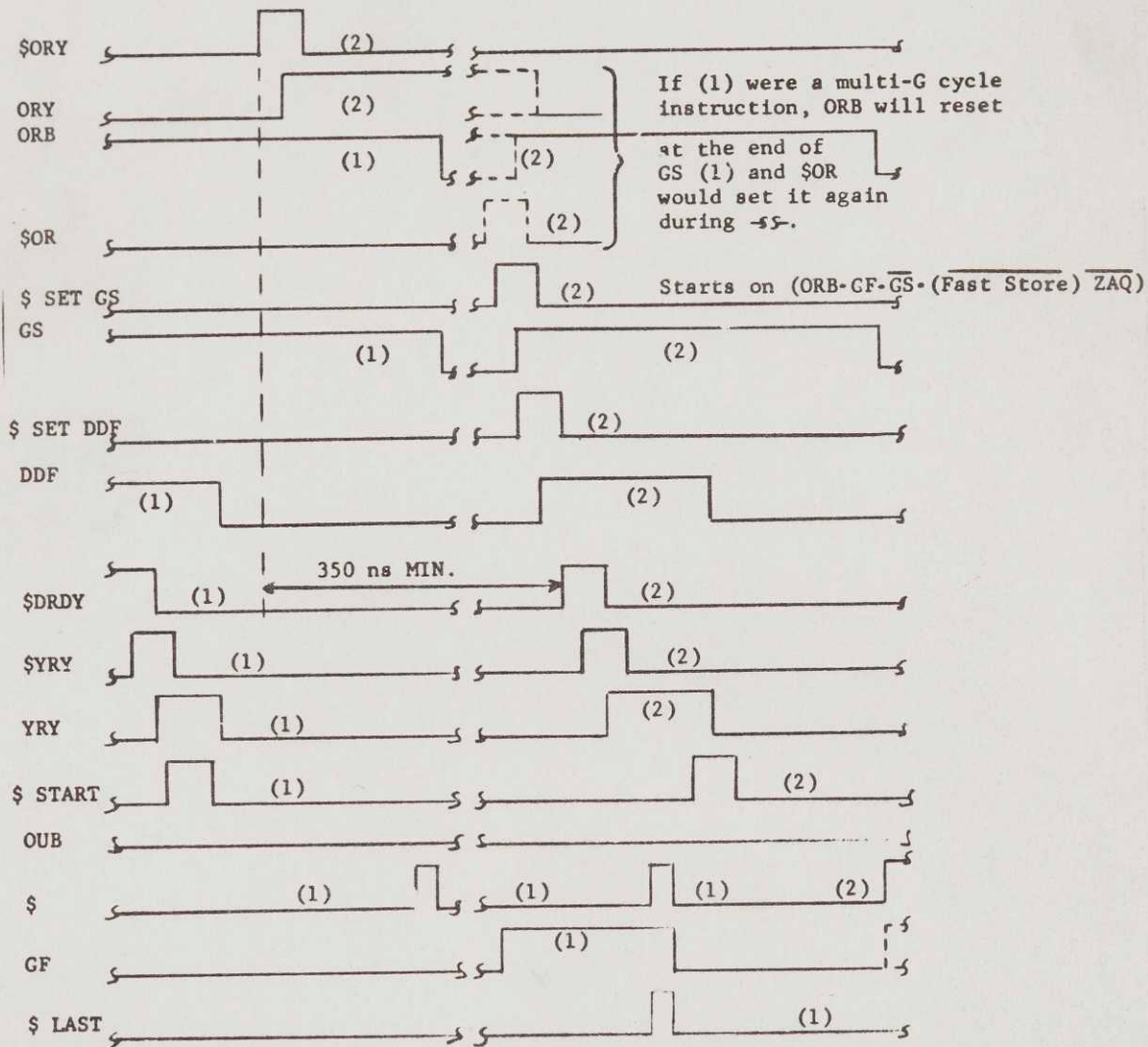
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PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh. 12-15 Sh. No. 12-14

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR



- NOTES: 1. (1) and (2) refer to overlapped instructions 1 and 2.
2. -- interval will be zero time for a GS-GF instruction, but will be variable for multi-G cycle instructions.
3. \$YRY (1) initiates \$ORY (2).
4. Under certain conditions \$ LAST may be delayed.

Fig. 12.2.1.1b Basic Control of the "GS" Cycle for Nonstore Instructions with Instruction Overlap (Single Precision)

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Spec. No. M50EB00107

Cont. on Sh.12-16 Sh. No.12-15

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

12.2.1.1 - contd

- 4) The condition which generated \$ SET GS for the even instruction $[(ORB) (\overline{OUB})]$ is inactive since the OUB flip-flop is still set and will remain set until completion of the even instruction. This term, then, will generate a \$ SET GS only for Case I conditions (startup or no overlap).

\$ SET GS for the odd instruction is generated only after the final (GF) cycle of the even instruction has been entered.

That is, $\$ SET GS = (ORB) (CF) (\overline{GS})$

- 5) \$ SET GS enters the DDF delay line exiting approximately 50 nanoseconds later. This delayed pulse (\$ SET DDF) sets the DDF flip-flop.
- 6) When GS sets, the contents of the O-register (containing the op code for the odd instruction) is gated to the output of the V switch. Control points affected by the odd instruction during GS are in the process of settling prior to completion of the even instruction. Decode for GF cycles is developed from the C-register; thus, there is no conflict resulting from the OU having two instructions active concurrently.
- 7) Approximately 300 nanoseconds after GS for the odd instruction has set, the final (GF) cycle of the even instruction will reset designating the completion of the instruction execution. The OUB flip-flop will not reset since $(GF) (\overline{GS}) = 0$.

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PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh. 12-17 Sh. No. 12-16

TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR

12.2.1.1 - contd

- 8) Upon receipt of \$DRDY (which normally occurs after completion of the previous instruction but can, in the case of a direct operand for the odd instruction or a multi-cycled even instruction, occur prior to termination of the even instruction) the operand for the odd instruction is strobed from the ZDI lines into the M-register. \$DRDY generates \$YRY which sets the YRY flip-flop indicating that the operand is ready for processing.
- 9) The operation code being settled ($DDF = 1$), the operand being ready ($YRY = 1$), and the even instruction being completed ($\overline{GF} = 1$), results in the generation of \$ START for the odd instruction.
- 10) \$ START strobes the contents of the 0-register into the C-register. \$ START enters the OU pulse generator delay network (paragraph 12.2.2). It will exit in approximately 320 nanoseconds for all instructions as \$₀, the first arithmetic pulse for the operation.
- 11) \$₀ resets the GS cycle and sets the next timing interval required by the operation.

GS resetting gates the C-register into the V switch.

\$₀ resets the ORB flip-flop freeing the 0-register to receive the operation code for the next instruction.

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PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh.12-18 Sh. No.12-17

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

12.2.1.2 GO - General Operate Cycle

The GO cycle is the main operate cycle for instructions which cannot be completed within a GS→GF sequence. The GO cycle is used when multiple arithmetic operations are required in order to execute the instruction.

For instruction classes 9 and 10, a single GO cycle is used to add the mantissas of the operands contained in the N-and A/Q-registers.

For instruction classes 3,5,6,7, and 11, multiple GO cycles are performed as explicitly implied by each instruction within these classes. Class 3 instructions require data shifting in which the contents of the N-register are shifted under control of the G counter. Class 5,6, and 7 instructions are multiply instructions which are performed under control of the G counter. To optimize the execution of multiply instructions a unique cycle, GOM (GO multiply) is utilized. GOM is generated in the RF frame where it is to be used which simplifies and speeds up the distribution of the function (GO) (MPLY). Class 11 instructions are Divide instructions which are performed under control of the G counter.

Instruction class 2a uses a single GO cycle for its execution. A logical AND is executed during the GO cycle of CMK. CWL uses a single GO cycle for an upper/lower limit comparison.

In classes 5,6,7, and 11, the multiple GO cycles are terminated with a final slow speed GO during which indicators are manipulated.

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PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh.12-19 Sh. No.12-18

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

12.2.1.3 GC - Single Precision Store, or First Half of a Double Precision Store Cycle

GC is a special cycle which is operative during a single precision store (class 1c) or during the first half of a double precision store (class 2b). This is the only cycle whose duration is coincident with two other cycles. That is, $GC = GS + GF$ for a single precision store or $GC = GS + GT$ for a double precision store. For all other operations, $GC = GS$.

The GC cycle controls the gating of data registers which are to be stored into the Data Out Buffer although other timing cycles are moving during these instructions. Logic transients between these cycles will not be felt in the Data Out Buffer.

12.2.1.4 GT - Double Precision Store Operation Cycle

GT is operational for instruction classes 2b or 2c only and is set for the duration following the GS cycle of a double precision store operation until completion of the first half store of the operation. The duration of GT is T_M time dependent and always occurs between a GS and a GFT cycle. The GT cycle is terminated by a $\$DS$ from the Interface Frame.

12.2.1.5 GFT - Last Half of a Double Precision Store Cycle

GFT is a special cycle used only during the second half of a double precision store instruction (class 2b or 2c). GFT is always T_M time dependent and always follows a GT cycle.

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Spec. No. M50EB00107

Cont. on Sh.12-20 Sh. No.12-19

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

12.2.1.6 GE - Floating Point Exponent Comparison Cycle

The GE cycle is used during the execution of instruction classes 8,9, or 10. The GE cycle is always a slow interval cycle and always follows GS cycle. During this cycle, two exponents are compared. The result of this comparison determines which exponent will be placed in the E-register, and which mantissas will be placed in the H- and N-registers. In addition, this comparison determines which mantissa, if either, requires alignment and how much, and whether the next cycle should be a GA, GO, or GF.

12.2.1.7 GA - Mantissa Alignment Cycle

The GA cycle is a fast interval cycle and always follows a GE cycle for instruction classes 8,9, and 10 if during that GE cycle, the exponent comparison had an absolute value of greater than zero and less than 72. During the GA cycle the smaller mantissa contained in the N-register will be shifted right 16, 4, or 1 bit(s) as determined by the G counter. If the G counter calls for more shifts GA will be repeated until LSA signals the last shift.

12.2.1.8 GD1 - First Divide Operation Cycle

A GD1 cycle will always follow a GS cycle of a class 11 instruction and will be a slow interval cycle.

For instruction classes 11a, 11b, and 11c the GD1 cycle defines the interval during which the divisor in M is transferred to H. The divisor is complemented if necessary to ensure a negative divisor. The N-register is cleared to zero and if the signs of the original dividend and divisor are different the Quotient Sign flip-flop (QSF) is set.

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PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh.12-21 Sh. No.12-20

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

12.2.1.8 - contd

For instruction class 11d the divisor in AQ is examined to determine if it is equal to zero. If divisor is zero, the Divide Check flip-flop (DVCK) will set and the OU will abort the operation. The dividend mantissa in M is transferred to H. The dividend exponent in M64-71 will be transferred to D. The N-register is cleared to zero and if the signs of the two original mantissas were different QSF will be set.

12.2.1.9 GD2 - Second Divide Operation Cycle

A GD2 cycle always follows a GD1 cycle and is a slow interval cycle.

For instruction classes 11a, 11b, and 11c the divisor in H is examined to see if it is equal to zero. If so, the Divide Check flip-flop (DVCK) is set and the OU will abort the operation. The positive dividend in AQ is transferred to N and the G counter is set for the appropriate number of GO cycles to execute the instruction.

For instruction class 11d the positive dividend in H is transferred to N, the negative divisor in AQ is transferred to H, the exponent registers D and E are exchanged, and the appropriate number of GO cycles to execute the instruction is loaded into the G counter.

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GENERAL ELECTRIC COMPANY
COMPUTER EQUIPMENT DEPARTMENT
PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh.12-22 Sh. No. 12-21

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

12.2.1.10 GN - Mantissa Normalization and/or Overshift
Correction Cycle

Although normalization is the primary function performed during GN, this cycle also may be entered for:

- a) Compensating for overshifts of data when executing instructions in class 3. The compensations may be a right or left shift of one.
- b) Backing out of an overflow condition which may have occurred while executing an instruction in classes 4, 5, 7, 9, or 10. This is accomplished with an arithmetic right shift of one with a corresponding increase in the exponent.

For instructions in classes 4,5,7,9, or 10 which enter GN for normalization, the mantissa to be normalized is in the N-register and is shifted left by 16,4, or 1 bit(s) at a time. The GN cycle will be repeated until normalization is complete. The G counter accumulates the number of normalization shifts.

12.2.1.11 GF - Final Cycle

GF is always the last "G" cycle to be performed within the OU when executing an instruction if no fault condition occurs earlier in the instruction execution. All final arithmetic operation, data transfers, indicator settings, etc. are performed during GF. This cycle is a slow interval for all nonstore operation, and a T_M interval for store operations.

COMPANY CONFIDENTIAL

GENERAL ELECTRIC COMPANY
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PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh.12-23 Sh. No.12-22

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

12.2.2 Timing Pulse Generator

The purpose of the Timing Pulse Generator is to produce and distribute to the OU pulses (\$) which are used to strobe all arithmetic and auxiliary registers in the OU. The \$ strobe is a 50-nanosecond wide pulse, and the interval or period from the end of one strobe pulse to the end of the next strobe pulse is dependent upon the instruction which is being processed and the "G" cycle which is active at that particular time. The four intervals between \$ strobes which are possible are:

- 1) Fast, which is approximately 200 nanoseconds.
- 2) Medium, which is approximately 320 nanoseconds.
- 3) Slow, which is approximately 400 nanoseconds.
- 4) T_M , which is memory speed dependent and is used to terminate all store data operations.

The three time intervals fast, medium, and slow have been selected in such a manner that any operation to be performed within the OU can be completed during one of these time periods. Below is an example of how one "G" cycle (GO) may be required by the operation being performed to be a fast, medium, or slow cycle.

Example:

A high speed GO would apply to shift cycles associated with shift operations. A medium speed GO would apply to iterative add cycles for multiply or divide. A slow speed GO would apply to operations which require setting of indicators at the end of the GO cycle as a result of arithmetic functions performed during the cycle.

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Spec. No. M50EB00107

Cont. on Sh. 12-24 Sh. No. 12-23

TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR

12.2.2 - contd

The three nonmemory dependent time cycles are all obtained or developed by delay lines and logic arrangements. (See Fig. 12.2.2.) There are three delay lines which are cascaded via logic nets. When some condition occurs to initiate a timing cycle, a pulse starts down the first delay element. While this delay is still active, a decision is made as to whether this should be a fast or not a fast cycle. If the decision is for a fast cycle, the output of delay line is routed to the general \$ distribution network and is inhibited from entering delay line 2; however, if the decision had been for a medium or slow cycle, then a pulse would have entered delay line 2 and would have been inhibited from entering the distribution network. After delay 2 has been propagated, and if this is to be a medium cycle, then the pulse is distributed to the system and inhibited from entering delay 3; however, if the cycle is to be slow then a pulse enters delay 3 and is inhibited from entering the \$ distribution network. After delay 3 has been propagated, a slow cycle \$ strobe is unconditionally distributed to the processor.

The first pulse to enter the delay chain for an instruction is \$ START which is derived from the fact that a new operation designator has been set up in the OU, its operand is ready, and GF of a prior instruction is not active. The first delay path established will be a medium (\$ START \$₀). Once the first \$ strobe has been generated it becomes the input to delay line 1 to produce a subsequent \$ strobe. Exceptions to the \$ strobe being recirculated to produce later \$ strobes are:

- a) When store data operations are being performed, the \$ strobe which starts the actual store operation may enter the delay line network but would not be enabled on the output so as to cause a \$ strobe to be distributed to the system. For store operations, the next \$ will be generated from the \$DS line and completes the store operation. This is the T_M period mentioned earlier.

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Spec. No. M50EB00107

Cont. on Sh.12-25 Sh. No.12-24

TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR

12.2.2 - contd

- b) When the \$ strobe occurs which is the last \$ for the execution of an instruction (that is, the one which resets GF). GF being set inhibits this pulse from again entering the delay line network. This pulse generates \$ LAST. \$ LAST notifies the CU that an instruction execution has been completed.
- c) When the OU is in Step mode. The Step mode flip-flop prevents any pulse from leaving the first delay line. In this mode each \$ pulse is generated as a function of the STEP switch.

Abbreviated equations describing the pulse generator are listed in terms of the "G" cycles and the OU instruction classes.

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Cont. on Sh.12-26 Sh. No.12-25

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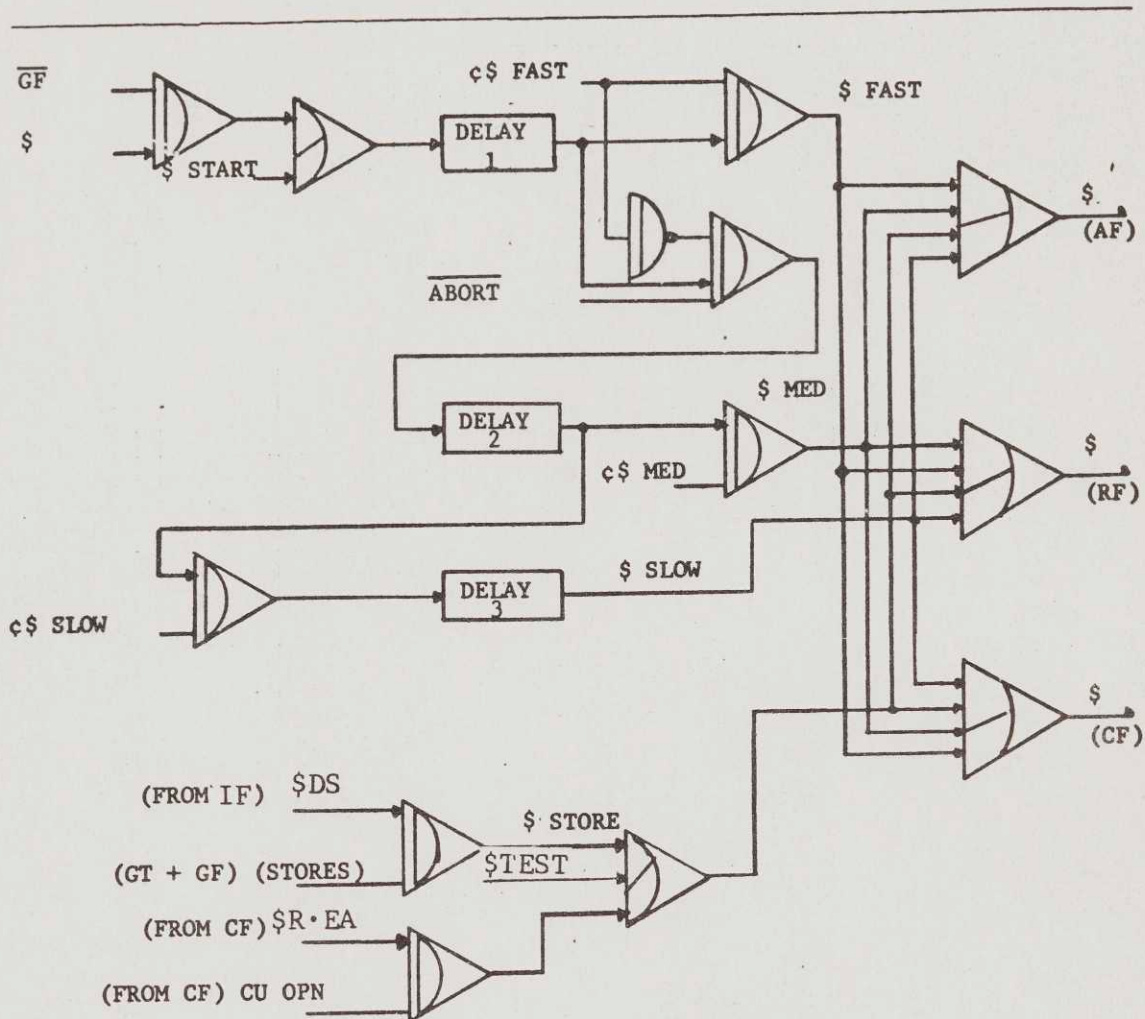


Fig. 12.2.2 OU Pulse Generator

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Spec. No. M50EB00107

Cont. on Sh. 12-27 Sh. No. 12-26

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

12.2.2 - contd

Equations defining the enabling terms on the output gates of the fast, medium, and slow delay lines are:

$$\phi \$ \text{ FAST} = (\text{GO}) (3) + \text{GN} + \text{GA}$$

$$\phi \$ \text{ MED} = (\text{GS}) + (\text{GO}) [4 + (\text{GR}=1) (5 + 6 + 7 + 11)]$$

$$\begin{aligned} \phi \$ \text{ SLOW} = & (\text{GE}) + (\text{GD1}) + (\text{GD2}) + (\text{GF}) \\ & (1b + 1c + 2b + 2c) + (\text{GO}) \\ & [2a + 9 + 10 + (\text{GR} = 1) (5 + 6 + 7 + 11)] + \\ & \text{GO (CMFF)} \end{aligned}$$

Equations defining the \$ output are:

$$\$ \text{ FAST} = [(\$) (\overline{\text{GF}}) + \$ \text{ START}] [\phi \$ \text{ FAST}] [\Delta \text{ FAST}]$$

$$\begin{aligned} \$ \text{ MED} = & [\{ (\$) (\overline{\text{GF}}) + \$ \text{ START} \} (\overline{\phi \$ \text{ FAST}}) \\ & (\Delta \text{ FAST})] (\phi \$ \text{ MED}) (\Delta \text{ MED}) \end{aligned}$$

$$\begin{aligned} \$ \text{ SLOW} = & [\{ (\$) (\overline{\text{GF}}) + \$ \text{ START} \} (\overline{\phi \$ \text{ FAST}}) \\ & (\Delta \text{ FAST})] (\Delta \text{ MED}) (\phi \$ \text{ SLOW}) (\Delta \text{ SLOW}) \end{aligned}$$

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Spec. No. M50EB00107

Cont. on Sh. 12-28 Sh. No. 12-27

TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR

12.2.2 - contd

$\$ \text{ STORE} = (\$ \text{DS}) [\text{GT} + \text{GF} (1\text{b} + 1\text{c} + 2\text{b} + 2\text{c})]$

$\$ \text{ SPECIAL}^* = \$ \text{R} \cdot \text{EA}$

The final output $\$$ is:

$\$ = \$ \text{ FAST} + \$ \text{ MED} + \$ \text{ SLOW} + \$ \text{ STORE} + \$ \text{R} \cdot \text{EA} + \$ \text{ TEST}$

12.2.3 Timing Sequences

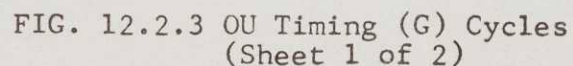
This paragraph defines the OU timing sequences which are used in the execution of instructions. This diagramatical representation reflects the various "G" cycles used and their time durations. The sequences shown are those which are necessary to execute all classes of instructions described in paragraph 12.2.

A detailed discussion as to what occurs during each sequence will be presented in paragraph 12.3.

— *Resets OFL, EOF, and EUF Indicators on TOV, TEO,
 or TEU.

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Cont. on Sh.12-29 Sh. No.12-28

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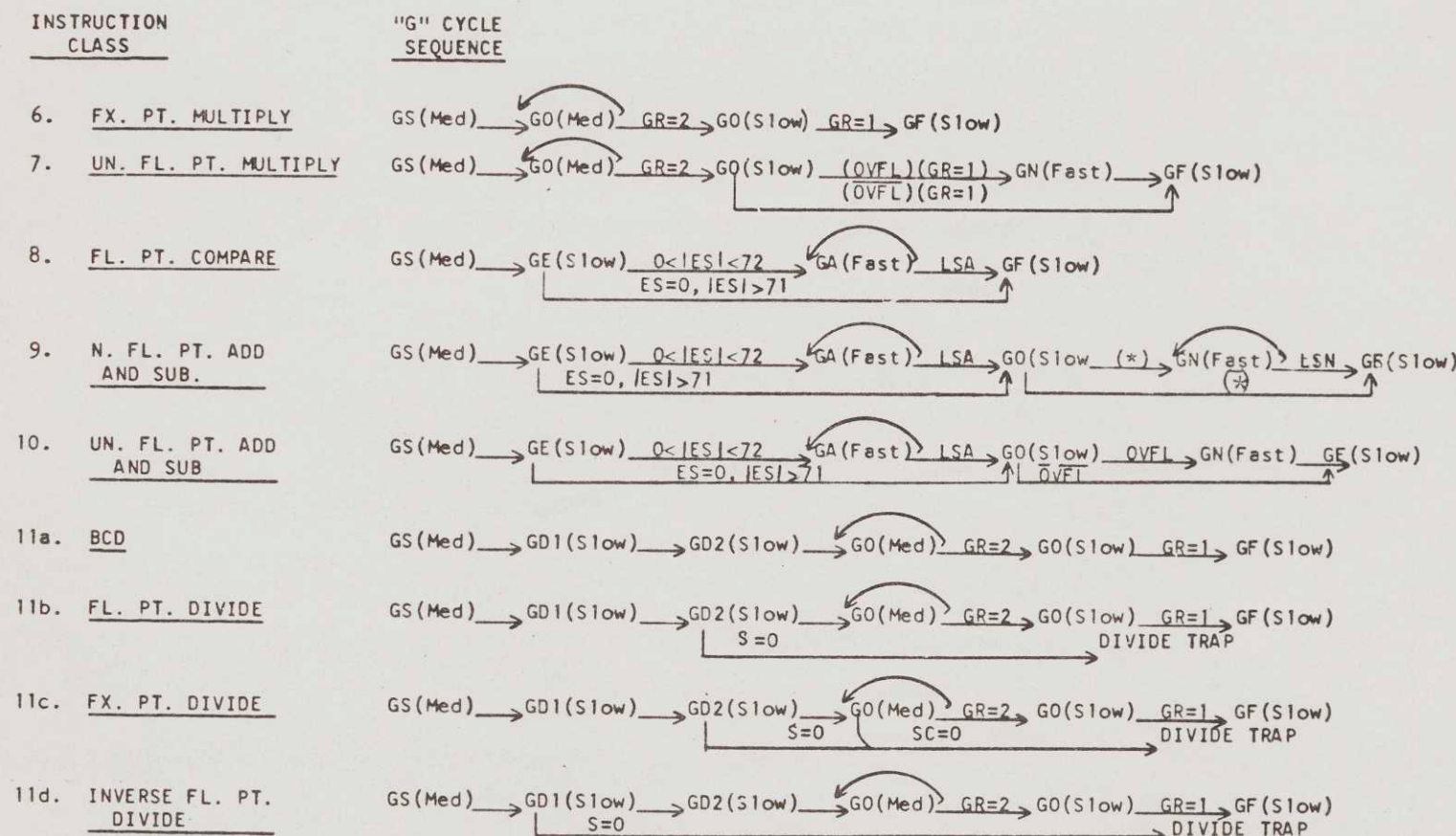
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Spec. No. M50EB00107

Cont. on Sh. 12-30 Sh. No. 12-29

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR



* normalization required

FIG. 12.2.3 OU Timing (G) Cycles
(Sheet 2 of 2)

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Spec. No. M50EB00107

Cont. on Sh.12-31 Sh. No.12-30

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

12.3 INSTRUCTION DESCRIPTION BY GROUP

For purposes of describing the basic "G" sequences it was convenient to place all those instructions into a class which required a specific sequence for their execution. Generally, these sequences were independent of whether the instruction was fixed point or floating point, or single precision or double precision. However, for detailed explanations of instructions, (that is, data paths, control points, and timing differences between instruction within a class) the instructions are further subdivided to reflect fixed point or floating point and single precision or double precision. This subdivision is called a group.

12.3.1 FIXED POINT ADD GROUP

This group of instructions, which number approximately 174, constitute the majority of instructions executed in the OU. The Add Group includes a variety of fixed point instructions which require only two "G" cycles. The group consists of additions, subtractions, logicals, loads, and compares. The major data paths and control points for these instructions are shown in Fig. 12.3.1. In the execution of these instructions, adder registers H and N are loaded from some source, the S-adder performs an operation determined by the adder control flip-flops, K₁, K₂, K₃, and K₇₂, and the results are strobed to some location and/or examined for the purpose of setting Arithmetic Indicators. (For detailed description of the S-adder operation see 12.10.)

To illustrate the control used in the execution of these instructions, several instructions will be explained in detail. For the detailed control of all instructions in this group, refer to the OU Specification Charts 43D139962, page 2, 3, 5, and 11.

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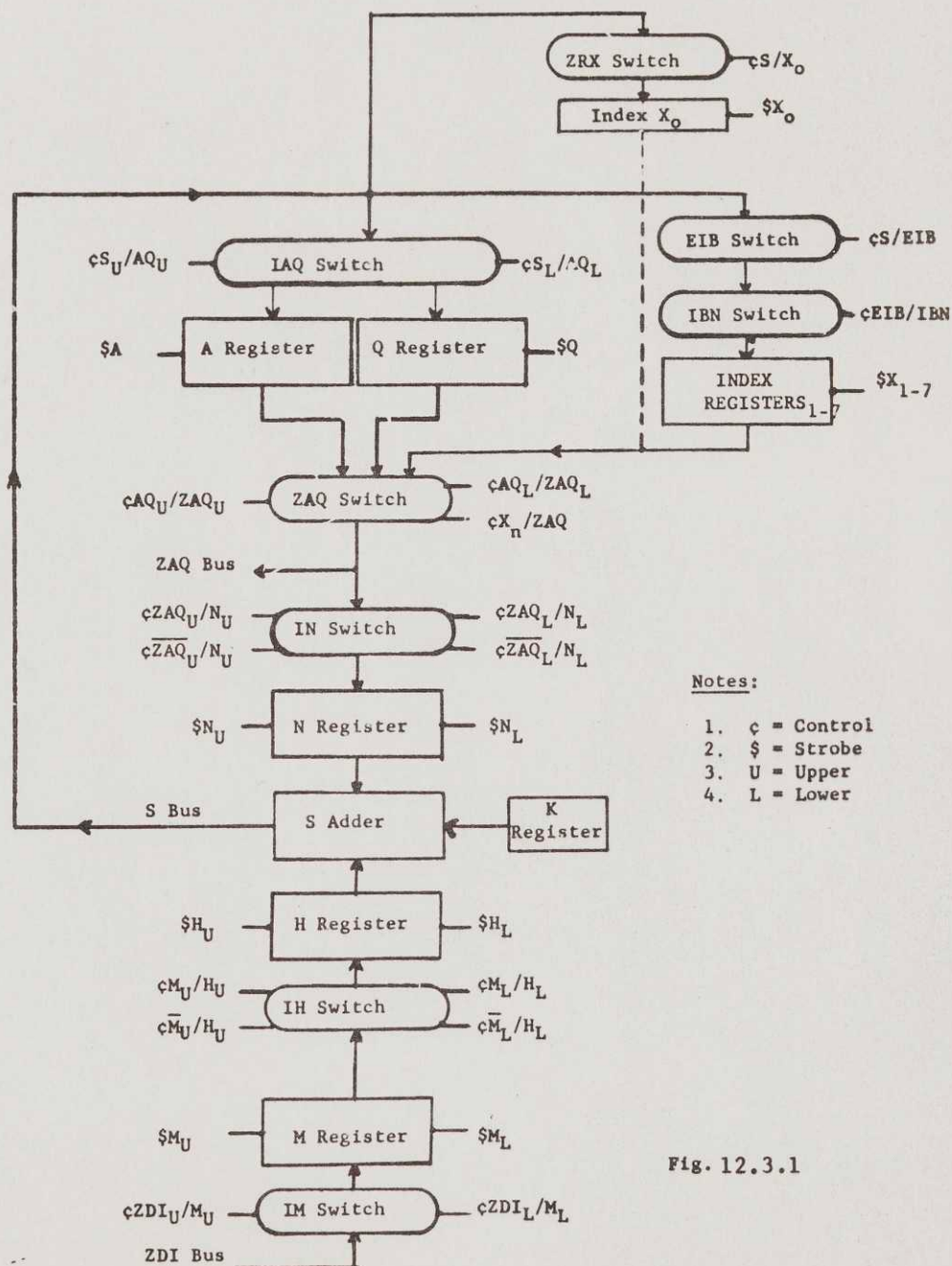
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Spec. No. M50EB00107

Cont. on Sh.12-32 Sh. No.12-31

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

Major Data Paths and Control Points for the
Fixed Point Add Type Instructions (OU)



Notes:

1. ϕ = Control
2. $\$$ = Strobe
3. U = Upper
4. L = Lower

Fig. 12.3.1

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Spec. No. M50EB00107

Cont. on Sh.12-33 Sh. No.12-32

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

12.3.1 - contd

In the explanation of all the example instructions, the following conditions will be assumed:

- 1) The instruction has been strobed in the 0-register.
- 2) The GS cycle flip-flop has been set.
- 3) The DDF flip-flop has been set indicating the operation decode has settled.

NOTE: Reference to Fig. 12.3.1 and the partial timing diagram at the end of each example will aid in the understanding of the instruction execution and implementation.

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Spec. No. M50EB00107

Cont. on Sh.12-34 Sh. No.12-33

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

12.3.1.1 Single Precision

The instructions comprising the single precision portion of the Add Group are:

ADLQ, ADLA, ADLX_n, AWCQ, AWCA, ADQ, ADA, ADX_n, CMPQ,
CMPA, CMPX_n, SBLQ, SBLA, SBLX_n, SWCQ, SWCA, SBQ, SBA,
SBX_n, CANQ, CANA, CANX_n, LCQ, LCA, LCX_n, ANQ, ANA, ANX_n,
CNAQ, CNA, CNAX_n, LDQ, LDA, SZN, LDX_n, ORQ, ORA
ORX_n, RET, EAQ, LDT, EAA, LDI, EAX_n, ERQ, ERA, ERX_n,
TSX_n, LXL_n, NEG, CMG, ADL, RCU, RTD.

Example 1: Load (LDA)

During this instruction the contents of a memory location Y are loaded into the A-register via the S-adder. The presence of the LDA instruction code on the ZOR lines together with the Double Precision flip-flop (DPFF) reset, the Byte Control flip-flop (BCFF) reset, and the Multiply flip-flop (DIC) reset, enable the IM switch. The control points $\phi ZDI_{0-17}/M_{0-17}$, $\phi ZDI_{18-27}/M_{18-27}$, and $\phi ZDI_{28-35}/M_{28-35}$ are enabled presenting the operand lines (ZDI bus) to the M-register inputs. When the operand ready strobe (\$DRDY) is received from the CU, the DPFF not being set allows the M-register strobe (\$M₀₋₇₁) to be generated and strobe the LDA operand into the M-register. The \$DRDY pulse is turned around as \$YRY and returned to the CU to signal that a new instruction may be prepared. \$YRY sets the operand ready flip-flop (YRY) in the OU. When YRY is set, the conditions exist to allow \$START to be generated by a last of three pulse detectors. (\$START) sets the OU Busy flip-flop (OUB), resets YRY and DDF, and transfers the operation code from the O-register to the C-register. It also enters the timing pulse generator delay line network.

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Spec. No. M50EB00107

Cont. on Sh.12-35 Sh. No.12-34

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

12.3.1.1 - contd

When the \$ START pulse propagates the medium delay elements, the operate strobe \$ occurs. This allows the following events:

- 1) \$H will strobe the LDA operand into the H-register from the M-register.
- 2) \$N will strobe all zeros into the N-register since the IN switch is not enabled.
- 3) The Zero and Sign Indicators reset.
- 4) ORB to reset, indicating that the O-register is free to receive the operation designator for the next instructor.
- 5) GS to reset and GF to set.

The \$ pulse will re-enter the timing pulse generator delay line network. GF being set will delay the pulse 400 nanoseconds before another \$ pulse is generated.

During this 400 nanoseconds the contents of H and N are added together in the S-adder. The add function takes place because none of the K flip-flops are set. The addition of H (operand) and N (zeros) produces the operand at the S-adder outputs.

When GF set, the $\phi S_{0-35}/AQ_{0-35}$ gate on the IAQ switch became enabled, making the S-adder outputs available on the inputs to the A-register. On the occurrence of the next \$ strobe, $\$AQ_{0-35}$ is generated and the adder output is strobed into the A-register. At this time the contents of the memory location Y are loaded into the A-register. This \$ strobe resets GF, turns on the Zero Indicator if the contents of A = 0, turns on the Sign Indicator if bit position 0 of A = 1, resets OUB if no other instruction has been initiated, and generates \$ LAST. \$ LAST is sent to the CU to indicate completion of the LDA instruction.

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 Cont. on Sh.12-36 Sh. No.12-35

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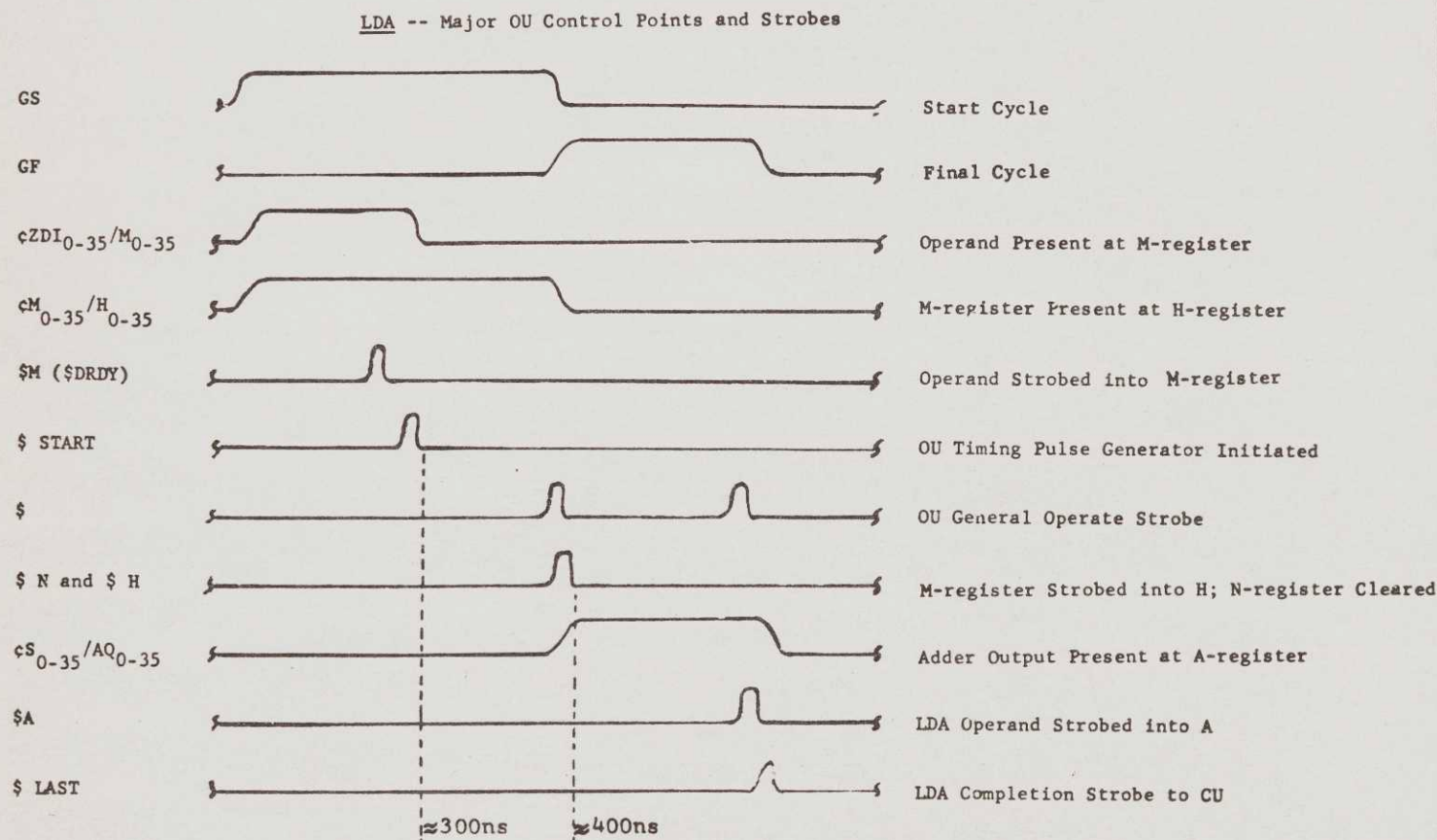


FIG. 12.3.1.1 LDA Instruction, Timing Diagram

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Spec. No. M50EB00107

Cont. on Sh.12-37 Sh. No. 12-36

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

12.3.1.1 - contd

Example 2: Add (ADX_n)

During this instruction the contents of bits 0-17 of a memory location Y are added to the contents of an index register X_n and the results are placed in X_n .

The presence of the ADX_n instruction code on the ZOR lines together with the DPFF reset, BCFF reset, and DIC reset enable the IM switch. The control point $\phi ZDI_{0-17}/M_{0-17}$ is enabled to allow the operand lines (ZDI bus) to be present at the M-register inputs. When the operand ready strobe ($\$DRDY$) is received from the CU, DPFF not being set allows $\$M_{0-71}$ to be generated and strobe the ADX_n operand into the M-register. The $\$DRDY$ pulse is turned around as $\$YRY$ and returned to the CU to signal that a new instruction may be prepared. $\$YRY$ sets the operand ready flip-flop (YRY) in the OU.

When YRY is set, the conditions exist to allow $\$START$ to be generated and enter the OU Timing Pulse Generator to later produce the operate strobe $\$$. $\$START$ also sets the OU busy flip-flop (OUB), resets YRY and DDF, and transfers the operation code from the O-register to the C-register.

GS

The IH switch is enabled by $\phi M_{0-35}/H_{0-35}$, the ZAQ switch by $\phi X_n/ZAQ_{0-17}$, and the IN switch by $\phi ZAQ_{0-35}/N_{0-35}$. These enabled switches allow the operands from memory and the index register to be present at the inputs to the H- and N-register.

When the $\$START$ pulse propagates the medium delay elements, the operate strobe $\$$ occurs. This pulse:

- 1) Strokes ($\$H$) the memory operand from the M- to the H-register.

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Spec. No. M50EB00107

Cont. on Sh.12-38 Sh. No. 12-37

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

12.3.1.1 - contd

- 2) Strobes (\$N) the present index register contents into the N-register.
- 3) Resets the Zero and Sign Indicators.
- 4) Resets the ORB flip-flop.
- 5) Resets the GS cycle and sets GF.
- 6) Re-enters the Timing Pulse Generator delay line network to produce another \$ strobe in approximately 400 nanoseconds.

During this 400-nanosecond time the contents of the H- and N-registers are added in the S-adder. The Adder Control Register (K_1, K_2, K_3, K_7) = 0, 0, 0, 0 defines an add function which will be performed during the GF cycle.

GF

When GF set, control points on the inputs to all index registers were turned on. These control points are $\phi S_{0-17}/ZRX_{0-17}$ for control of data into X_0 , and $\phi S_{0-17}/EIB_{0-17}$ and $\phi EIB_{0-17}/IBN_{0-17}$ for control of data into X_{1-7} . On the occurrence of the next \$ strobe, $\$X_n$ is generated and the adder output $[C(Y) + C(X_n)]$ is strobed into the index register specified by the instruction. The \$ strobe also:

- 1) Resets GF.
- 2) Resets OUB if no other instruction has been initiated.
- 3) Sets the Sign Indicator if bit zero of the sum was negative ($S_0 = 1$).

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Spec. No. M50EB00107

Cont. on Sh.12-39 Sh. No. 12-38

TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR

12.3.1.1 - contd

- 4) Sets the Zero Indicator if the sum was zero ($S = 0$).
- 5) Sets the Carry Indicator if a carry out of bit zero is generated during the add, ($SC_0 = 1$) or resets it if no carry ($SC_0 = 0$).
- 6) Sets the Overflow Indicator if the range of X_n is exceeded, ($OFL = 1$).
- 7) Generates \$ LAST, which is sent to the CU to indicate completion of the ADX_n instruction.

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Cont. on Sh.12-40 Sh. No.12-39

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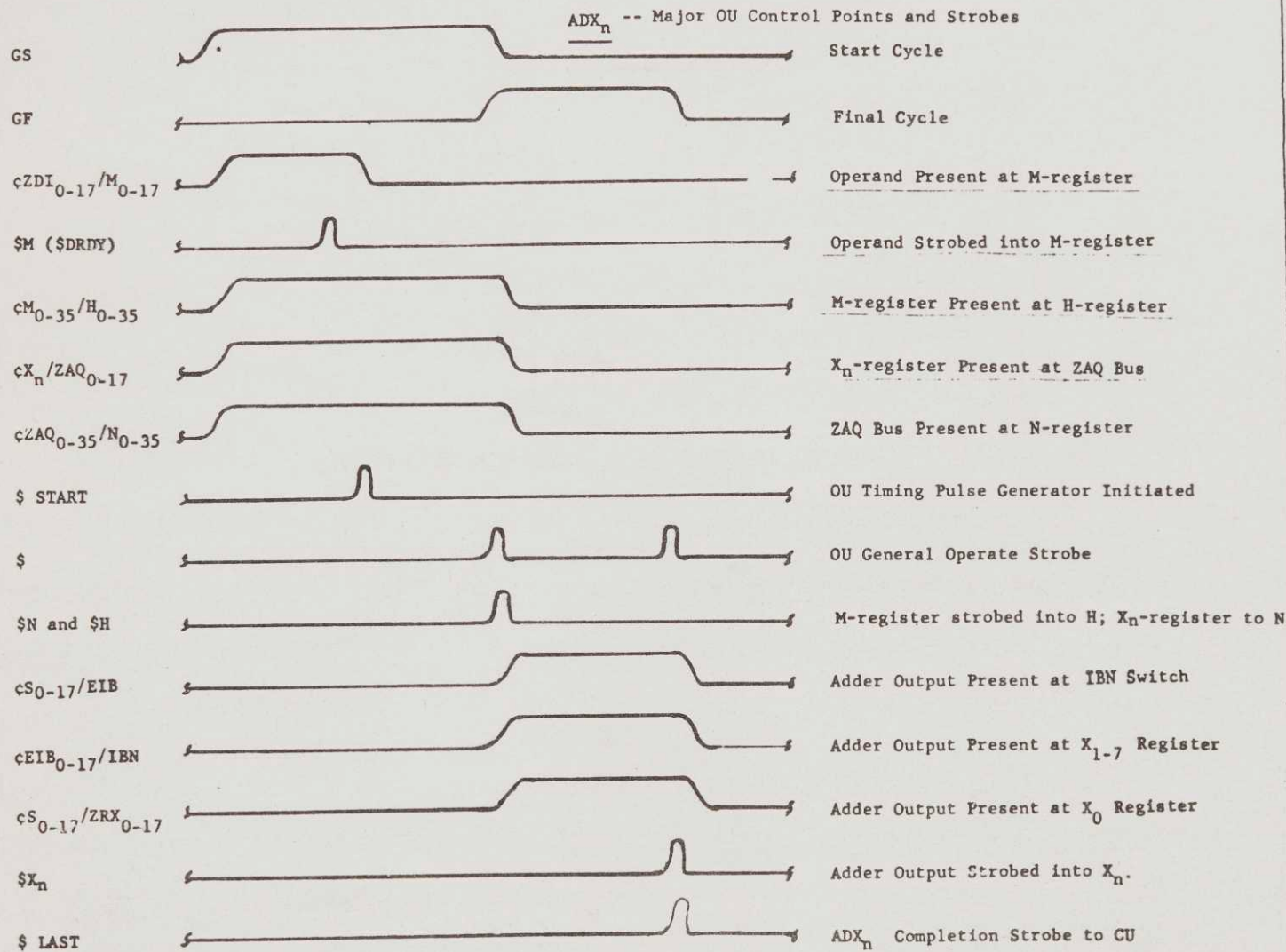


FIG. 12.3.1.1a AD_{X_n} Instruction, Timing Diagram

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Spec. No. M50EB00107

Cont. on Sh. 12-41 Sh. No. 12-40

TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR

12.3.1.1 - contd

Example 3: Logical (ORA)

During this instruction the Boolean connective "OR" function is performed with the contents of the A-register and the contents of a memory location Y. The logical OR is performed in the S-adder and the results placed in the A-register.

The data path from ZDI/M and the generation of \$ START for the ORA instruction is identical to that of the LDA instruction.

GS

During GS, the IH switch is enabled by $\phi M_0-35/H_0-35$, the ZAQ switch by $\phi AQ_0-35/ZAQ_0-35$, and the IN switch by $\phi ZAQ_0-35/N_0-35$. These enabled switches allow the operands from memory and the A-register to be present at the inputs to the H- and N-registers.

When the \$ START pulse propagates the medium delay elements, the operate strobe \$ occurs. This pulse permits the following:

- 1) The GS cycle to reset the GF cycle to set.
- 2) \$H is generated which strobes the memory operand from the M- to the H-register.
- 3) \$N is generated which strobes the present A-register contents into the N-register.
- 4) The Zero and Sign Indicators to reset.
- 5) The ORB flip-flop to reset.
- 6) Flip-flops K_1 and K_2 of the adder control register are set to place the adder in a Logical "OR" configuration.

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Spec. No. M50EB00107

Cont. on Sh.12-42 Sh. No.12-41

TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR

12.3.1.1 - contd

- 7) The \$ strobe enters the Timing Pulse Generator delay line network to produce another \$ strobe in approximately 400 nanoseconds.

GF

During GF the Logical "OR" of the contents of the H- and N-registers is produced by the S-adder.

When the GF set, the $\phi S_0-35/AQ_0-35$ gate on the IAQ switch became enabled making the S-adder outputs available on the inputs to the A-register. On the occurrence of the next \$ strobe, $\$AQ_0-35$ is generated and the adder output is strobed into the A-register. At this time the results of the Logical OR of a memory location Y and the A-register are placed in the A-register. This \$ strobe also:

- 1) Resets the GF cycle flip-flop.
- 2) Resets the OUB flip-flop if no other instruction has been initiated.
- 3) Sets the Sign Indicator if bit zero of the "OR" resultant was a 1.
- 4) Sets the Zero Indicator if the "OR" resultant was zero.
- 5) Resets K_1 and K_2 adder controls.
- 6) Generates \$ LAST, which is sent to the CU to indicate completion of the ORA instruction.

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Spec. No. M50EB00107

Cont. on Sh.12-43 Sh. No.12-42

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GE-645 PROTOTYPE PROCESSOR

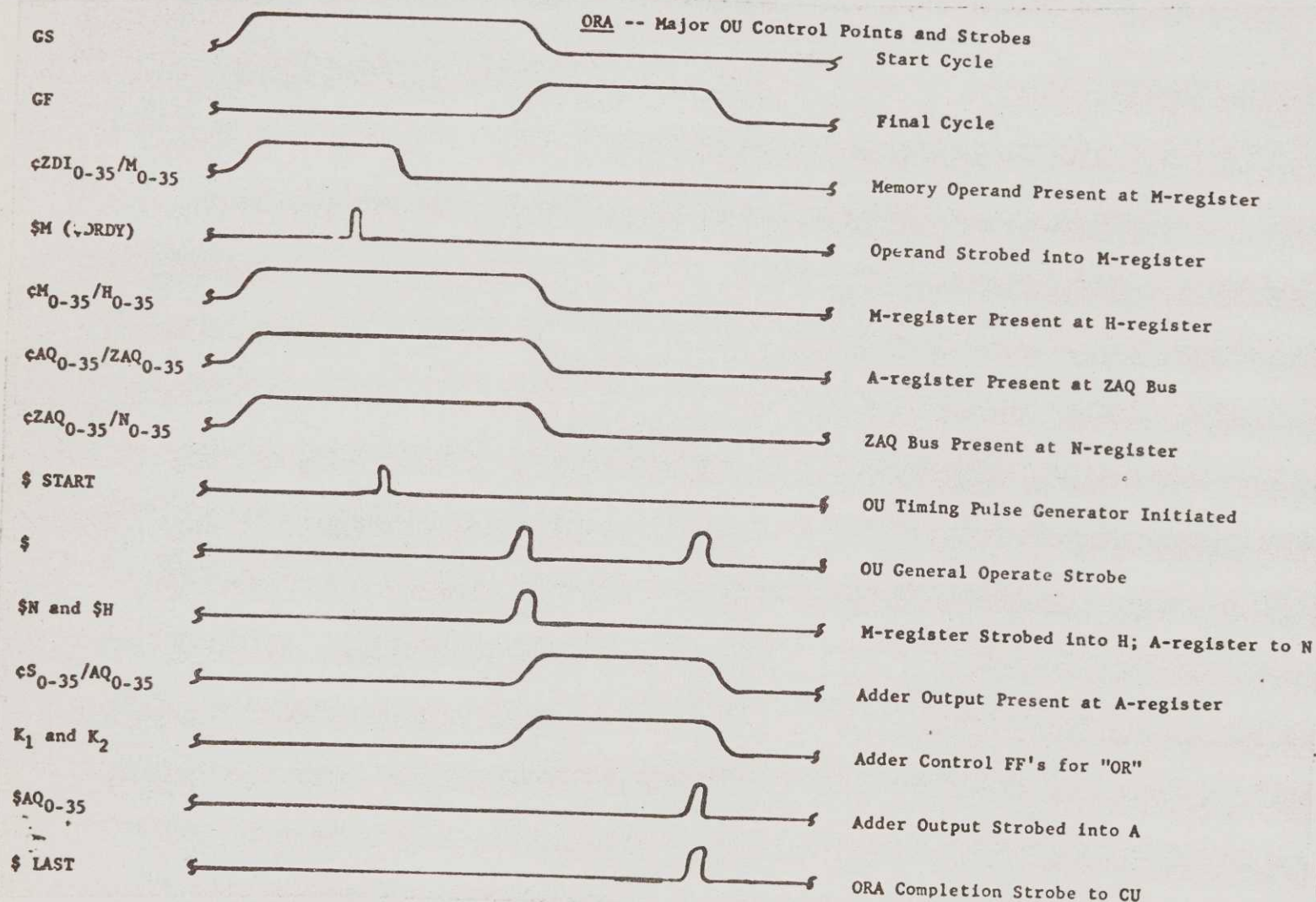


FIG. 12.3.1.1b ORA Instruction, Timing Diagram

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Cont. on Sh.12-44 Sh. No.12-43

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GE-645 PROTOTYPE PROCESSOR

ORA (275)₈
OR to Accumulator

All Registers are shown before the strobe at the end
of the cycle.

GS

$\phi M_{0-35}/H_{0-35}$	AQ	0	A	35 36	Q	71
		001100	→	00	111001	→ 111
$\phi AQ_{0-35}/ZAQ_{0-35}$	N	0		35 36		71
		00	→	00	01110	→ 00
$\phi ZAQ_{0-35}/N_{0-35}$	S	0		35 36		71
		000	→	010	01110	→ 00
$\phi SET K_1, \phi SET K_2$	H	0		35 36		71
$\phi RESET ZERO IND$		000	→	010	00	→ 00
$\phi RESET NEGATIVE IND$						
ϕH	M	0		35 36		71
ϕN		010110	→	00	00000	→ 000

Strobe on \$

FIG. 12.3.1.1c Register Contents During GS Cycle of ORA Instruction

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Spec. No. M50EB00107

Cont. on Sh.12-45 Sh. No. 12-44

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

ORA (275)₈
OR to Accumulator - Cont

GF

¢S₀-35/A

¢ RESET K₁
¢ RESET K₂
¢ Set ZERO IND
if S = 0
¢ SET NEGATIVE IND
if S₀ = 1
\$A

Strobe
on \$

AQ	0	A	35	36	Q	71
	001100	→	00	111001	→	111
N	0		35	36		71
	001100	→	00	000	→	000
S	0		35	36		71
	0111100	→	000	0000	→	000
H	0		35	36		71
	010110	→	00	000	→	000
M	0		35	36		71
	010110	→	00	00000	→	000

Contents of Registers
at the end of the "OR"
operation. Note that
the Q portion of the
AQ is unaffected.

	0	A		Q	71
AQ	0111100→000		111001→1111		
	0				71
N	001100→00		00→000		
	0				71
S	011110→00		0000→000		
	0				71
H	010110→00		000→000		

FIG. 12.3.1.1d Register Contents During GF Cycle of ORA Instruction

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TITLE: ENGINEERING PRODUCT SPECIFICATION
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12.3.1.1 - contd

Example 4: Compare (CMG)

During this instruction the contents of a memory location Y are magnitude compared with the contents of the A-register and the Zero or Sign Indicators are set depending on the comparison. In general, a compare is a subtract operation where the register contents are not altered. Since this operation is a compare magnitude, the operands to be compared must be of unlike signs. If the numbers are of like signs, the memory operand must be two's complemented before the compare is actually made.

The data path from ZDI/M and the generation of \$ START are the same as for the LDA instruction.

GS

During GS the signs of M_0 and A_0 are used to control the transfer of data from M to H. Because of the compare algorithm used, these signs must be opposite. Therefore, if the signs are not different, IH is enabled by $\bar{c}M_{0-35}/H_{0-35}$; if the signs are different, IH is enabled by cM_{0-35}/H_{0-35} . At the same time, the ZAQ switch is enabled by $\bar{c}AQ_{0-35}/ZAQ_{0-35}$ and the IN switch by $cZAQ_{0-35}/N_{0-35}$. These enabled switches allow the operands from memory and the A-register to be present at the inputs to the H- and N-registers.

When the \$ START pulse propagates the medium delay elements, the operate strobe \$ occurs. This allows the following events:

- 1) The GS cycle to reset and the GF cycle to set.
- 2) \$H is generated which strobes the memory operand from the M- to the H- register.
- 3) \$N is generated which strobes the A-register contents into the N-register.

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TITLE: ENGINEERING PRODUCT SPECIFICATION
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12.3.1.1- contd

- 4) If the signs of the A- and M-registers are the same, K₇₂ control flip-flop will be set to force an initial carry into the adder.
- 5) The Zero and Sign Indicators are reset.
- 6) The ORB flip-flop to reset.
- 7) The \$ strobe enters the Timing Pulse Generator delay line network to produce another \$ strobe in approximately 400 nanoseconds.

GF

During GF the contents of the N- and H-registers are subtracted in the S-adder. (Refer to section 12.10 for a detailed description of the adder.)

On the occurrence of the next \$ strobe, an indicator may be set depending on the compare. If the contents of A and Y were equal, the Zero Indicator is set. If the contents of A were greater than Y, no indicator is set. If the contents of A were less than Y, the Sign Indicator is set. This \$ strobe also:

- 1) Resets the GF cycle flip-flop.
- 2) Resets the OUB flip-flop if no other instruction has been initiated.
- 3) Resets the K₇₂ control flip-flop if it is set.
- 4) Generates \$ LAST, which is sent to the CU to indicate completion of the CMG instruction.

TITLE: ENGINEERING PRODUCT SPECIFICATION
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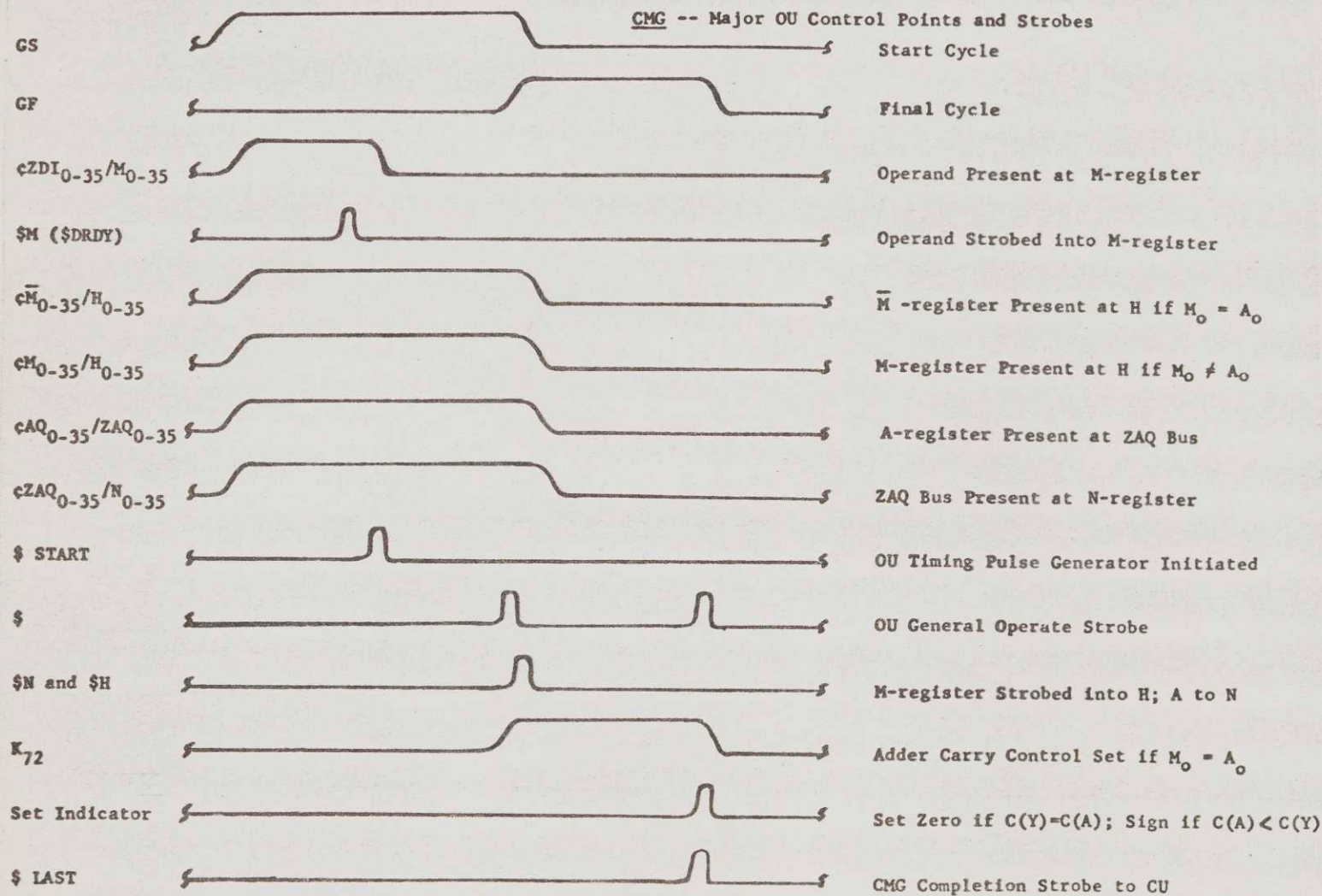


FIG. 12.3.1.1e CMG Instruction, Timing Diagram

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TITLE: ENGINEERING PRODUCT SPECIFICATION
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12.3.1.1 - contd

Example 5: Negate (NEG)

During this instruction, the contents of the A-register are converted to the negative of the original quantity by forming the two's complement of the number. The results are stored in the A-register.

No memory operand is required for this instruction. However, a \$DRDY is still received from the CU for the necessity of generating \$ START. The generation of this pulse is the same as for the instructions previously discussed.

GS

When the GS cycle is started and the NEG decode complete, the ZAQ switch becomes enabled by $\bar{c}AQ_{0-35}/ZAQ_{0-35}$, and the IN switch by $\bar{c}ZAQ_{0-35}/N_{0-35}$ and $\bar{c}ZAQ_{36-71}/N_{36-71}$. These enabled switches allow the one's complement of the A-register to be present at the inputs of the N-register.

When the \$ START pulse propagates the medium delay elements, the operate strobe \$ occurs. This allows the following events:

- 1) The GS cycle to reset and the GF cycle to set.
- 2) \$H is generated, but since the IH switch is not enabled all zeros are strobed into H.
- 3) \$N is generated which strobes the one's complement of the A-register into N.
- 4) The Zero and Sign Indicators are reset.
- 5) The adder control flip-flop K_{72} is set to force the initial carry in forming the two's complement.

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12.3.1.1 - contd

- 6) The ORB flip-flop is reset.
- 7) The \$ strobe enters the Timing Pulse Generator to produce another \$ strobe in approximately 400 nano-seconds.

GF

During GF the contents of H (H = 0) and N are added in the S-adder.

When GF set, the $\phi S_{0-35}/AQ_{0-35}$ gate on the IAQ switch was enabled making the adder outputs available on the inputs to the A-register. On the occurrence of the next \$ strobe, $\$AQ_{0-35}$ is generated and the adder output is strobed into the A-register. At this time the two's complement of the original contents of A are placed back in A. This \$ strobe also:

- 1) Resets the GF cycle flip-flop.
- 2) Resets the OUB flip-flop if no other instruction has been initiated.
- 3) Sets the Sign Indicator if bit zero of the negated resultant is a one.
- 4) Sets the Zero Indicator if the negate resultant is zero.
- 5) Sets the Overflow Indicator if the range of A is exceeded.
- 6) Resets the K₇₂ flip-flop.
- 7) Generates \$ LAST, which is sent to the CU to indicate completion of the NEG instruction.

TITLE:

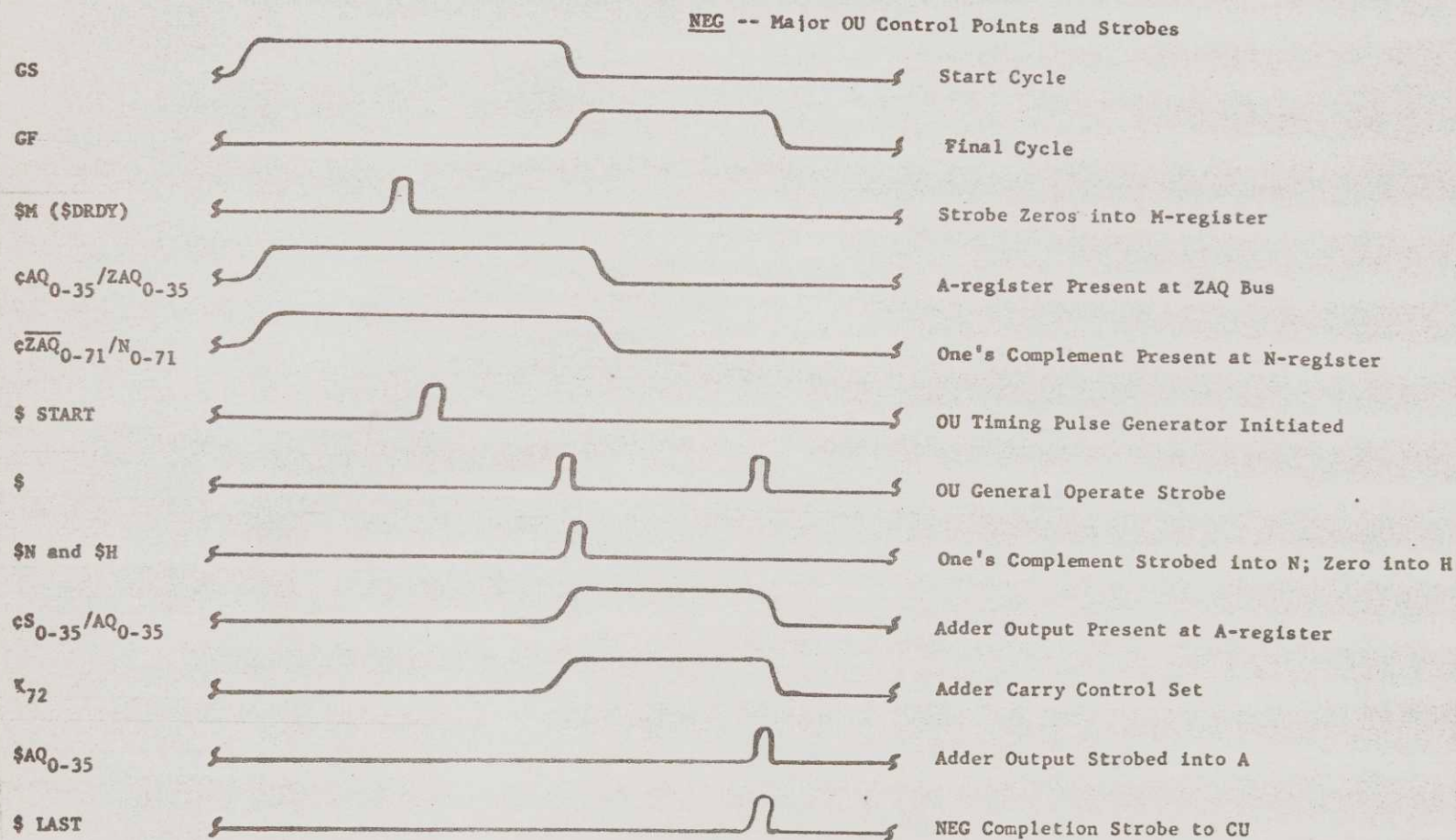
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FIG. 12.3.1.1f NEG Instruction, Timing Diagram

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TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

12.3.1.1 - contd

Example 6: Logical (ANA)

During this instruction the Boolean connective "AND" function is performed with the contents of the A-register and the contents of a memory location Y. The logical AND is performed in the S-adder and the results are placed in the A-register.

The data path from ZDI/M and the generation of \$ START is identical to the LDA instruction.

Because of an internal peculiarity in the S-adder when executing a logical product or AND, it is necessary to load the one's complement of the memory operand into the H-register. This is made necessary because the adder equation for a logical AND is $(N_1) (\bar{H}_1)$.

GS

During GS the IH switch is enabled by $\bar{c}M_{0-35}/H_{0-35}$. The ZAQ witch is enabled by cAQ_{0-35}/Z_{0-35} and the IN switch by cZ_{0-35}/N_{0-35} . These enabled switches allow the operands to be present at the H- and N-registers.

The lower half of $\bar{M}$ is enabled into H, but this is a don't care condition. Since the N-register will contain only zeros in the lower half, this is sufficient to inhibit any one's from being produced in the lower half of the adder output.

When the \$ START pulse propagates the medium delay elements, the operate strobe \$ occurs. This allows the following events:

- 1) The GS cycle to reset and the GF cycle to set.

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TITLE: ENGINEERING PRODUCT SPECIFICATION
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12.3.1.1 - contd

- 2) \$H is generated which strobes the complement of the memory operand from the M- to the H-register.
- 3) \$N is generated which strobes the A-register contents into the N-register.
- 4) The Zero and Sign Indicators to reset.
- 5) Flip-flops K_1 and K_3 of the adder control register are set to place the adder in the Logical "AND" configuration.
- 6) The ORB flip-flop to reset.
- 7) The \$ Strobe enters the Timing Pulse Generator delay line network to produce another \$ strobe in approximately 400 nanoseconds.

GF

During the GF the Logical "AND" of the contents of the H- and N-registers is generated in the S-adder.

When GF set, the $\phi S_{0-35}/AQ_{0-35}$ gate on the IAQ switch was enabled making the adder outputs available at the inputs to the A-register. On the occurrence of the next \$ strobe, $\$AQ_{0-35}$ is generated and the adder output is strobed into the A-register. This \$ strobe also:

- 1) Resets the GF cycle flip-flop.
- 2) Resets the OUB flip-flop if no other instruction has been initiated.
- 3) Sets the Zero Indicator if the "AND" resultant is zero.

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Cont. on Sh.12-54 Sh. No.12-53

TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR

12.3.1.1 - contd

- 4) Sets the Sign Indicator if bit zero of the "AND" resultant is a one.
- 5) Resets K_1 and K_3 flip-flops.
- 6) Generates \$ LAST, which is sent to the CU to indicate completion of the ANA instruction.

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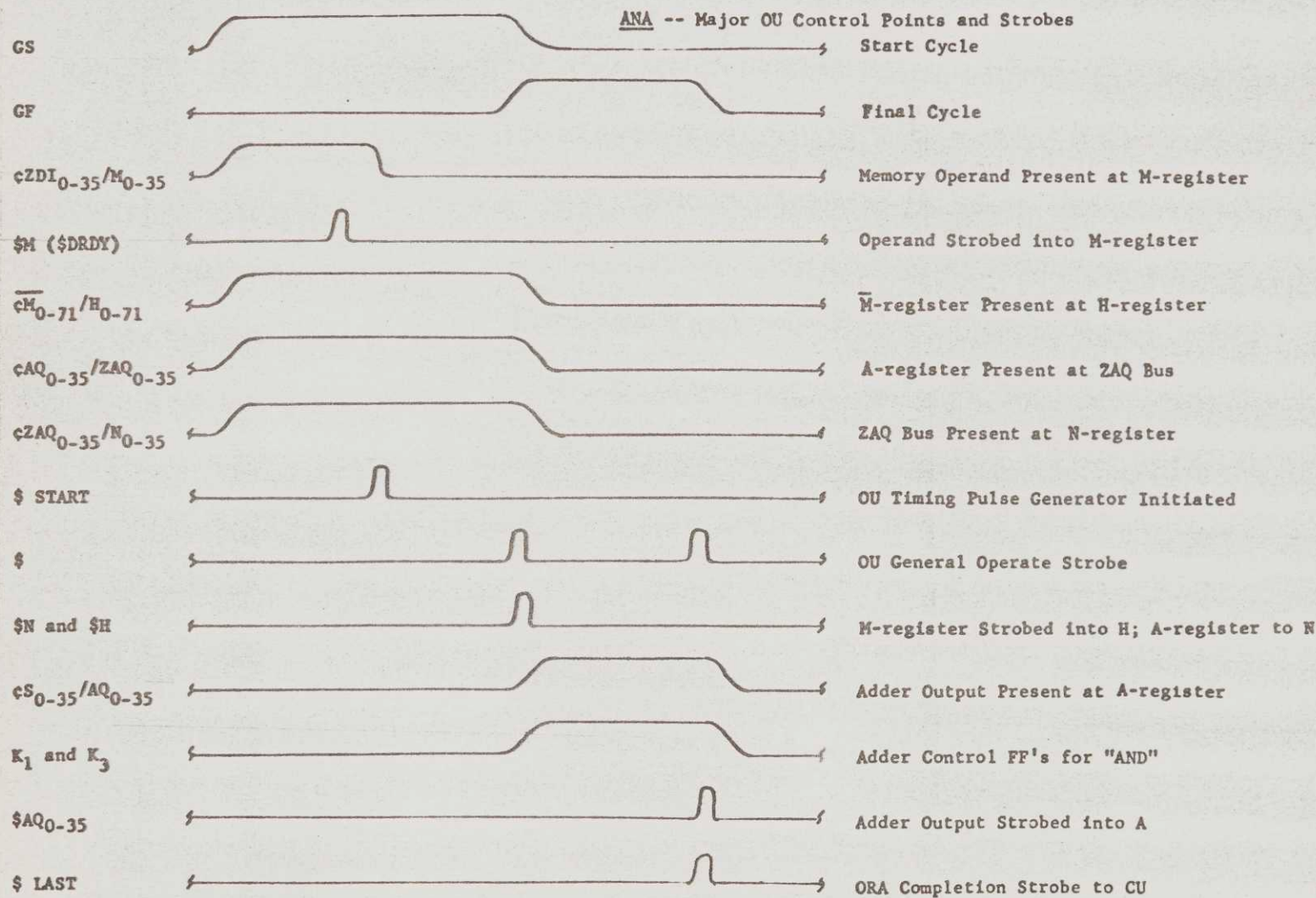


FIG. 12.3.1.1g ANA Instruction, Timing Diagram

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TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR

ANA (375)₈
 AND to Accumulator

All Registers are shown before the strobe at the end of the cycle.

GS

$\bar{c}M_{0-35}/H_{0-35}$, $\bar{c}M_{36-71}/H_{36-71}$

AQ

0	AQ	35	36	Q	71
0101100	→	00	001111	→	111

$\bar{c}AQ_{0-35}/ZAQ_{0-35}$

N

0	35	36	71
1110111	→	1111	111 → 111

$\bar{c}ZAQ_{0-35}/N_{0-35}$

S

0	35	36	71
1111000	→	000	00 → 000

$\bar{c}SET K_1$, $\bar{c}SET K_3$
 $\bar{c} RESET ZERO IND$
 $\bar{c} RESET NEGATIVE IND$
 $\$H$, $\$N$ } On \$

H

0	35	36	71
0000	→	000	000 → 001

M

0	35	36	71
010011	→	1111	000 → 0000

FIG. 12.3.1.1h Register Contents During GS Cycle of ANA Instruction

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TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

ANA (375)₈
AND to Accumulator - Contd

GF

¢S₀-35/A

¢ RESET K₁ ¢ RESET K₃
¢ SET ZERO IND if S = 0
¢ SET NEGATIVE IND if
S₀ = 1

\$A

on \$

AQ 0 A 35 36 Q 71
0101100→00 001111→1111

N 0 35 36 71
0101100→00 00→000

S 0 35 36 71
0100100→000 000→000

H 0 35 36 71
101100→0000 111→1111

M 0 35 36 71
010011→1111 000→000

(K₁)
(K₃)

Contents of Registers
at the end of the ANA
operation. Note that
the Q portion of the
AQ is unaffected.

AQ 0 A Q 71
0100100→000 001111→1111

N 0 71
0101100→00 000→00

S 0 71
0000100→000 11111→11111

H 0 71
1011000→000 1111→1111

M 0 71
010011→11111 0000→000

FIG. 12.3.1.1i Register Contents During GF Cycle of ANA Instruction

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TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

12.3.1.1 - contd

Example 7: Add (ADL)

During this instruction a 72-bit operand is formed using a 36-bit word from memory by placing the memory word in the lower 36 through 71-bit positions of the H-register and forcing bits 0 through 35 to be the same as the sign bit of the memory word. When this operand is formed, it is added to the contents of the 72-bit AQ-register and the results are stored in AQ. This is the only instruction in the single precision portion of the Add Group which generates a 72-bit arithmetic resultant.

The control points $\zeta ZDI_{0-27}/M_{36-63}$ and $\zeta ZDI_{28-35}/M_{64-71}$ are enabled to allow the memory operand to be placed in the the lower half of the M-register on \$DRDY. \$ START is generated in the normal manner.

GS

During GS the IH switch is enabled by $\zeta M_{36-71}/H_{36-71}$ and $\zeta M_{0-35}/H_{0-35}$. If bit zero of the memory operand (M_{36}) were a one, then ζM_{0-35} is also enabled. The control of $\zeta M_{0-35}/H_{0-35}$ allows the upper half of the H-register to be filled with ones or zeros depending on the sign of the memory operand. The ZAQ switch is enabled by $\zeta AQ_{0-35}/ZAQ_{0-35}$ and $\zeta AQ_{36-71}/ZAQ_{36-71}$. The IN switch is enabled by $\zeta ZAQ_{0-35}/N_{0-35}$ and $\zeta ZAQ_{36-71}/N_{36-71}$. These enabled switches allow the generated 72-bit memory operand and the AQ operand to be present at the H- and N-registers.

When the \$ START pulse propagates the medium delay elements, the operate strobe \$ occurs. This allows the following events:

- 1) The GS cycle to reset and the GF cycle to set.
- 2) \$H is generated which strobes the memory operand plus its extended sign from the M-to the H-register.

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12.3.1.1 - contd

- 3) \$N is generated which strobes the AQ-register contents into the N-register.
- 4) The Zero and Sign Indicators to reset.
- 5) The ORB flip-flop to reset.
- 6) The \$ strobe enters the Timing Pulse Generator delay line network to produce another \$ strobe in approximately 400 nanoseconds.

GF

During GF the contents of H and N are added in the S-adder.

When GF was set, the $\phi S_{0-35}/AQ_{0-35}$ and $\phi S_{36-71}/AQ_{36-71}$ gates on the IAQ switch were enabled making the adder outputs available at the inputs to the AQ-register. On the occurrence of the next \$ strobe, \$AQ₀₋₃₅ and \$AQ₃₆₋₇₁ are generated and the adder output is strobed into AQ. This \$ strobe also:

- 1) Resets the GF cycle flip-flop.
- 2) Resets the OUB flip-flop if no other instruction has been initiated.
- 3) Sets the Zero Indicator if the resultant of the ADL is zero.
- 4) Sets the Sign Indicator if bit zero of the ADL resultant is a one.
- 5) Sets the Overflow Indicator if the range of AQ is exceeded.

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TITLE: ENGINEERING PRODUCT SPECIFICATION
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12.3.1.1 - contd

- 6) Sets the Carry Indicator if there was a carry out of bit zero of the adder; otherwise off.
- 7) Generates \$ LAST, which is sent to the CU to indicate completion of the ADL instruction.

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TITLE: ENGINEERING PRODUCT SPECIFICATION
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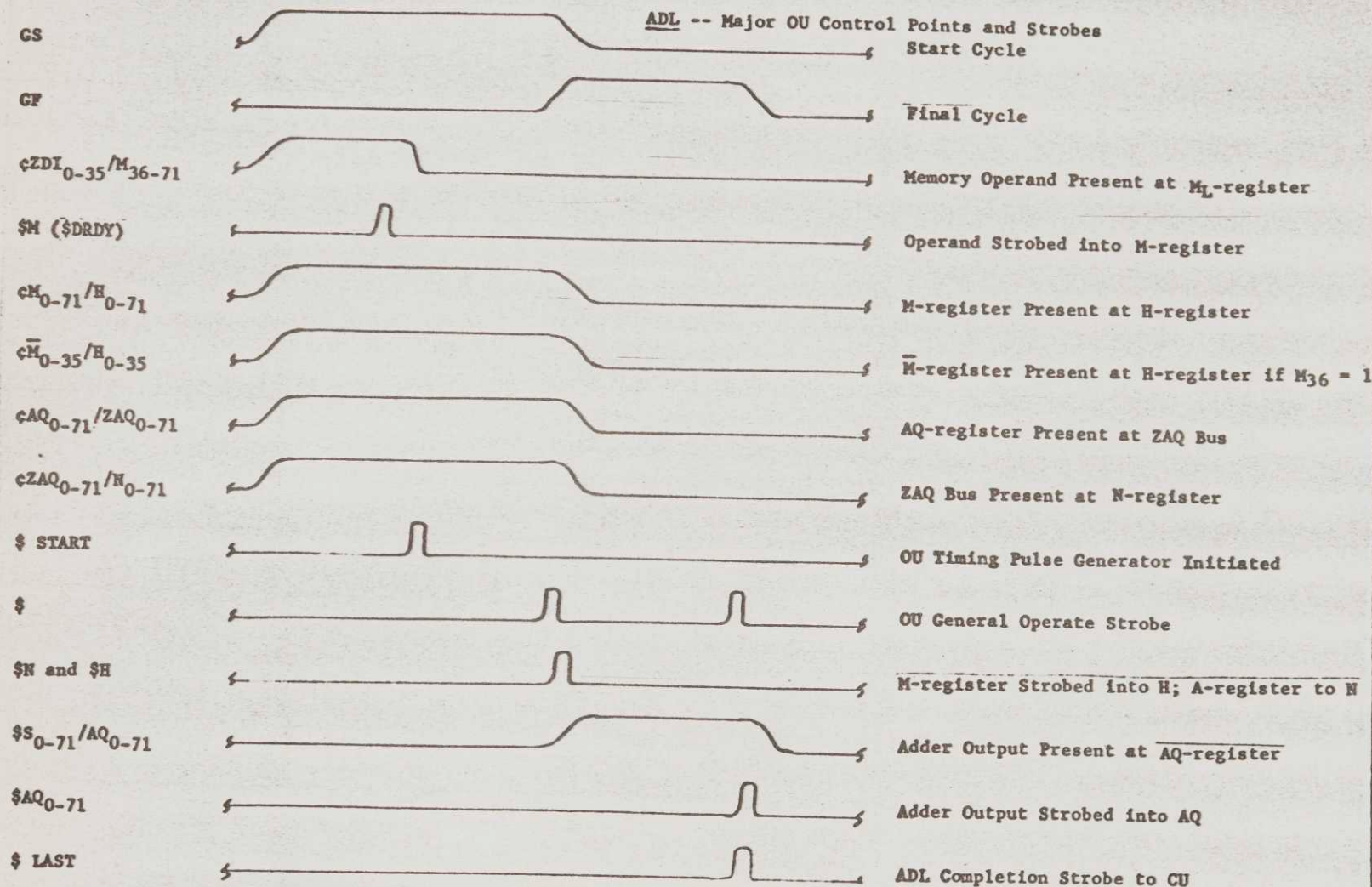


FIG. 12.3.1.1j ADL Instruction, Timing Diagram

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TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR

12.3.1.1 - contd

Example 8: Special Load RET - RTD - RCU.

All three of these instructions are treated the same by the OU. In fact the CF forces a 630 op code into the O-register for all three instructions. The only action of the OU is to load its Indicator Register from data supplied from memory. To determine what bit sets what indicator see GE-645 EPS, Sec. I.

These instructions are the same as the LDA (Example 1) except that during GF the contents of S₁₈₋₂₇ are strobed directly into the Indicator Register.

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TITLE: ENGINEERING PRODUCT SPECIFICATION
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12.3.1.2 Double Precision

The instructions comprising the double precision portion of the Add Group are:

RMCM, NEGL, ADLAQ, ADAQ, CMPAQ, SBLAQ, SBAQ, CANAQ, LCAQ, ANAQ, CNAAQ, LDAQ, ORAQ, ERAQ, RCCL.

The only difference in the OU between these instructions and those in the single precision portion of the Add Group is that these instructions manipulate 72 bits of data instead of 36, and two \$DRDY's are required to accumulate input data in the M-register instead of one.

Example 1: Logical (CANAQ)

During this instruction, the contents of a pair of memory locations are compared logically with the contents of the AQ-register by means of the Boolean connective "AND" function. The only differences between this and the ANA instruction described in Section 12.3.1.1 is that this instruction is double precision, only sets indicators, and the contents of the AQ-register are not disturbed.

The IM switch is enabled by the presence of the CANAQ decode together with DPFF, BCFF, and DIC all reset. The control points $\phi ZDI_{0-17}/M_{0-17}$, $\phi ZDI_{18-27}/M_{18-27}$, and $\phi ZDI_{28-35}/M_{28-35}$ are enabled to allow the ZDI bus to be present at the M-register inputs. When the first operand ready strobe \$DRDY is received from the CU, the Double Precision flip-flop not yet being set allows the M-register strobe $\$M_{0-71}$ to be generated and strobe the most significant portion of the CANAQ operand into the M-register. This \$DRDY strobe sets the Double Precision flip-flop (DPFF). The OU will not generate \$ START until the second \$DRDY is received. On the setting of DPFF, the IM switch becomes enabled by $\phi ZDI_{0-27}/M_{36-63}$ and $\phi ZDI_{28-35}/M_{64-71}$.

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TITLE: ENGINEERING PRODUCT SPECIFICATION
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12.3.1.2 - contd

When the second \$DRDY is received about 300 nanoseconds after the first, the fact that DPFF is set and the CANAQ decode is true allows the M-register strobe \$M₃₆₋₇₁ to be generated and strobe the least significant portion of the CANAQ operand into the M-register. This \$DRDY strobe resets DPFF and is turned around as \$YRY and returned to the CU to signal that a new instruction may be prepared.

GS

During GS the IH switch is enabled by $\bar{c}M_{0-35}/H_{0-35}$ and $\bar{c}M_{36-71}/H_{36-71}$. The ZAQ switch is enabled by cAQ_{0-35}/ZAQ_{0-35} and cAQ_{36-71}/ZAQ_{36-71} , and the IN switch is enabled by $cZAQ_{0-71}/N_{0-71}$. These enabled switches allow the operands to be present at the H- and N-registers.

When the \$ START pulse propagates the medium delay elements, the operate strobe \$ occurs. This allows the following events:

- 1) The GS cycle to reset and the GF cycle to set.
- 2) \$H is generated which strobes the complement of the memory operand from the M- to the H-register.
- 3) \$N is generated which strobes the AQ-register contents into N.
- 4) The Zero and Sign Indicators are reset.
- 5) Flip-flops K₁ and K₃ of the adder control register to set which place the adder in the Logical "AND" configuration.
- 6) The ORB flip-flop to reset.

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Cont. on Sh. 12-65 Sh. No.12-64

TITLE: ENGINEERING PRODUCT SPECIFICATION
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12.3.1.2 - contd

- 7) The \$ strobe enters the Timing Pulse Generator to produce another \$ strobe in approximately 400 nanoseconds.

GF

During GF, the Logical "AND" of the contents of the H- and N-registers is produced in the S-adder.

When the next \$ strobe occurs:

- 1) GF cycle flip-flop is reset.
- 2) OUB flip-flop is reset if no other instruction has been initiated.
- 3) The Zero Indicator is set if the "AND" results were zero.
- 4) The Sign Indicator is set if bit zero of the "AND" was a one.
- 5) Flip-flops K_1 and K_3 are reset.
- 6) Generates \$ LAST, which is sent to the CU to indicate completion of the CANAQ instruction.

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TITLE: ENGINEERING PRODUCT SPECIFICATION
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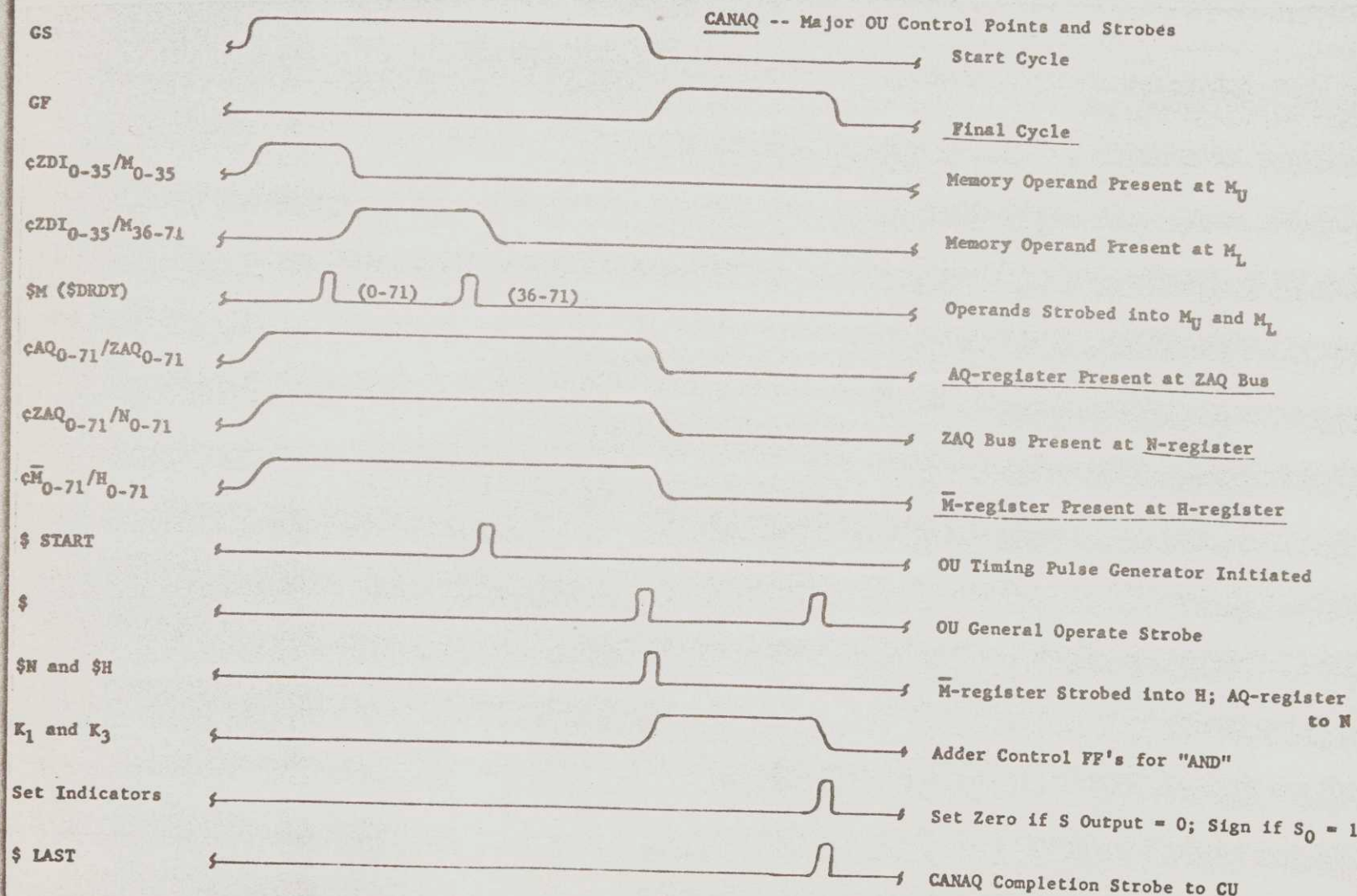


FIG. 12.3.1.2 CANAQ Instruction, Timing Diagram

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TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

12.3.1.2 - contd

Example 2: (SBAQ)

During this instruction the contents of a pair of memory locations are subtracted from AQ and the results are stored in AQ.

The IM switch is enabled by the presence of the SBAQ decode together with DPFF, BCFF, and DIC all reset. The control points $\phi ZDI_{0-17}/M_{0-17}$, $\phi ZDI_{18-27}/M_{18-27}$, and $\phi ZDI_{28-35}/M_{28-35}$ are enabled to allow the ZDI bus to be present at the M-register inputs. When the first operand ready strobe \$DRDY is received from the CU, the Double Precision flip-flop not yet being set allows the M-register strobe \$M₀₋₇₁ to be generated and strobe the most significant half of the SBAQ operand into the M-register. This \$DRDY strobe sets the Double Precision flip-flop (DPFF). The OU will not generate \$ START until the second \$DRDY is received. On the setting of DPFF, the IM switch becomes enabled by $\phi ZDI_{0-27}/M_{36-63}$ and $\phi ZDI_{28-35}/M_{64-71}$.

When the second \$DRDY is received about 300 nanoseconds after the first, the fact that DPFF is set and the SBAQ decode is true allows the M-register strobe \$M₃₆₋₇₁ to be generated and strobe the least significant portion of the SBAQ operand into the M-register. This \$DRDY strobe resets DPFF and is turned around as \$YRY and returned to the CU to signal that a new instruction may be prepared.

GS

During GS the IH switch is enabled by $\overline{\phi M}_{0-35}/H_{0-35}$ and $\overline{\phi M}_{36-71}/H_{36-71}$. The bar side of the M-register is enabled into H because subtraction in the two's complement system requires that one operand be negated (one's complement) and the initial carry be forced.

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GE-645 PROTOTYPE PROCESSOR

12.3.1.2 - contd

The ZAQ switch is enabled by $\phi AQ_{0-35}/ZAQ_{0-35}$ and $\phi AQ_{36-71}/ZAQ_{36-71}$, and the IN switch by $\phi ZAQ_{0-35}/N_{0-35}$ and ZAQ_{36-71}/N_{36-71} . These enabled switches allow the operands to be present at the H- and N-registers.

When the \$ START pulse propagates the medium delay elements, the operate strobe \$ occurs. This allows the following events:

- 1) The GS cycle to reset and the GF cycle to set.
- 2) \$H is generated which strobes the complement of the memory operand from the M- to the H-register.
- 3) \$N is generated which strobes the AQ-register contents into N.
- 4) The Zero and Sign Indicators are reset.
- 5) Flip-flop K₇₂ is set to force the initial carry into the adder.
- 6) The ORB flip-flop is reset.
- 7) The \$ strobe enters the Timing Pulse Generator delay line network to produce another \$ strobe in approximately 400 nanoseconds.

GF

During GF the contents of H and N are subtracted in the adder.

When GF set, the IAQ switch was enabled by $\phi S_{0-35}/AQ_{0-35}$ and $\phi S_{36-71}/AQ_{36-71}$. This allows the adder outputs to be available at the inputs to the AQ-register.

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Cont. on Sh. 12-69 Sh. No. 12-68

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12.3.1.2 - contd

When the next \$ strobe occurs, \$AQ₀₋₃₅ and \$AQ₃₆₋₇₁ are produced to strobe the adder output into AQ. This \$ strobe also:

- 1) Resets the GF flip-flop.
- 2) Resets the OUB flip-flop if no other instruction has been initiated.
- 3) Sets the Zero Indicator if the subtract resultant is zero.
- 4) Sets the Sign Indicator if bit zero of the subtract resultant is one.
- 5) Sets the Overflow Indicator if the range of AQ is exceeded.
- 6) Sets the Carry Indicator if a carry out of bit zero occurs, or resets it if no carry.
- 7) K₇₂ adder control is reset.
- 8) Generates \$ LAST, which is sent to the CU to indicate completion of the SBAQ instruction.

The SBLAQ instruction is identical to this instruction with the exception that the Overflow Indicator is not affected for SBLAQ.

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Cont. on Sh. 12-70 Sh. No. 12-69

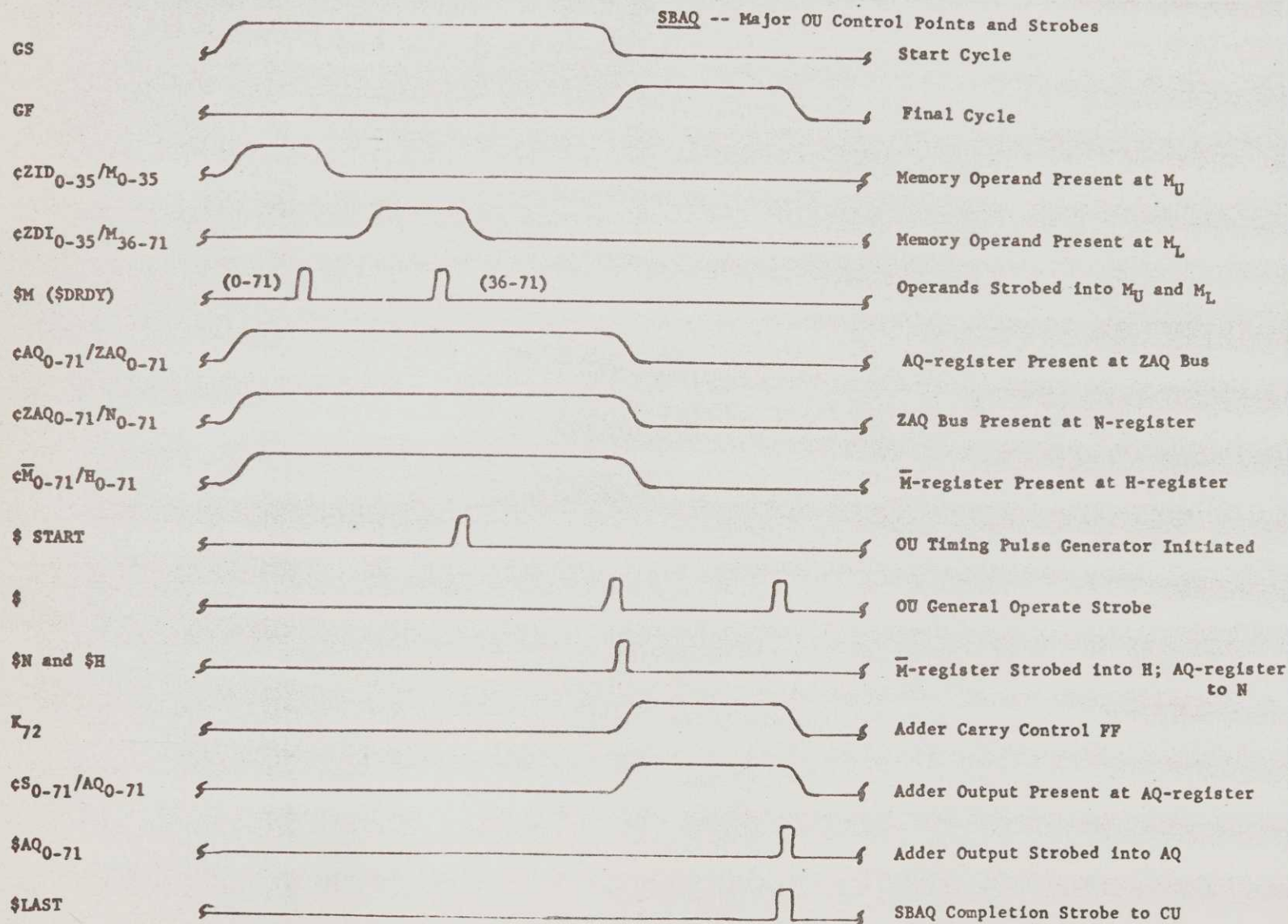


FIG. 12.3.1.2a SBAQ Instruction, Timing Diagram

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12.3.2 FIXED POINT STORE GROUP

This group of 31 instructions constitute the majority of store instructions executed in the OU. The major data paths and control points for these instructions are shown in Fig. 12.3.2. In the execution of these instructions, the contents of some OU-register are transferred to the ZDO bus (data out bus) via the ZAQ switch or the S-adder, and the ZDO switch.

To illustrate the control used in the execution of these instructions, several instructions will be explained in detail. For the detailed control of all instructions in this group, refer to the OU Specification Charts.

In the explanation of all the example instructions, the following conditions will be assumed:

- 1) The instruction has been strobed into the O-register.
- 2) The GS and GC cycle flip-flops have been set.
- 3) The DDF flip-flop has been set indicating the operation decode has settled.

NOTE: Reference to Fig. 12.3.2 and the partial timing diagram at the end of each example will aid in the understanding of the instruction execution and implementation.

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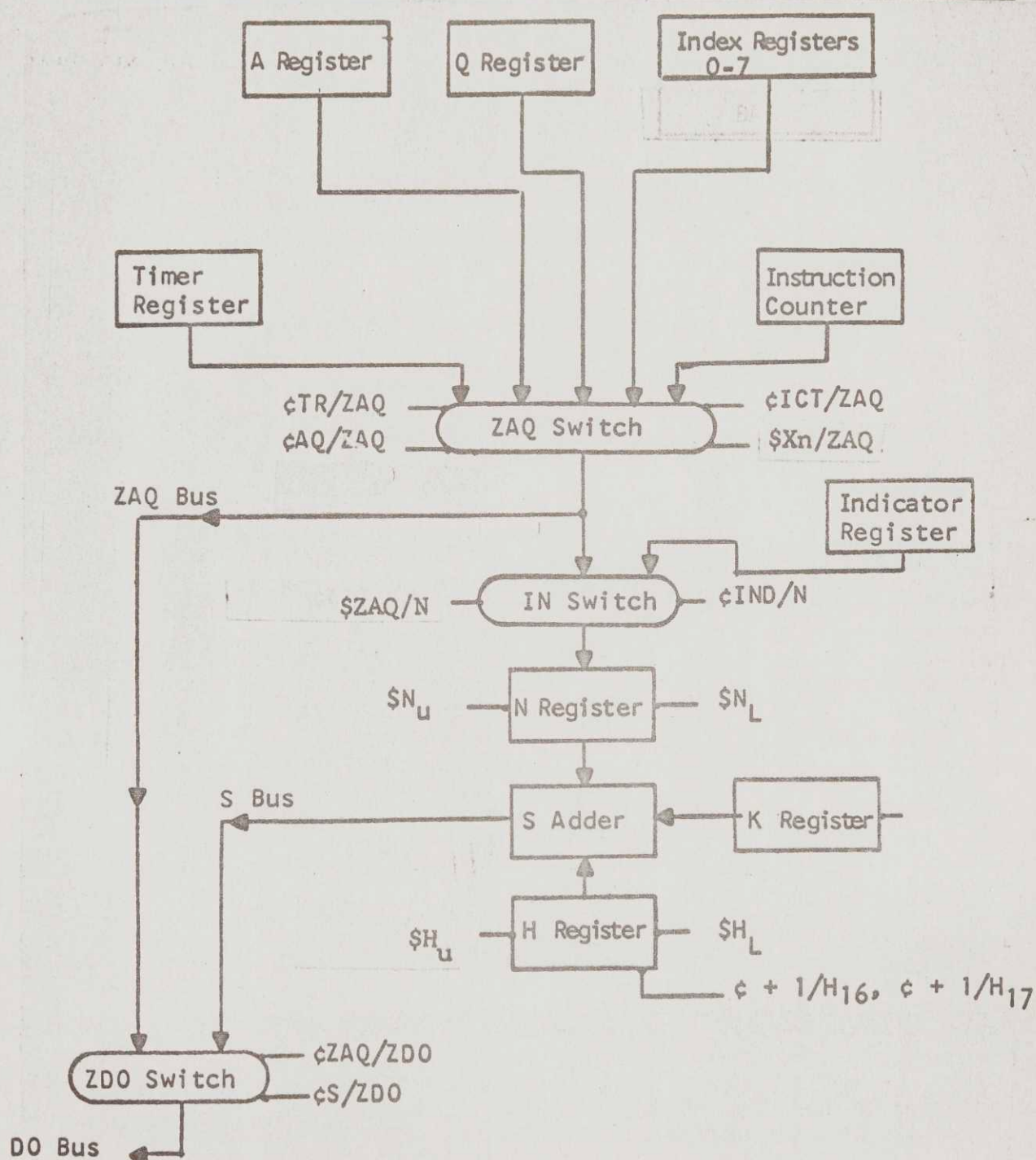


Fig. 12.3.2 Major Data Paths & Control Points for the Fixed Point Store Group of Instructions (OU)

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TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

12.3.2.1 Single Precision

The instructions comprising the single precision portion of the Fixed-Point Store Group are:

STX_n, STA, STQ, STBA, STZ, STT, STCA, STCQ, STBQ,
SXL_n, SMIC, STC1, STI, STC2,

The last three of these instructions are different only in that they are stored via the S-adder, whereas the rest are stored via the ZAQ bus. One other difference is that \$SDY for these three instructions is \$ Reset GS delayed and for all other stores and RAR's \$SDY is Set GS or Reset (GF).

Example 1: Store Q (STQ)

During this instruction the contents of the Q-register are stored in a memory location Y via the ZAQ bus.

The ZAQ and ZDO switches are enabled by the presence of the STQ decode together with the Byte Control flip-flop (BCFF) reset, the GC cycle flip-flop set, and the control point $\phi_{YS/ZDO}$ not enabled. The GC cycle will remain set from the beginning of the GS cycle to the end of the GF cycle for this store instruction. The ZAQ and ZDO switches are enabled by control points $\phi_{AQ36-71/ZAQ0-35}$ and $\phi_{ZAQ0-35/ZDO0-35}$.

When the \$ Set GS pulse was generated for this instruction, it was delayed by about 40 nanoseconds to become \$YRY and becomes \$SDY (store data ready). \$YRY sets the operand ready flip-flop, and is returned to the CU to signal that a new operation code may be sent to the OU. YRY set allows the

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Cont. on Sh.12-74 Sh. No.12-73

TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR

12.3.2.1 - contd

\$ START pulse to be generated and enter the Timing Pulse Generator to later produce the first operate strobe \$. \$ START sets the OU busy flip-flop, OUB. \$SDY is sent to the CU to initiate the memory store cycle prior to the occurrence of the first \$ strobe in the OU.

When the \$ START pulse propagates the medium delay elements the first operate strobe \$ occurs. This causes the following events:

- 1) The GS cycle to reset and the GF cycle to set.
- 2) The O-register Busy flip-flop (ORB) to reset.
- 3) The \$ strobe re-enters the Timing Pulse Generator, but is inhibited from exiting the delay line network.

The operand will be stored in the Data Out Buffer, in the Interface Frame, by \$INT. \$INT will also generate a \$DS and send it to the OU. \$DS is "ORed" into the Timing Pulse Generator and exits on the general strobe (\$) lines. This pulse:

- 1) Resets the GF and GC cycle flip-flops.
- 2) Resets the OUB flip-flop if no other instruction has been initiated.
- 3) Generates \$LAST, which is sent to the CU to indicate completion of the STQ instruction.

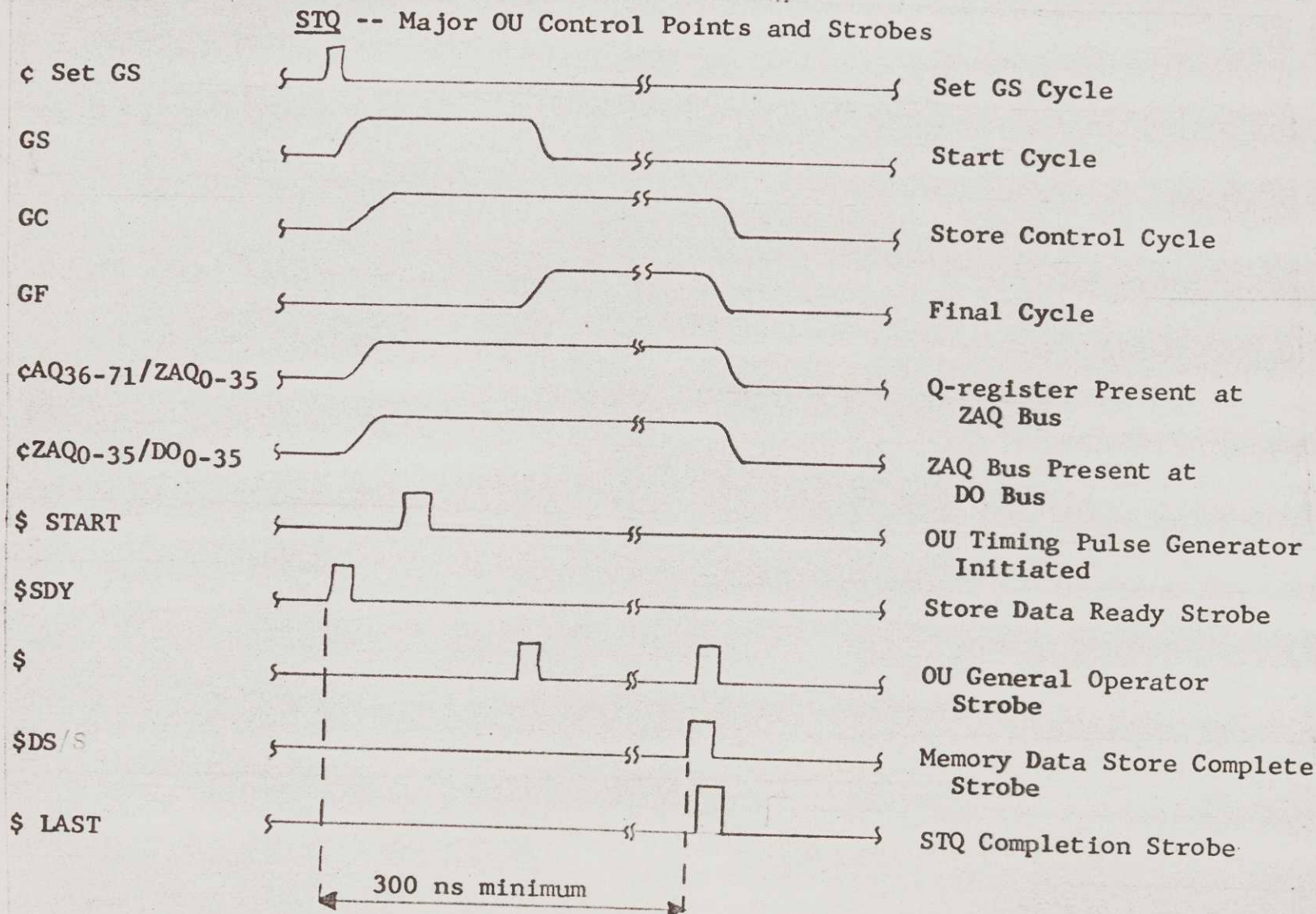


FIG. 12.3.2.1 STQ Instruction, Timing Diagram

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Cont. on Sh. 12-76 Sh. No. 12-75

TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR

12.3.2.1 - contd

Example 2: Store Instruction Counter Plus 1 (STC1)

During this instruction the contents of the Instruction Counter C are incremented by one and stored via the adder in bit positions 0-17 of a memory location Y. The Indicator Register is stored into bit positions 18-28 of the memory location Y at the same time the (ICT_c+1) is stored.

When the STC1 decode is complete and the GS cycle has been set, the ZAQ and IN switches become enabled. ZAQ is enabled by $\phi ICT_c/ZAQ_{0-17}$ and IN is enabled by $\phi ZAQ_{0-35}/N_{0-35}$ and $\phi IND/N_{18-35}$. These enabled switches allow the Instruction Counter and the Indicator Register to be present at the N-register input. At the same time that the ZAQ and IN switches are enabled, $\phi + 1/H_{17}$ is enabled on the input gate to bit 17 of the H-register.

When the \$ Set GS pulse was generated for this instruction, it was delayed by about 40 nanoseconds to become \$YRY. \$YRY sets the operand ready flip-flop YRY, and is returned to the CU. YRY set allows the \$ START pulse to be generated and enter the OU Timing Pulse Generator to later produce the operate strobe \$. \$ START sets the OU busy flip-flop OUB. \$ reset GS is delayed about 180 nanoseconds to become \$SDY.

\$SDY is sent to the CU to initiate the store cycle. The \$SDY strobe for the three instructions which are stored via the adder output bus anticipates the fact the OU will have the proper data on the DO bus by the time the Interface Frame is ready to accept it.

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Cont. on Sh.12-77 Sh. No.12-76

TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR

12.3.2.1 -contd

GS

When the \$ START pulse propagates the medium delay elements the first operate strobe \$ occurs. This causes the following events:

- 1) The GS cycle to reset and the GF cycle to set.
- 2) \$N strobes the Instruction Counter C into bit positions 0-17 of N, strobes the Indicator Register into bit positions 18-28 of N, and strobes zeros into the balance of the N-register.
- 3) \$H strobes all zeros into the H-register with the exception of bit 17 which is set to a one.
- 4) The ORB flip-flop is reset.
- 5) The \$ strobe re-enters the Timing Pulse Generator, but since a store is being executed it will be inhibited from exiting onto the general \$ lines.

GF

When the GF sets, the ZDO switch is enabled by $\phi S_{0-35}/DO_{0-35}$. This allows the adder output (which is the ICT_c+1 and the Indicator Register) to be present on the DO bus.

The operand will be stored in the Data Out Buffer, in the Interface Frame, by \$INT. \$INT will also generate a \$DS and send it to the OU. \$DS is "ORed" into the Timing Pulse Generator and exits on the general strobe (\$) lines. This pulse:

- 1) Resets the GF cycle.
- 2) Resets the OUB flip-flop if no other instruction has been initiated.
- 3) Generates \$ LAST, which is sent to the CU to indicate completion of STC1 instruction.

The STC2 instruction is similar to the STC1 except the ICT_c is incremented by 2 and the Indicator Register is not stored with ($ICT+2$).

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TITLE:

ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

STC1 -- Major OU Control Points and Strobes

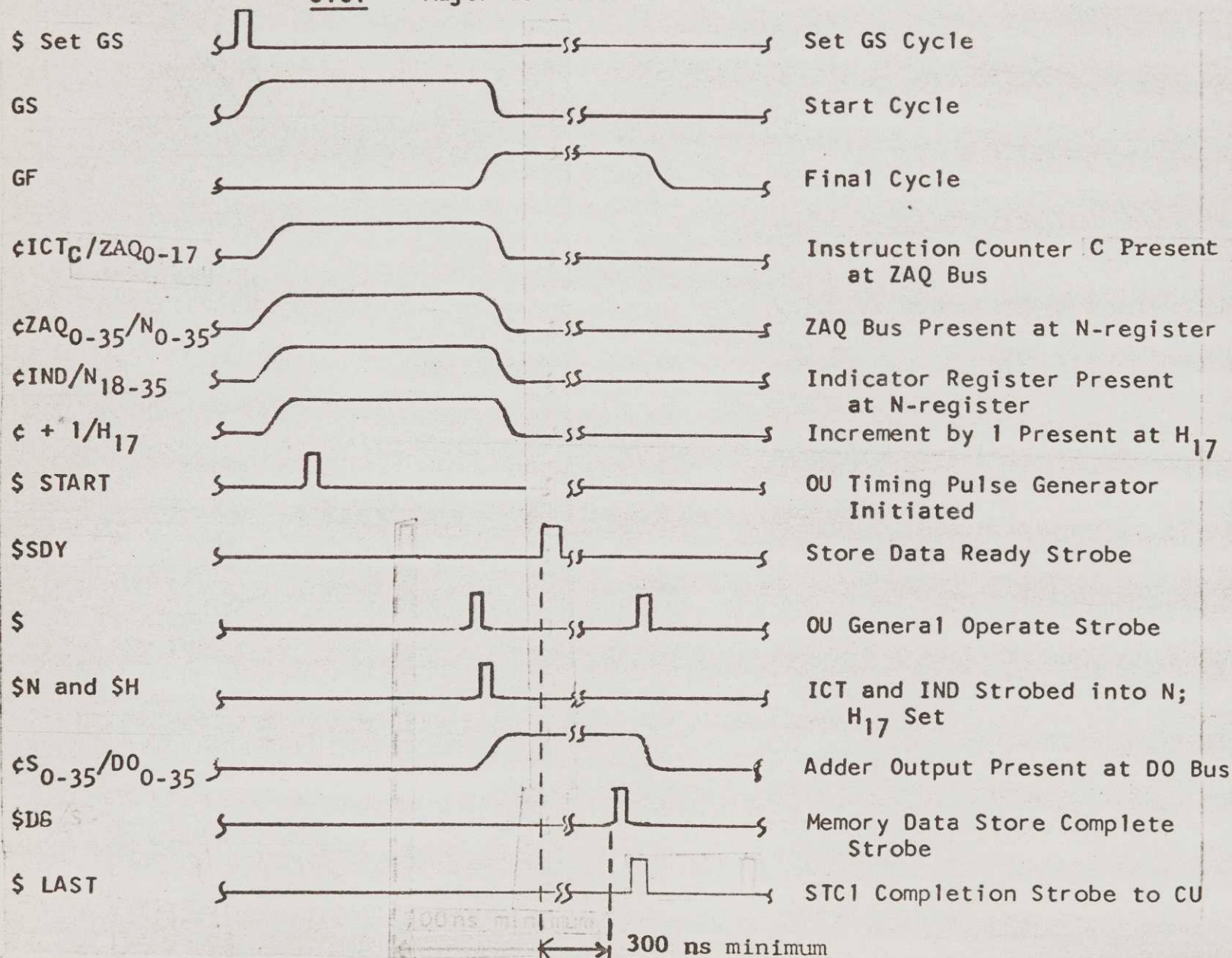


FIG. 12.3.2.1a STC1 Instruction Timing Diagram

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TITLE: ENGINEERING PRODUCT SPECIFICATION
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12.3.2.2 Double Precision

The instructions comprising the double precision portion of the Fixed-point Store Group are SMCM, LACL, and STAQ. In these instructions the contents of AQ are stored via the ZAQ bus.

Example 1: Set Memory Controller Mask Register (SMCM)

During this instruction the contents of the AQ are stored in a Memory Controller Interrupt Mask Register and a Memory Controller Access Mask Register as specified by bits 0-2 of the effective address Y.

When the SMCM decode has settled and the GS cycle is set, the GC cycle flip-flop sets. This allows the ZAQ and ZDO switches to be enabled by $\phi AQ_{0-35}/ZAQ_{0-35}$ and $\phi ZAQ_{0-35}/DO_{0-35}$. These switches enable the A-register to be present at the DO bus.

When the \$ Set GS pulse was generated for this instruction, it was delayed by about 40 nanoseconds to become \$YRY and it becomes \$SDY. \$YRY sets the operand ready flip-flop YRY, and is returned to the CU. YRY set allows the \$ START pulse to be generated and enter the OU Timing Pulse Generator to later produce the operate strobe \$. \$ START sets the OU busy flip-flop OUB.

\$SDY is sent to the CU to initiate the store cycle prior to the occurrence of the first \$ strobe in the OU.

GS

When the \$ START pulse propagates the medium delay elements the operate strobe \$ occurs. This causes the following events:

- 1) The GS cycle to reset and the GT cycle to set.

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TITLE: ENGINEERING PRODUCT SPECIFICATION
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12.3.2.2 - contd

- 2) The O-register busy flip-flop ORB, to reset.
- 3) A level consisting of DP stores and GT goes high.
- 4) The \$ strobe re-enters the Timing Pulse Generator, but since a store is being executed it is inhibited from exiting onto the general \$ lines.

GT

After a minimum time of 300 nanoseconds after \$SDY, the first half of the store operation will be complete and the first \$DS will be received from the Interface Frame to signal this fact. \$DS will produce a \$ strobe which will:

- 1) Reset the GC and GT cycle flip-flops.
- 2) Set the GF and GFT cycle flip-flops.
- 3) Cause the DP stores and GT level to go low after about 60 nanoseconds but only after \$ strobe has "ANDed" with it to produce \$DP which is delayed by approximately 270 nanoseconds before being sent to the Interface Frame to signify that the second data word is ready to be stored.

GF

When GF set, the ZAQ and ZDO switches became enabled by control points $\text{cAQ}_{36-71}/\text{ZAO}_{0-35}$ and $\text{cZAO}_{0-35}/\text{DO}_{0-35}$. This allows the Q-register outputs to be present at the DO bus before the OU sends the \$DP pulse to the Interface Frame for the second half store.

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Cont. on Sh.12-81 Sh. No.12-80

TITLE: ENGINEERING PRODUCT SPECIFICATION
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12.3.2.2 - contd

The \$DP strobes the data into the Data Out Buffer bits 36-71 and is returned as the second \$DS indicating the second half data has been received. This \$DS will generate a \$ strobe pulse which will:

- 1) Rest the GF and GFT cycles.
- 2) Reset the OUB flip-flop if no other instruction has been initiated.
- 3) Generates \$ LAST, which is sent to the CU to indicate completion of the SMCM instruction.

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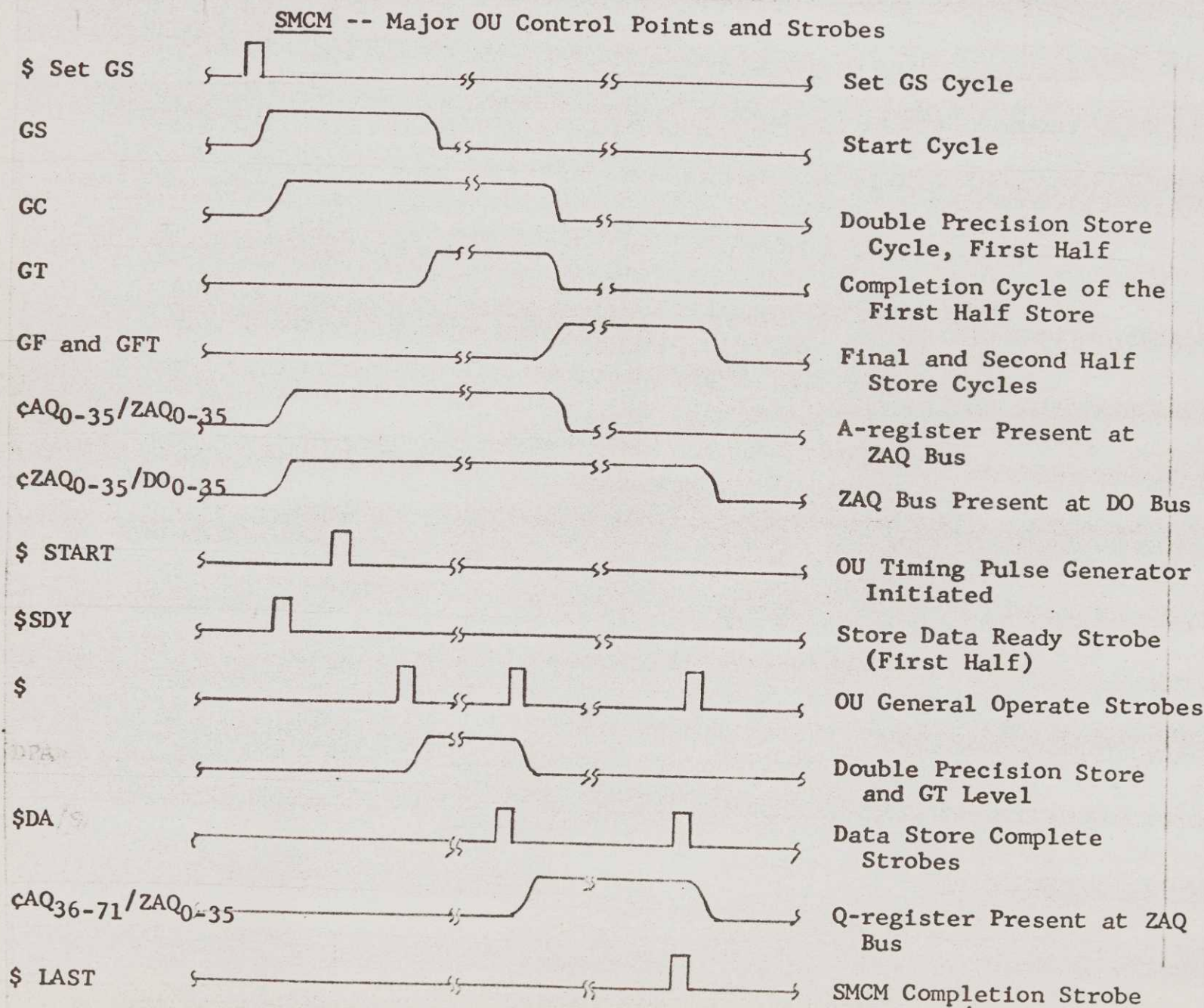


FIG. 12.3.2.2 SMCM Instruction. Timing Diagram

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TITLE: ENGINEERING PRODUCT SPECIFICATION
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12.3.3 READ-ALTER-REWRITE GROUP

This group of 52 instructions may be considered to be a composite of the single precision portion of the Add Group and Store Group instructions previously presented. They look like the Add Group in that a memory word is pulled into the OU and it is altered in the S-adder with the contents of some register (A, Q, or X_n). The storing of the adder results to the original memory location then make these instructions look similar to the Store Group. The instructions comprising the RAR Group are:

ASQ, ASA, ASX_n, SSQ, AOS, SSA, SSX_n, ANSQ, ANSA,
ANSX_n, ORSQ, ORSA, ORSX_n, ERSQ, ERSX_n, STAC.

These instructions are all single precision, all use the S-adder, and are all executed with a GS-GF cycle sequence. The major data paths and control points for these instructions are shown in Fig. 12.3.3.

To illustrate the control used in the execution of these instructions, several instructions will be explained in detail. For the detailed control of all instructions in this group, refer to the OU Specification Charts 43D140232, pages 2, 3, 5, and 11.

In the explanation of all the example instructions, the following conditions will be assumed:

- 1) The instruction has been strobed into the 0-register.
- 2) The GS cycle flip-flop has been set.
- 3) The DDF flip-flop has been set indicating the operation decode has settled.

NOTE: Reference to Fig. 12.3.3 and the partial timing diagram at the end of each example will aid in the understanding of the instruction execution and implementation.

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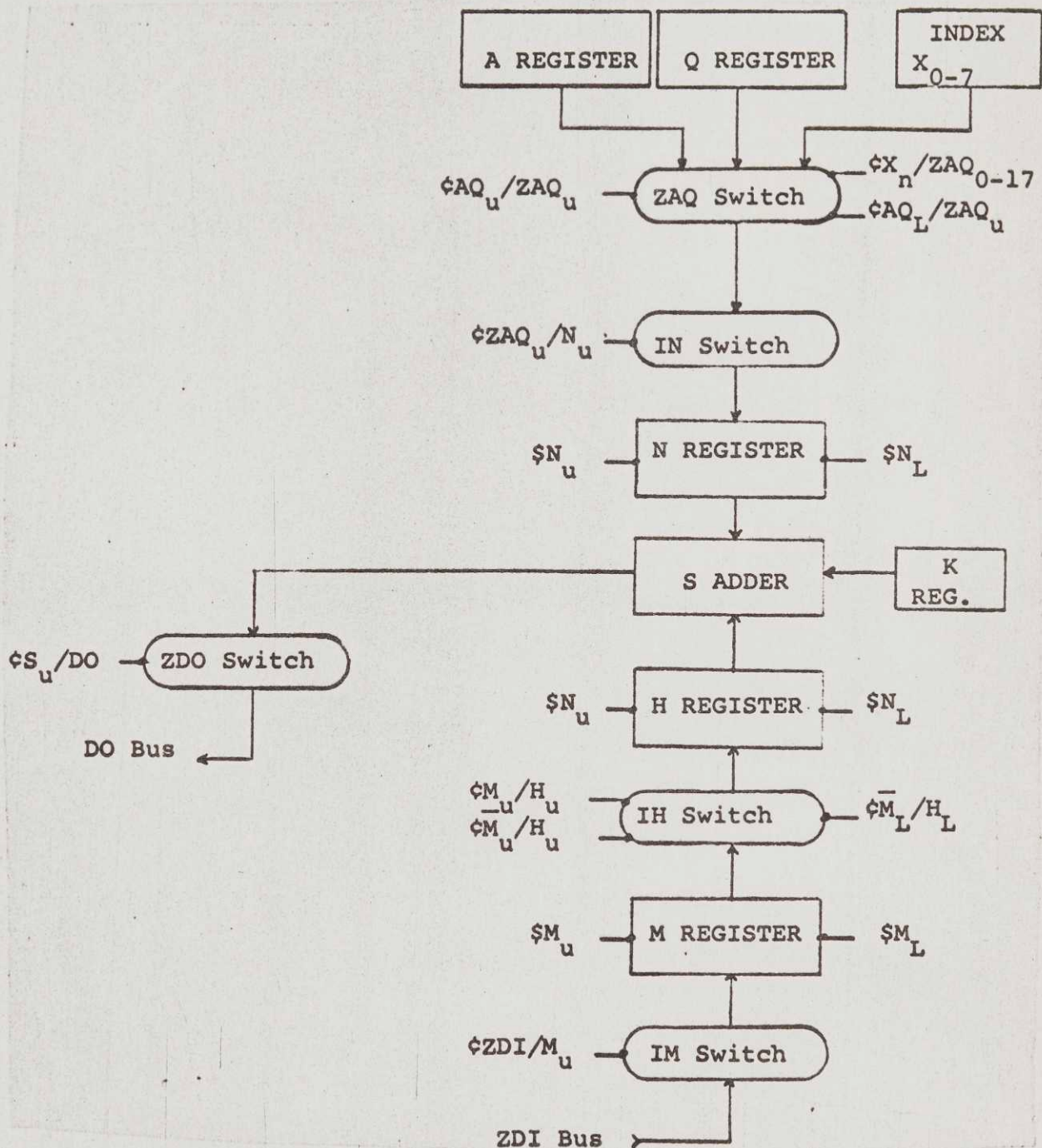


Fig. 12.3.3 Major Data Paths and Control Points for the Read-Alter-Rewrite Group of Instructions (OU)

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12.3.3 - contd

Example 1: Add One to Storage (AOS)

During this instruction the contents of a memory location Y are incremented by one and the results are placed back in Y.

The IM switch is enabled by the presence of the AOS decode together with DPFF, BCFF, and DIC all reset. The control points $\phi ZDI_{0-17}/M_{0-17}$, $\phi ZDI_{18-27}/M_{18-27}$, and $\phi ZDI_{28-35}/M_{28-35}$ are enabled to allow the ZDI bus to be present at the M-register inputs. About the same time that IM is enabled, the IH switch is enabled with $\phi M_{0-35}/H_{0-35}$ and $\phi M_{36-71}/H_{36-37}$. This will allow the memory operand to be present at bits 0-35 of the H-register and all one's at bit positions 36-71. All one's are forced into the lower half of H so that when an add is performed with an initial carry, the carry will ripple down to bit 35 permitting +1 to be added to the memory operand.

\$ set GS generates \$SDY and sends it to the CU as a request for the AOS operand to be retrieved from memory. After about 1100 nanoseconds the operand ready strobe \$DRDY is received from the CU.

The reception of \$DRDY and the double precision flip-flop not set allows the M-register strobe ϕM_{0-71} to be generated and strobe the memory operand into M. \$ START is generated in the normal manner.

GS

When the \$ START pulse propagates the medium delay elements, the operate strobe \$ occurs. This causes the following events:

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GE-645 PROTOTYPE PROCESSOR

12.3.3 - contd

- 1) The GS cycle to reset and the GF cycle to set.
- 2) \$H strobes the memory operand into H (0-35).
All one's are strobed into H (36-71).
- 3) \$N is generated, but since the IN switch is not enabled all zeros are loaded into N.
- 4) The adder carry control flip-flop K_{72} is set.
- 5) The Zero and Sign Indicators are reset.
- 6) The $(\text{RAR} \cdot \text{GS} \cdot \overline{\text{GF}})$ level gates \$ to produce the \$DP strobe. This pulse delayed 350 nanoseconds will be used for the storage of the altered AOS operand in the Data Out Buffer.

GF

When GF set, the control point $\text{cS}_{0-35}/\text{DO}_{0-35}$ became enabled. This permits the adder outputs to be present at the DO bus. The \$DP will strobe the altered word into the Data Out Buffer and will be returned as \$DS. This \$DS will produce a \$ strobe which will:

- 1) Reset the GF cycle.
- 2) Reset the OUB flip-flop if no other instruction has been initiated.
- 3) Set the Zero Indicator if the adder output is zero.

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12.3.3 - contd

- 4) Set the Sign Indicator if bit zero of the adder is a one.
- 5) Set the Carry Indicator if a carry was generated out of bit zero, or reset it if no carry.
- 6) Set the Overflow Indicator if the range of Y is exceeded.
- 7) Reset the K72 carry flip-flop.
- 8) Generate \$ LAST, which is sent to the CU to signal completion of the AOS instruction.

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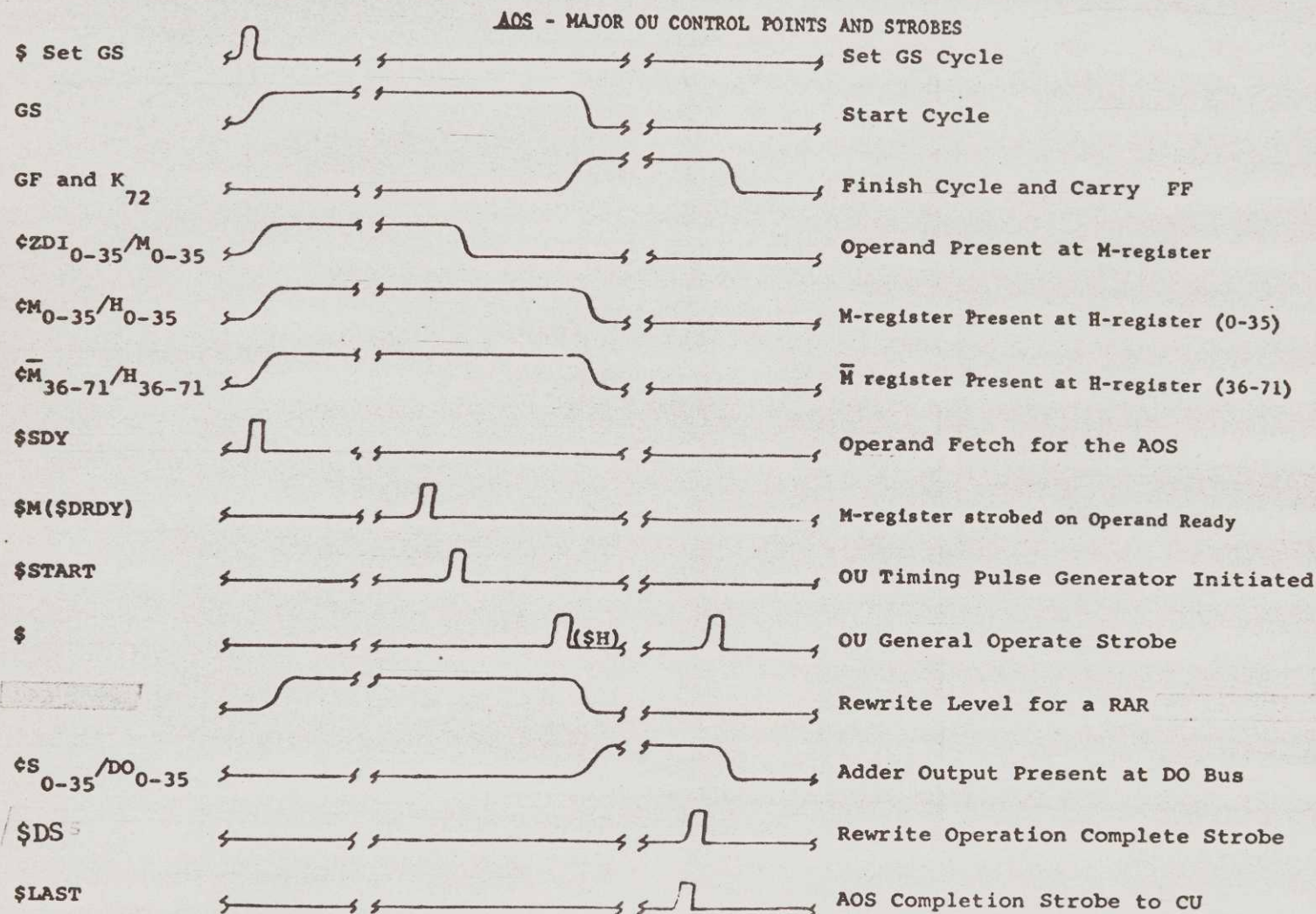


FIG. 12.3.3a AOS Instruction, Timing Diagram

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12.3.3 - contd

Example 2: Exclusive "OR" to Storage Q (ERSQ)

During this instruction the exclusive "OR" function is performed using the contents of a memory location Y and the contents of the Q-register. The results are stored in location Y.

The IM switch is enabled by the presence of the ERSQ decode together with DPFF, BCFF, and DIC all reset. Control points $\phi ZDI_{0-17}/M_{0-17}$, $\phi ZDI_{18-27}/M_{18-27}$, and $\phi ZDI_{28-35}/M_{28-35}$ are enabled to allow the ZDI bus to be present at the M-register inputs. About the same time the IM switch is enabled the IH, ZAQ, and IN switches are enabled. IH is enabled by $\phi M_{0-35}/H_{0-35}$; ZAQ by $\phi AQ_{36-71}/ZAQ_{0-35}$; and IN by $\phi ZAQ_{0-35}/N_{0-35}$. These enabled switches will allow the operands to be present at the H- and N-register inputs.

\$ set GS generates a \$SDY which is sent to the CU as a request for the ERSQ operand to be retrieved from memory. After about 1100 nanoseconds the operand ready strobe \$DRDY is received from the CU.

The reception of \$DRDY and the double precision flip-flop not set allows the M-register strobe ϕM_{0-71} to be generated and strobe the memory operand into M. \$ START is generated in the normal manner.

GS

When the \$ START pulse propagates the medium delay elements, the operate strobe \$ occurs. This causes the following events:

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Spec. No. M50EB00107

Cont. on Sh. 12-90 Sh. No.12-89

TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR

12.3.3 - contd

- 1) The GS cycle to reset and the GF cycle to set.
- 2) \$H strobes the memory operand into H.
- 3) \$N strobes the Q-register operand into N.
- 4) The adder control flip-flop K_1 is set to force an exclusive "OR" to be performed.
- 5) The Zero and Sign indicators are reset.
- 6) The $(RAR \cdot GS \cdot \overline{GF})$ level which is high gates \$ to produce the \$DP strobe. This pulse delayed 350 nanoseconds will be used for the rewrite of the altered ERSQ operand.

GF

When GF set, the control point $\phi S0-35/D00-35$ became enabled. This will allow the adder outputs to be present at the DO bus. The \$DP will strobe the altered word into the Data Out Buffer and will be returned as \$DS.. This \$DS will produce a \$ strobe which will:

- 1) Reset the GF cycle.
- 2) Reset the OUB flip-flop if no other instruction has been initiated.
- 3) Set the Zero Indicator if the adder output is zero.
- 4) Set the Sign Indicator if bit zero of the adder is a one.
- 5) Reset K_1 of the adder control.
- 6) Generates \$ LAST, which is sent to the CU to signal completion of the ERSQ instruction.

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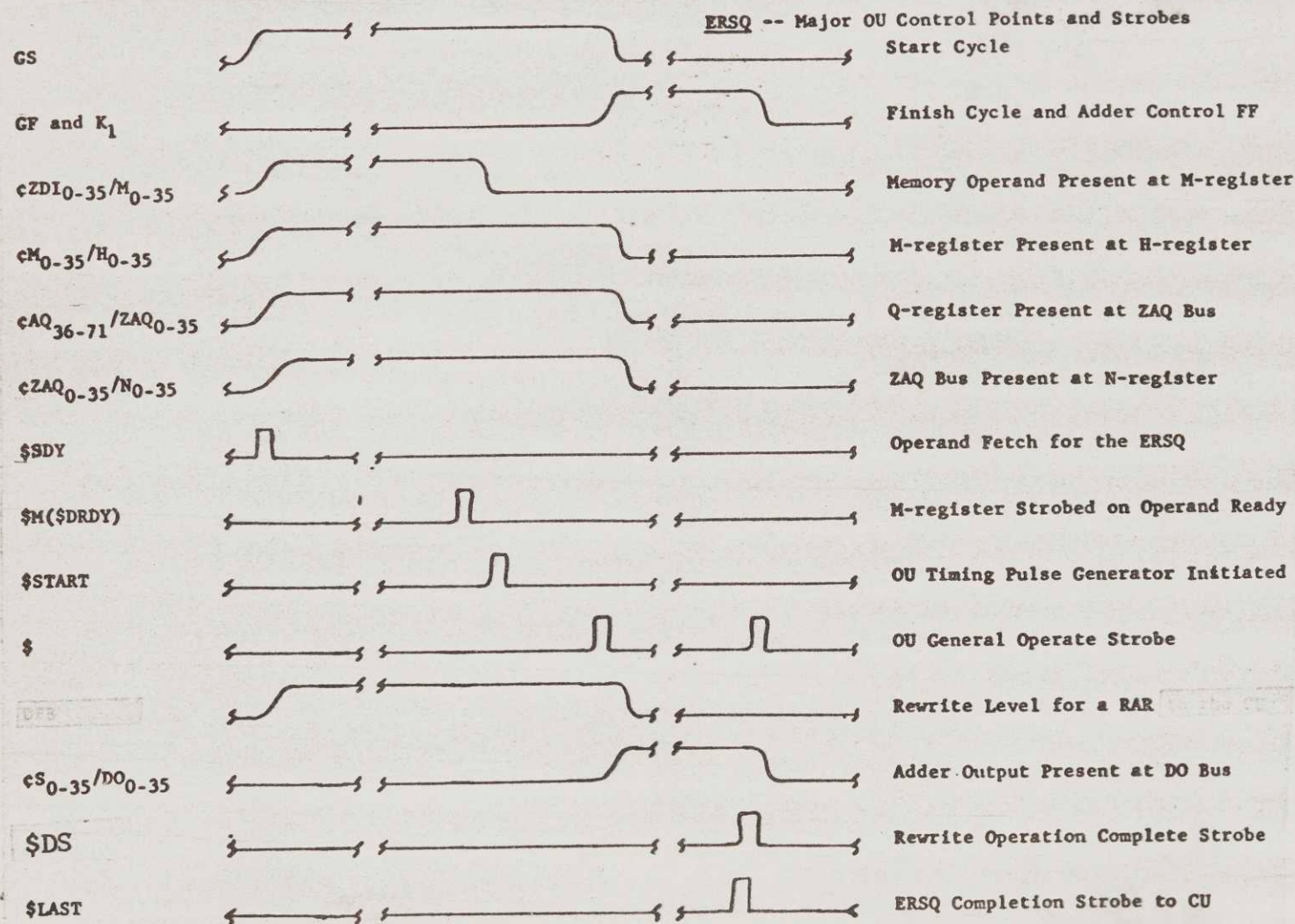


FIG. 12.3.3b EROS Instruction, Timing Diagram

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Spec. No. M50EB00107

Cont. on Sh. 12-92 Sh. No.12-91

TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR

12.3.4 SHIFT GROUP

This group of 12 instructions constitute the controllable shifting capabilities of this machine. These instructions permit left shifts, right shifts, and left rotations of the A-, Q-, or combined AQ-registers with from 0 to 127 bit displacements. Even though shifts of greater than 35 for single precision and shifts of greater than 71 for double precision are generally meaningless, they are allowed by the hardware.

All shifts are performed under control of the OU G-counter* which contains the number of shifts to be executed. The G-counter is loaded with bits 11-17 of the shift operand which specifies the number of shifts. The shift logic is implemented so that shifts of 16, 4, or 1 in that order may be performed during one shift or GO cycle. For each bit shifted, the shift count in G is decremented by one. This continues until the G count is zero. During this shift process there may be a right or left overshift of one bit position. In this event a Reverse flip-flop (REV) is set and the overshifted bit is retained and inserted back into the data word during the GN cycle used for overshift correction.

All shifts are performed by transferring the A-, Q-, or AQ-registers into the N-register and then switching the N-register outputs back into the appropriate inputs in order to accomplish the actual shift. When the shift operation is complete, the results are stored back in the A-, Q-, or AQ-register.

*Refer to paragraph 12.4 for a detailed description of the G-counter.

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Spec. No. M50EB00107

Cont. on Sh.12-93 Sh. No.12-92

TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR

12.3.4 - contd

To illustrate the control used in the execution of these instructions, two instructions will be explained in detail. For the detailed control of all instructions in this group, refer to the OU Specification Chart.

In the explanation of the example instructions, the following conditions will be assumed.

- 1) The instruction has been strobed into the 0-register.
- 2) The GS cycle flip-flop has been set.
- 3) The DDF flip-flop has been set indicating the operation decode has settled.

NOTE: Reference to Fig. 12.3.4 and the partial timing diagram at the end of each example will aid in the understanding of the instruction execution and implementation.

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Cont. on Sh.12-94 Sh. No.12-93

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

C*-N to N Shift Control

1. ϵ_{N-1/N_0}
2. ϵ_{N_0/N_0}
3. $\epsilon_{N_0/N_{0-3}}$
4. $\epsilon_{N_0/N_{0-15}}$
5. $\epsilon_{N_{0-34}/N_{1-35}}$
6. $\epsilon_{N_{0-31}/N_{4-35}}$
7. $\epsilon_{N_{0-19}/N_{16-35}}$
8. $\epsilon_{N_{35-70}/N_{36-71}}$
9. $\epsilon_{N_{32-67}/N_{36-71}}$
10. $\epsilon_{N_{20-55}/N_{36-71}}$
11. $\epsilon_{N_0/N_{35}}$
12. $\epsilon_{N_{0-3}/N_{32-35}}$
13. $\epsilon_{N_{0-15}/N_{20-35}}$
14. $\epsilon_{N_{1-35}/N_{0-34}}$
15. $\epsilon_{N_{4-35}/N_{0-31}}$
16. $\epsilon_{N_{16-35}/N_{0-19}}$
17. $\epsilon_{(N_{36}+N_{36A})/N_{35}}$
18. $\epsilon_{N_{36-39}/N_{32-35}}$
19. $\epsilon_{N_{36-51}/N_{20-35}}$
20. $\epsilon_{N_0/N_{71}}$
21. $\epsilon_{N_{0-3}/N_{68-71}}$
22. $\epsilon_{N_{0-15}/N_{56-71}}$
23. $\epsilon_{N_{37-71}/N_{36-70}}$
24. $\epsilon_{N_{40-71}/N_{36-67}}$
25. $\epsilon_{N_{52-71}/N_{36-55}}$
26. $\epsilon_{N_{72}/N_{71}}$
27. ϵ_{N_{35}/N_0}

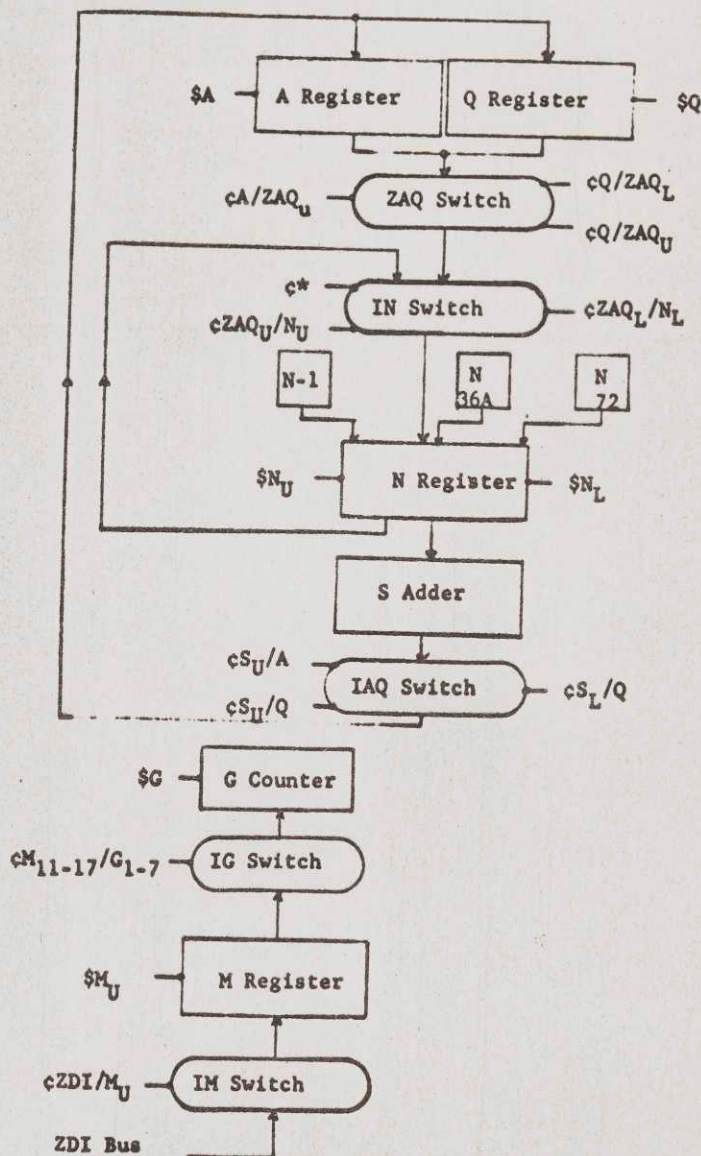


Fig. 12.3.4

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Spec. No. M50EB00107

Cont. on Sh.12-95 Sh. No.12-94

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

12.3.4 - contd

Example 1: A-register Left Shift (ALS)

During this instruction the contents of the A-register will be shifted left the number of positions specified by bits 11-17 of the ALS instruction word. The vacated positions will be filled with zeros and the final result will be placed in A. For this example a shift of 7 will be executed.

The IM switch is enabled by the presence of the ALS decode together with the DPFF, BCFF, and DIC all reset. The control points $\phi ZDI_{0-17}/M_{0-17}$, $\phi ZDI_{18-27}/M_{18-27}$, and $\phi ZDI_{28-35}/M_{28-35}$ are enabled to allow the ZDI bus to be present at the M-register inputs. Shortly after the IM switch is enabled the IG, ZAQ, and IN switches are enabled. IG is enabled by $\phi M_{11-17}/G_{1-7}$; ZAQ by $\phi AQ_{0-35}/ZAQ_{0-35}$; and IN by $\phi ZAQ_{0-35}/N_{0-35}$. These enabled switches allow the operands to be present at the N and G inputs.

When $\$DRDY$ is received from the CU, the double precision flip-flop not being set allows the M-register strobe $\$M_{0-71}$ to be generated and strobe the shift count into M. $\$START$ is generated in the normal manner.

GS

When the $\$START$ pulse propagates the medium delay elements the operate strobe $\$$ occurs. This causes the following events:

- 1) The GS cycle to reset and the GO cycle to set.
- 2) $\$N$ strobes the contents of A into N.
- 3) $\$H$ strobes all zeros into H.

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Spec. No. M50EB00107
Cont. on Sh.12-96 Sh. No.12-95

TITLE: ENGINEERING PRODUCT SPECIFICATIONS
GE-645 PROTOTYPE PROCESSOR

12.3.4 - contd

- 4) \$G strobes the contents of M₁₁₋₁₇ into G₁₋₇ as shown:

G =	0	1	2	3	4	5	6	7
	0	0	0	0	0	1	1	1
	Shift 16				Shift 4		Shift 1	

- 5) The Zero, Sign, and Carry Indicators are all reset.
- 6) The \$ strobe re-enters the Timing Pulse Generator delay line network to produce another \$ strobe in approximately 200 nanoseconds.

(GO) (G = 7)

During this 200-nanosecond interval the first fast GO cycle is true and the control points are set up to execute the first shift. The G contents call for one (01)₂ shift of 4 and three (11)₂ shifts of 1. The greater shifts are executed first, so the shift of 4 will occur during this first GO cycle. The control point enabled for this is $\phi N_{4-35}/N_{0-31}$. This control will allow bits 4-35 of N to be switched into bit positions 0-31 of N on the next \$N. Since the inputs to N₃₂₋₃₅ will not be true at this time, zeros will be forced into the lower 4-bit positions of N.

When the \$ strobe does occur at the end of this first GO cycle, the following events occur:

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Spec. No. M50EB00107

Cont. on Sh. 12-97 Sh. No. 12-96

TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR

12.3.4 - contd

- 1) \$N strobes the N-register inputs and performs the shift of 4.
- 2) \$G decrements the G-counter by 4.
- 3) The Carry Indicator will set if all of the 4-bits shifted out of N were not alike.
- 4) The GO cycle will be strobed but will remain set because the G count indicates another GO cycle is necessary.
- 5) The \$ pulse will re-enter the Timing Pulse Generator delay line network to produce another \$ in about 200 nanoseconds.

(GO) (G = 3)

During this 200 nanosecond interval the second GO cycle is true and the control points are set up to execute the second shift. At this time the G-counter still has bits 6 and 7 true which call for three shifts of 1. The shift control logic is set up in such a manner that a shift of 3 will be done by a shift of 4 and a reverse shift of 1. This speeds up the over-all shift by one cycle. The control point again enabled is $\phi N_{4-35}/N_{0-31}$ which is the same control used for the first shift of 4. The set reverse control line comes high by the decode of (G count = 3) (GO) (ALS) and sets up the necessary condition for terminating the GO cycle and entering the GN cycle.

When the \$ strobe occurs at the end of the second GO cycle, the following events occur:

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Spec. No. M50EB00107
Cont. on Sh. 12-98 Sh. No. 12-97

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

12.3.4 - contd

- 1) \$N strobes the N-register inputs and performs the shift of 4.
- 2) \$G decrements the G-counter to zero by resetting G_6 and G_7 .
- 3) The Carry Indicator will set if any of the 4-bits shifted out of N are not all the same (zeros or ones) and it was not set during the first GO cycle.
- 4) The N_{-1} flip-flop is set or reset depending on whether N_3 was a one or a zero. This will later control the sign of N when the overshift correction is done and N_{-1} is restored to the N_0 position.
- 5) The GO cycle is reset and the GN cycle set.
- 6) The \$ strobe will re-enter the Timing Pulse Generator to produce another \$ in about 200 nanoseconds.
- 7) The reverse flip-flop (REV) is set.

GN

During the GN cycle the control points are set up to execute the overshift correction. For this case the correction is a right shift of one and the insertion of the overshifted bit contained in N_{-1} back into N_0 . The control points enabled are $\phi N_0-31/N_1-35$ and $\phi N_{-1}/N_0$.

When the \$ strobe occurs at the end of the GN cycle, the following events occur:

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Spec. No. M50EB00107

Cont. on Sh.12-99 Sh. No.12-98

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

12.3.4 - contd

- 1) \$N strobes the N-register inputs and performs a right shift of one and pulls in bit zero.
- 2) The Reverse flip-flop (REV) is reset.
- 3) The GN cycle is reset and the GF cycle is set.
- 4) The \$ strobe is re-enter the Timing Pulse generator to produce another \$ in about 400 nanoseconds.

GF

At this point the shift is complete and all that remains is to restore the shifted operand back to A-register. This restore is done via the S-adder. The IAQ switch control enabled is $\phi S_0-35/AQ_0-35$. When the \$ strobe occurs at the end of GF, the following events occur:

- 1) \$AQ0-35 restores the shifted A operand.
- 2) The Zero Indicator is set if the contents of $A = 0$.
- 3) The Sign Indicator is set if bit zero of $A = 1$.
- 4) The GF cycle is reset.
- 5) It generates \$ LAST, which is sent to the CU to signal completion of the ALS instruction.

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Spec. No. M50EB00107

Cont. on Sh. 12-100sh. No. 12-99

TITLE:

ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

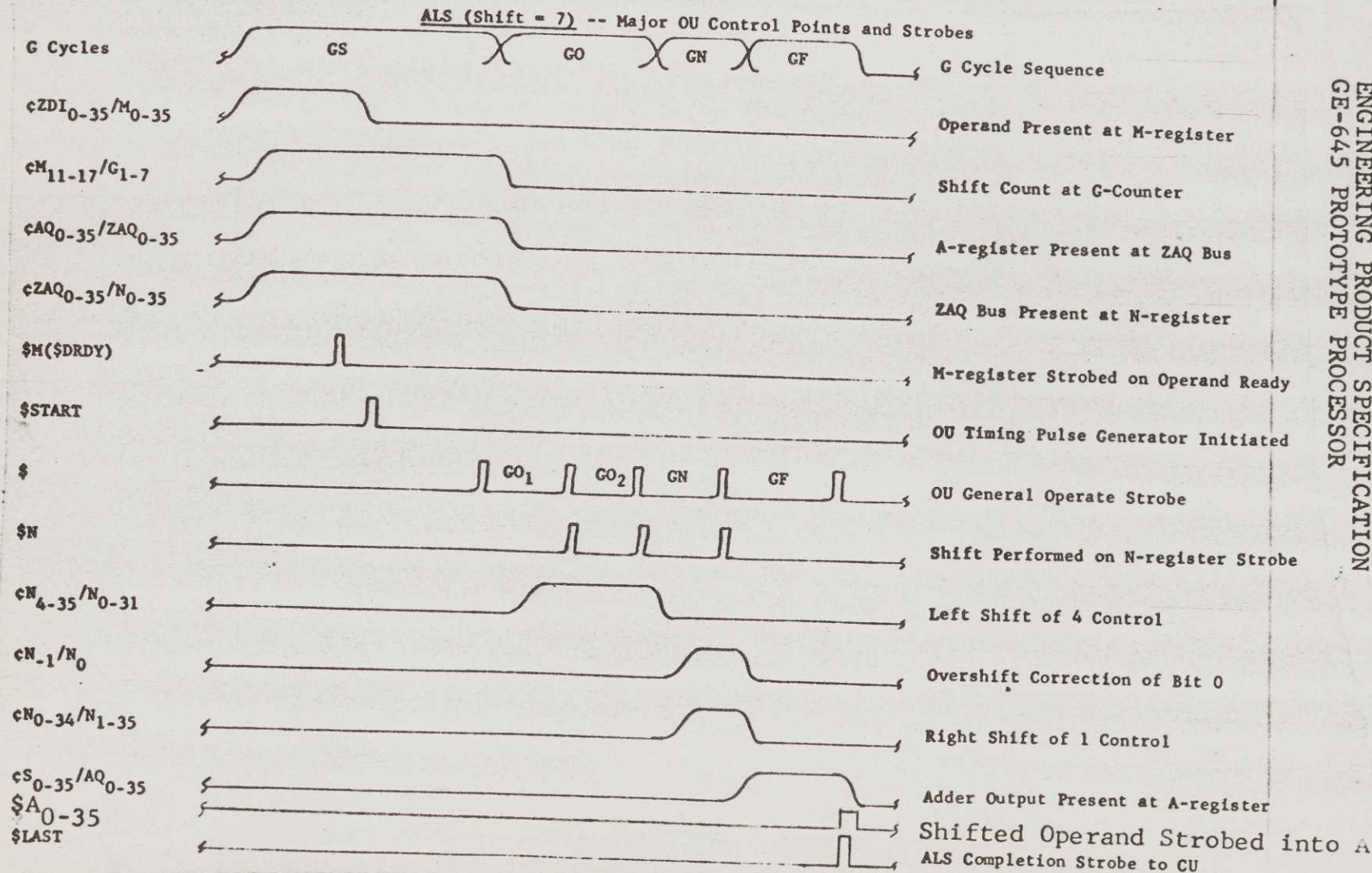


FIG. 12.3.4a ALS Instruction, Timing Diagram

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Spec. No. M50EB00107

Cont. on Sh.12-101 Sh. No.12-100

TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR

12.3.4 - contd

Example 2: Left Rotate the AQ (LLR)

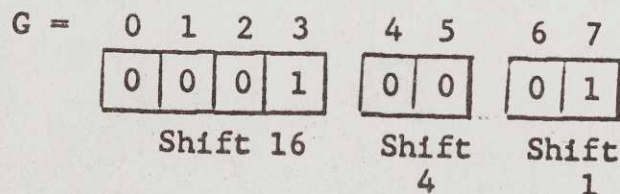
During this instruction the contents of the AQ-register are rotated out the left and in on the right by the amount specified in bits 11-17 of the LLR instruction word. The results are restored to AQ. For this example a rotation of 17 places will be executed.'

ZDI/M controls and \$ START generation are the same as for Example 1.

GS

When the \$ START pulse propagates the medium delay elements the operate strobe \$ occurs. This causes the following events:

- 1) The GS cycle to reset and the GO cycle is set.
- 2) \$N strobes the contents of AQ into N.
- 3) \$H strobes all zeros into H.
- 4) \$G strobes the contents of M₁₁₋₁₇ into G₁₋₇ as shown:



- 5) The Zero and Sign Indicators are reset.
- 6) The \$ strobe re-enters the Timing Pulse Generator to produce another \$ strobe in approximately 200 nanoseconds.

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Spec. No. M50EB00107

Cont. on Sh.12-102 Sh. No.12-101

TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR

12.3.4 - contd

(GO) (G = 17)

During this 200-nanosecond interval the first fast GO cycle is true and the control points are set up to execute the first rotation. The G contents call for one rotation of 16 and one rotation of 1. The greater rotations are executed first, so the rotation of 16 will occur during this first GO cycle. The control points enabled for this are $\phi N_0-15/N_{56-71}$, $\phi N_{16-35}/N_{0-19}$, $\phi N_{36-51}/N_{20-35}$ and $\phi N_{52-71}/N_{36-55}$. This control will allow a left rotation on N by 16 positions on the next \$N strobe.

On the \$ strobe at the end of this first GO cycle, the following events occur:

- 1) \$N strobes the N-register inputs and performs the rotation of 16.
- 2) \$G decrements the G-counter by 16.
- 3) The GO cycle will be strobed but will not reset because the G count indicates another GO cycle is necessary.
- 4) The \$ pulse will re-enter the Timing Pulse Generator to produce another \$ in about 200 nanoseconds.

(GO) (G = 1)

During this second GO cycle the control is set up to execute the second rotation. At this time the G-counter has bit 7 true which calls for one rotation of 1. The control points enabled are $\phi N_0/N_{71}$, $\phi N_{1-35}/N_{0-34}$, $\phi(N_{36} + N_{36A})/N_{35}$ and $\phi N_{37-71}/N_{36/70}$. This control will allow a left rotation of N by 1 bit on the next \$N strobe.

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Spec. No. M50EB00107

Cont. on Sh.12-103 Sh. No.12-102

TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR

12.3.4 - contd

When the \$ strobe occurs at the end of the second GO cycle, the following events occur:

- 1) \$N strobes the N-register inputs and performs the rotation of 1.
- 2) \$G decrements the G-counter to zero by resetting G₇.
- 3) The GO cycle is reset and the GF cycle set.
- 4) The \$ strobe will re-enter the Timing Pulse Generator to produce another \$ in about 400 nanoseconds.

GF

At this point the rotation is complete and all that remains is to restore the rotated operand back to the AQ-register. This restore is done via the S-adder. The IAQ switch control enabled is $\phi S_{0-35}/AQ_{0-35}$ and $\phi S_{36-71}/AQ_{36-71}$. When the \$ strobe occurs at the end of GF, the following events occur:

- 1) \$AQ₀₋₇₁ restores the rotated AQ operand.
- 2) The Zero Indicator is set if the contents of AQ = 0.
- 3) The Sign Indicator is set if bit zero of AQ = 1.
- 4) The GF cycle is reset.
- 5) It generates \$ LAST, which is sent to the CU to signal completion of the LLR instruction.

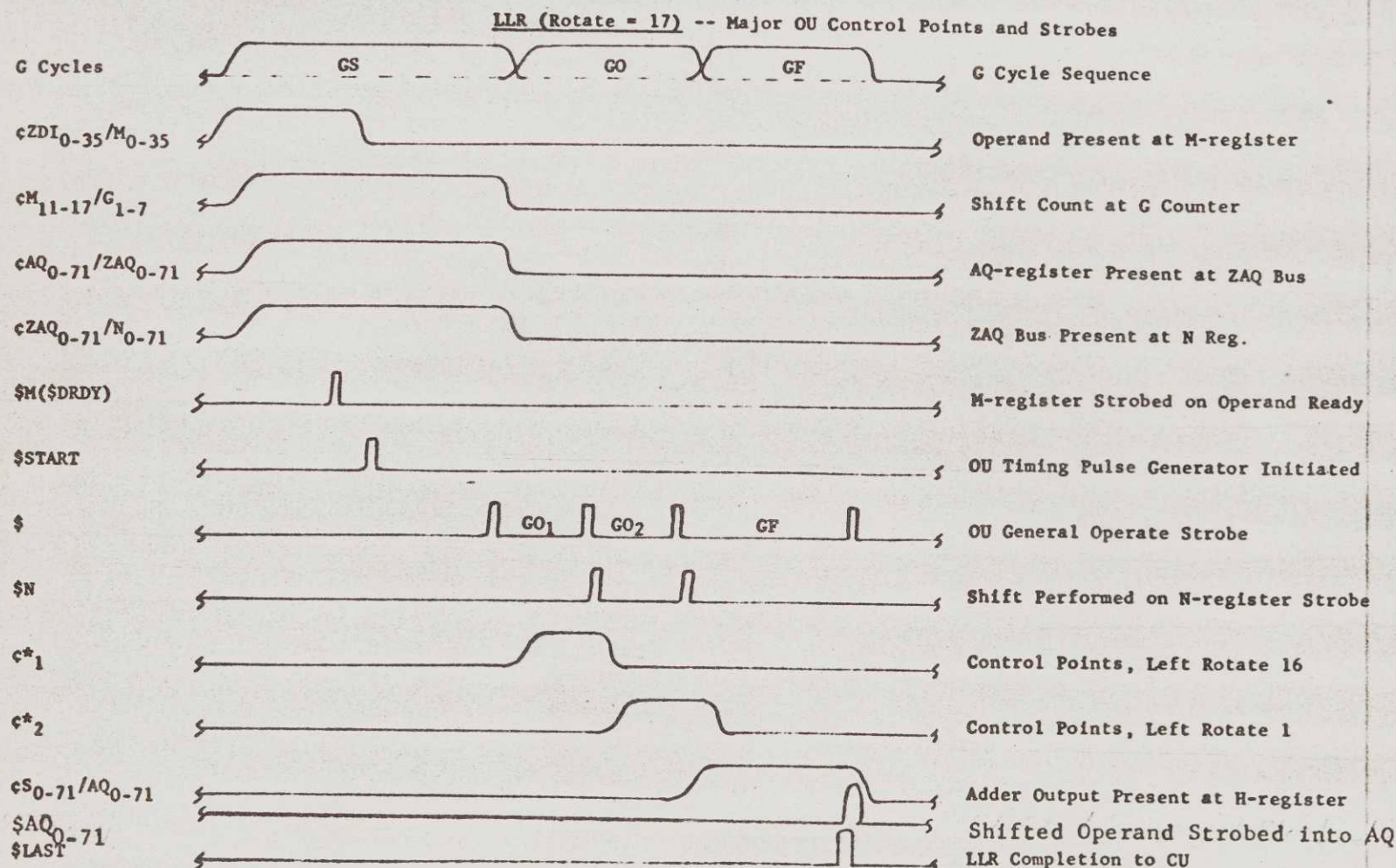
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Spec. No. M50EB00107

Cont. on Sh.12-104 Sh. No.12-103

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR



*₁ = cN_{0-15}/N_{56-71} ; cN_{16-35}/N_{0-19} ; cN_{36-51}/N_{20-35} ; cN_{52-71}/N_{36-55}

*₂ = cN_{1-35}/N_{0-34} ; cN_{37-71}/N_{36-70} ; cN_0/N_{71} ; $c(N_{36} + N_{36A}/N_{35})$

FIG. 12.3.4b LLR Instruction, Timing Diagram

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Spec. No. M50EB00107

Cont. on Sh.12-105 Sh. No.12-104

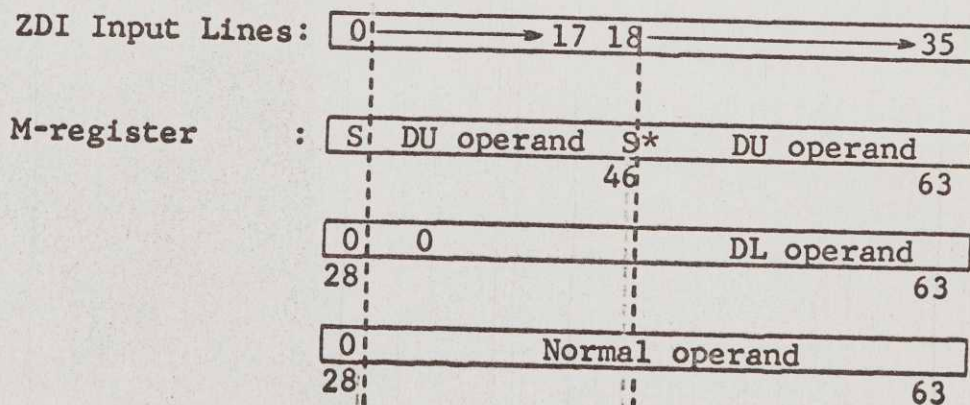
TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR

12.3.5 FIXED POINT MULTIPLY GROUP

This group of two instructions provide the fixed point multiply capabilities of this machine. The major data paths and control points for these instructions are shown in Fig. 12.3.5.

The instructions MPY and MPF allow integer and fractional multiplication to be accomplished. For either instruction, a 36-bit (including sign) multiplicand is multiplied by a 36-bit (including sign) multiplier. When a Direct Upper (DU) operand is specified, the multiplier consists of the direct operand in bits 0-17 and zeros in bits 18-35. A Direct Lower (DL) modifier results in a multiplier with zeros in bits 0-17 and the DL operand in bits 18-35. The multiplicand is contained in the A-register for MPF and in the Q-register for MPY. For either instruction, the multiplier is contained in the M-register and is always right justified to bit 63 of the M-register. The partial products are accumulated in the H-register and the final 72-bit product is restored to the combined AQ-register.

The possible multiplier configurations which may be contained in the M-register with respect to the ZDI lines from the Base Frame are shown below:



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PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh.12-106 Sh. No.12-105

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

Major Data Paths and Control Points for the Fixed Point
Multiply Instructions (OU)

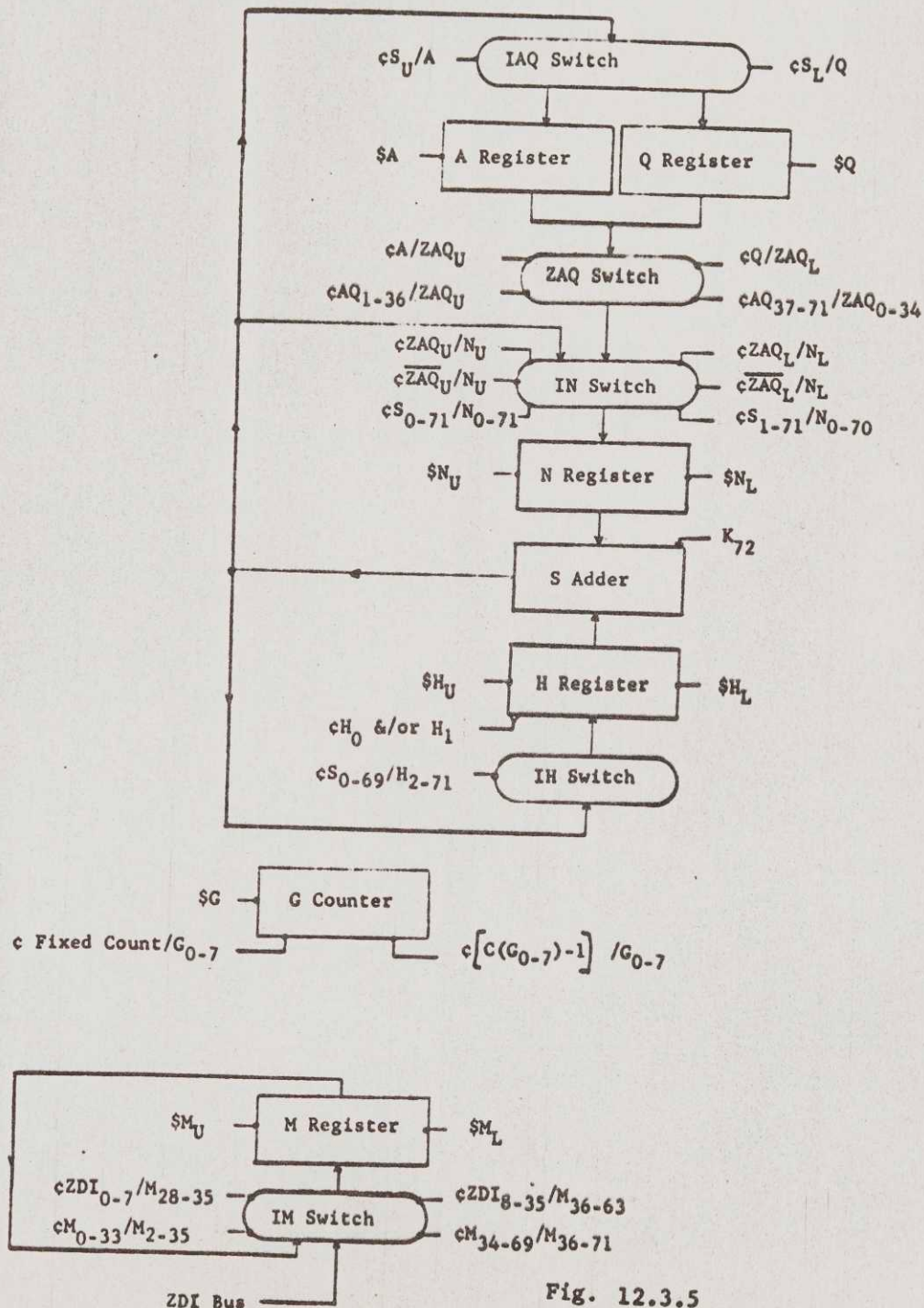


Fig. 12.3.5

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

12.3.5 - contd

When the multiplier is specified by a Direct Upper tag, the number of multiply cycles will be nine less than for those multipliers which are not Direct Upper. This results from the fact that for a Direct Upper multiplier the lower half of the 36-bit word is zero. The multiply algorithm used would result in nine passes or multiplications by zero for these 18 bits. To speed up the multiply in this case, the multiplications by zero are bypassed and only the meaningful 18 or Direct Upper bits are used to perform the multiply. For control convenience in the CU, a DU operand is placed on both the 0-17 and 18-35 output bit positions. This does not affect the OU because only bits 18-35 are used.

When the multiplier is specified by a Direct Lower tag, the upper 18 bits of a 36-bit word will be zero. No speed-up technique is employed in this case and the number of multiply cycles is 19. A Direct Lower multiplier will always be a positive number.

For the detailed control of both instructions in this group, refer to the OU Specification Chart 43D140232, page 8.

In the explanation of all the example instructions, the following conditions will be assumed:

- 1) The instruction has been strobed into the 0 register.
- 2) The GS cycle flip-flop has been set.
- 3) The DDF flip-flop has been set indicating the operation decode has settled.

NOTE: Reference to Fig. 12.3.5 and the partial timing diagram at the end of the example will aid in the understanding of the instruction execution and implementation.

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Spec. No. M50EB00107

Cont. on Sh.12-108 Sh. No.12-107

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

12.3.5 - contd

Example 1: Fractional Multiply (MPF)

During this instruction, the contents of the A-register are multiplied by the contents of a memory location Y to produce a 71-bit fractional product plus sign which is stored in the AQ-register. Bit position 71 of the AQ product will contain a zero. For this example, no operands are used but all major controls are explained.

The IM switch is enabled by the presence of the MPF decode together with DIC and DPFF reset. The control points cZDI0-7/M28-35 and cZDI8-35/M36-63 are enabled to allow the ZDI bus to be present at the M-register inputs. When the operand ready strobe $\text{\$DRDY}$ is received from the CU, the Double Precision flip-flop not being set allows the M-register strobe $\text{\$M0-71}$ to be generated and strobe the multiplier into the M-register. See page 12-104 for the possible arrangements of the multiplier. If the multiplier operand being furnished by the CU is a Direct Upper, $\text{\$DMF}$ will be received from the CU at the same time as $\text{\$DRDY}$. $\text{\$DMF}$ will set the Direct Upper Multiplier flip-flop (DUM). The $\text{\$DRDY}$ strobe is turned around as $\text{\$YRY}$ and returned to the CU to signal that a new instruction may be prepared. $\text{\$YRY}$ also sets the operand ready flip-flop, and with the MPF decode sets the M-register is busy with a multiply flip-flop (DIC). The DIC flip-flop is used as an inhibit on the ZDI/M controls for the duration in which the multiplier is contained in the M-register.

GS

During the 320 nanoseconds of GS from $\text{\$ START}$ to the first $\text{\$}$, the control is established to load the G-counter with the proper count on the first $\text{\$}$. If DUM is set (which defines the multiplier as a DU, Fixed Count/G control will force a count of 10 into G (that is, set G_4 and G_6). If DUM is reset, a count of 19 is placed in G (that is, set G_3 , G_6 , and G_7).

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GENERAL ELECTRIC COMPANY
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PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh.12-109 Sh. No.12-108

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

12.3.5 - contd

As per the multiply algorithm, the low-order two bits of the multiplier M_{62-63} are decoded during this same 320 nanoseconds of GS to indicate whether the first multiplication will be by 0, 1, 2, or 3. The decode of M_{62-63} is interpreted as:

- 1) If $M_{62-63}=00$, this represents multiplication by zero or a pass condition (that is, no modification of the partial product in H which at this time is zero). No ZAQ or IN switch is enabled.
- 2) If $M_{62-63}=01$, this represents multiplication of the multiplicand by one. Since at this time there is no partial product, the multiplicand will become the first partial product. To accomplish this, the ZAQ and IN switches are enabled by $\bar{c}AQ_{0-35}/ZAQ_{0-35}$ and $\bar{c}ZAQ_{0-35}/N_{0-35}$. These enabled switches allow the A-register multiplicand to be present at the N-register inputs.
- 3) If $M_{62-63}=10$, this represents multiplication of the multiplicand by two. For a binary number this may be done by shifting the number left by one bit position. To accomplish this, the ZAQ and IN switches are enabled by $\bar{c}AQ_{1-36}/ZAQ_{0-35}$ and $\bar{c}ZAQ_{0-35}/N_{0-35}$. The control input to N_{35} is forced to be a zero at this time so that the effective AQ/N transfer will be AQ_{1-35}/N_{0-34} .
- 4) If $M_{62-63}=11$, this represents multiplication of the multiplicand by three. This is accomplished by doing a multiply of $(4-1=3)$. The multiply by 4 is accomplished by adding one to the bit which will be contained in M_{63} during the next multiply cycle. Effectively, this means that the bits presently contained in M_{60-61} are to be incremented by one. The minus one control is set up during the present multiply cycle (GS) and is performed by subtracting the contents of A from the partial product. The ZAQ and IN switches are enabled by $\bar{c}AQ_{0-35}/ZAQ_{0-35}$, $dZAQ_{0-35}/N_{0-35}$ and $\bar{c}ZAQ_{36-71}/N_{36-71}$. These switches present the one's complement of the A-register to N_{0-35} and all ones are present at the N_{36-71} inputs.

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PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh.12-110 Sh. No.12-109

TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR

12.3.5 - contd

Because a new set of multiplier bits will be needed for the next multiply cycle (the first GO cycle), the control is set up to allow a right shift of the M-register by two. The IM switch is enabled by $\phi M_{0-33}/M_{2-35}$ and $\phi M_{34-69}/M_{36-71}$ to accomplish this right shift.

When the \$ START pulse propagates the medium delay elements, the first operate strobe \$ occurs. This allows the following events:

- 1) The GS cycle to reset and the GO cycle to set.
- 2) The Zero and Sign Indicators to reset.
- 3) \$G is generated which strobes the count of 10 or 19 into the G-counter depending on the control lines enabled.
- 4) \$M is generated which strobes the M-register and executes a right shift of two to set up a new set of multiplier bits.
- 5) \$H is generated which strobes the H-register, but since no IH switch is enabled at this time, all zeros are loaded into H.
- 6) \$N is generated which strobes the N-register and sets up the data to produce the first partial product in the adder. The data loaded into N depends on which controls were enabled from A into N as a function of the first set of M_{62-63} bits.
- 7) The K_{72} adder control flip-flop and String flip-flop (STFF) are set if the first M_{62-63} set were 11₂ which called for a multiplier of 3.
- 8) The PASS flip-flop is set if the first M_{62-63} set were 00₂.

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GENERAL ELECTRIC COMPANY
COMPUTER EQUIPMENT DEPARTMENT
PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh.12-111 Sh. No.12-110

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

12.3.5 - contd

- 9) The Partial Product Sign flip-flop (PPS) has the contents of A_0 strobed into it if a multiplier of 1 or 2 was called for, has $\bar{A}_0$ strobed in if the multiplier were 3, or is left unchanged if the multiplier was zero.
- 10) The $\$$ strobe re-enters the Timing Pulse Generator delay line network to produce another $\$$ strobe in about 320 nanoseconds.

(GO) $G > 3$

During this 320 nanosecond time the first GO cycle is true and the S-adder is used to produce the first partial product and make it available on the S bus at the adder output. While this partial product is being developed, the control points are established to store the partial product on the S bus into H and set up the control to perform the next 2-bit multiplication.

During the GO cycles, the determination of what the next effective multiplier will be is not only a function of M_{62-63} as it was in GS, but it is also dependent on the state of the String flip-flop (STFF). Although there are still only four possibilities for a multiplier, there are now two conditions that cause each possibility. These are shown in truth table form:

M_{62}	M_{63}	STFF	Effective Multiplier
0	0	0	0
0	1	0	+1
1	0	0	+2
1	1	0	3 (or -1)
0	-	1	+1
0	1	1	+2
1	0	1	3 (or -1)
1	1	1	0

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COMPUTER EQUIPMENT DEPARTMENT
PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh.12-112 Sh. No.12-111

TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR

12.3.5 - contd

The control points enabled as a function of the effective multiplier are the same as the ones mentioned during GS when the multiplier was 0, 1, 2, or 3.

The IH switch is enabled during GO to allow the partial product to be strobed into H. The control points for this during GO are $\phi S_0-33/H_2-35$ and $\phi S_{34-69}/H_{36-71}$. Refer to paragraph 3.1.

During this GO cycle, the controls on the IM switch are again enabled to allow the M-register to be right shifted by two in order to have a new set of multiplier bits for the next cycle. The Full Counter Decrement control (ϕFCD) becomes enabled so that the next \$G will decrement the count by one.

When the first \$\$ strobe propagates the medium delay elements, the second \$ is distributed to the OU to end the first GO cycle and the following events occur:

- 1) The GO flip-flop is strobed, but because the G count is not zero it remains set.
- 2) \$G decrements the G-counter by one.
- 3) \$M strobes the M-register and sets in a new pair of multiplier bits.
- 4) \$H strobes the partial product into H_2-71 . The content of the Partial Product Sign flip-flop (PPS) is strobed into H_0 unconditionally and into H_1 if no overflow occurred.

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GENERAL ELECTRIC COMPANY
COMPUTER EQUIPMENT DEPARTMENT
PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh.12-113 Sh. No.12-112

TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR

12.3.5 - contd

- 5) \$N strobes the new premultiplied multiplicand in the N-register as determined by the multiplier decode.
- 6) The K₇₂ adder control flip-flop and the String flip-flop (STFF) are set if the effective multiplier is 3. STFF is reset if the effective multiplier is +1, +2, or ± 2 and not changed if it is zero. K₇₂ is reset for values of other than 3.
- 7) The PASS flip-flop is set for an effective multiplier of zero, or reset for 1, 2, or 3.
- 8) The PPS flip-flop is strobed and sets or resets for the same conditions listed at the end of GS.
- 9) The \$ strobe re-enters the Timing Pulse Generator delay line network to produce another \$ strobe in about 320 nanoseconds.

Up until the time when the G-counter is decremented to a count of 3, the functions performed during all of the G0 cycles are iterative of the first G0 cycle.

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GENERAL ELECTRIC COMPANY
COMPUTER EQUIPMENT DEPARTMENT
PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh.12-114 Sh. No.12-113

TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR

12.3.5 - contd

(GO) (G = 3)

During the GO cycle when $G = 3$, the next to last partial product is formed in the S-adder, and the last multiplicand is prepared for addition to the partial product during $G = 2$ time. The conditions to enable control points during $G = 3$ are the same as those used for $G > 3$ with these exceptions:

- 1) For the decode of $M_{62-63} = 102$ and $STFF = 0$ (multiplier = ± 2), two times the multiplicand is prepared for subtraction from the partial product during $G = 2$. This necessitates that $\phi ZAQ_{0-35}/N_{0-35}$ and $\phi ZAQ_{36-71}/N_{36-71}$ be enabled and the control to set K_{72} must be enabled.
- 2) When $G = 3$, a level resets the DIC flip-flop and frees the M-register.
- 3) The control on the set/reset of PPS is not a function of the (± 2) multiplier.
- 4) The set/reset control of STFF is not a function of any multiplier.

When the \$ pulse is generated at the end of $G = 3$, the same strobes occur as for $G > 3$ with the exception of \$M. \$M is not produced because the multiplier in M has been exhausted by this time. The String flip-flop (STFF) is unconditionally reset at this time. This strobe decrements the G count to 2 and the multiply continues.

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COMPUTER EQUIPMENT DEPARTMENT
PHOENIX, ARIZONA

Spec. No. M50EB00107
Cont. on Sh.12-115 Sh. No.12-114

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

12.3.5 - contd

(GO) (G = 2)

During $G = 2$, the final partial product is formed in the S-adder as a function of the former partial product in H and the multiplier controlled multiplicand in N. Because this will be the last add cycle, no control points are enabled to load a new multiplicand into N on the strobe at the end of $G = 2$.

When the \$ pulse is generated at the end of $G = 2$, the same strobes are produced that occurred at the end of $G = 3$. Because no switches are enabled into N, this register is cleared to all zeros. The K_{72} flip-flop is unconditionally reset and the G count is decremented to one. ~~additionally reset and the G~~

(GO) (G = 1)

During $G = 1$ the final fractional product is contained in the H_{1-71} register with the binary point to the right of H_1 . The control is set up to transfer H_{1-71} to N_{0-70} and thereby place the binary point to the right of N_0 . The control point enabled for this is $\phi S_{1-71}/N_{0-70}$. When the \$ pulse is generated at the end of $G-1$, the following events occur:

- 1) The GO cycle is reset and the GF cycle set.
- 2) \$N transfers the product with a left shift of one from H via S adder to N. N_{71} is cleared to zero.
- 3) \$G decrements the G count to zero.
- 4) The Sign Indicator is set if $S_0 = 1$.
- 5) The Zero Indicator is set if the adder output is zero.
- 6) The Overflow Indicator is set if bit S_0 and S_1 are different.
- 7) The \$ strobe re-enters the Timing Pulse Generator delay line network to produce the last \$ strobe in about 400 nanoseconds.

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GENERAL ELECTRIC COMPANY
COMPUTER EQUIPMENT DEPARTMENT
PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh.12-116 Sh. No.12-115

TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR

12.3.5 - contd

GF

During GF the control points are enabled to transfer the contents of N to AQ. This is done via the adder and IAQ switch with $\phi S_{0-35}/AQ_{0-35}$ and $\phi S_{36-71}/AQ_{36-71}$.

When the \$ strobe occurs, the following events occur:

- 1) The GF cycle is reset.
- 2) The product is strobed into AQ.
- 3) It generates \$ LAST, which is sent to the CU to signal completion of the MPF instruction.

The execution of MPY is the same as MPF except that the multiplicand is contained in the Q-register, and during the $G = 1$ or product alignment cycle, the product is already correctly aligned with the binary point to the right of H_{71} . Therefore, the contents of H_{0-71} is transferred directly to N_{0-71} via the adder with no shift.

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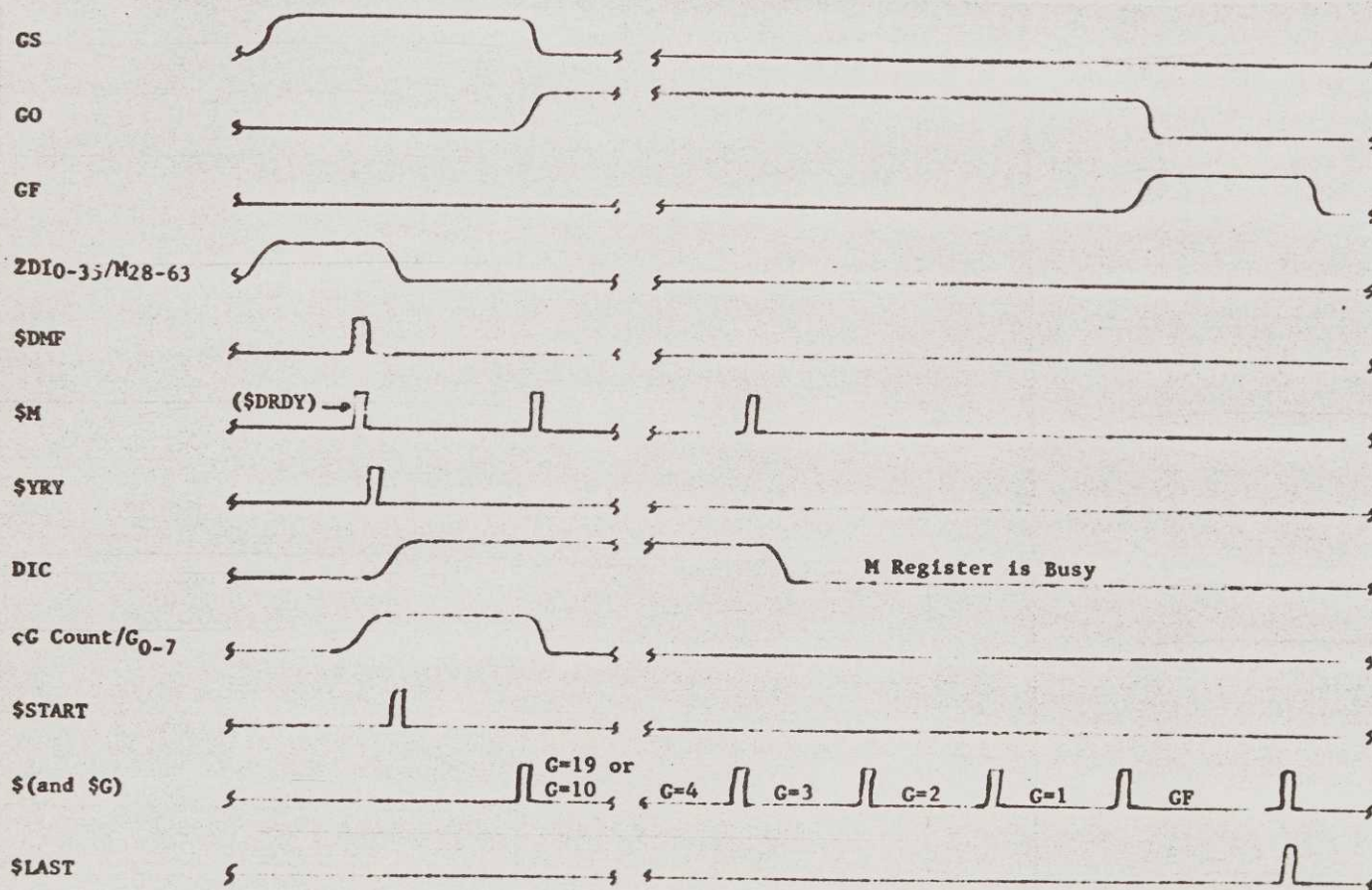
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PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh.12-117 Sh. No.12-116

TITLE:

ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR



MPF - - Major OU Control Points and Strobes (Part 1)

FIG. 12.3.5a MPF Instruction, Timing Diagram
(Sheet 1 of 2)

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Cont. on Sh.12-118 Sh. No.12-117

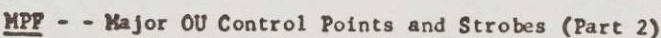
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GE-645 PROTOTYPE PROCESSOR

FIG. 12.3.5a MPF Instruction, Timing Diagram
(Sheet 2 of 2)

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COMPUTER EQUIPMENT DEPARTMENT
PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh.12-119 Sh. No.12-118

TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR

12.3.6 FIXED POINT DIVIDE GROUP

This group of two instructions provides the fixed point divide capabilities of this machine. The major data paths and control points for these instructions are shown in Fig. 12.3.6. The instructions DIV and DVF allow integer and fractional division to be accomplished. A 36-bit divisor is divided into a 36-bit dividend for DIV or into a 71-bit dividend for DVF to produce a 36-bit quotient plus a 36-bit remainder. The dividend is contained in Q for DIV or AQ for DVF, the divisor is contained in H after the initial load, and the quotient and remainder are stored in the AQ-register.

DVF

Whenever performing fractional division the dividend and divisor must be less than unity and the resulting quotient must also be less than unity. Division by zero also is an invalid operation.

$$\frac{\cdot X}{\cdot Y} \geq 1 \text{ not valid}$$

$$\frac{\cdot X}{\cdot Y} \leq 1 \text{ is valid}$$

$$\frac{\cdot X}{0-0} \text{ not valid}$$

Detection of either of two invalid magnitude conditions will immediately abort the divide execution and result in an entry into the Divide Check Fault routine.

A quotient of $+2^{35}$ is not permitted since Q-register capacity is $(2^{35}-1)$. Although a quotient of -2^{35} could be represented with the 36-bit word size, for hardware simplification this is not allowed.

The data format for some of these quantities are:

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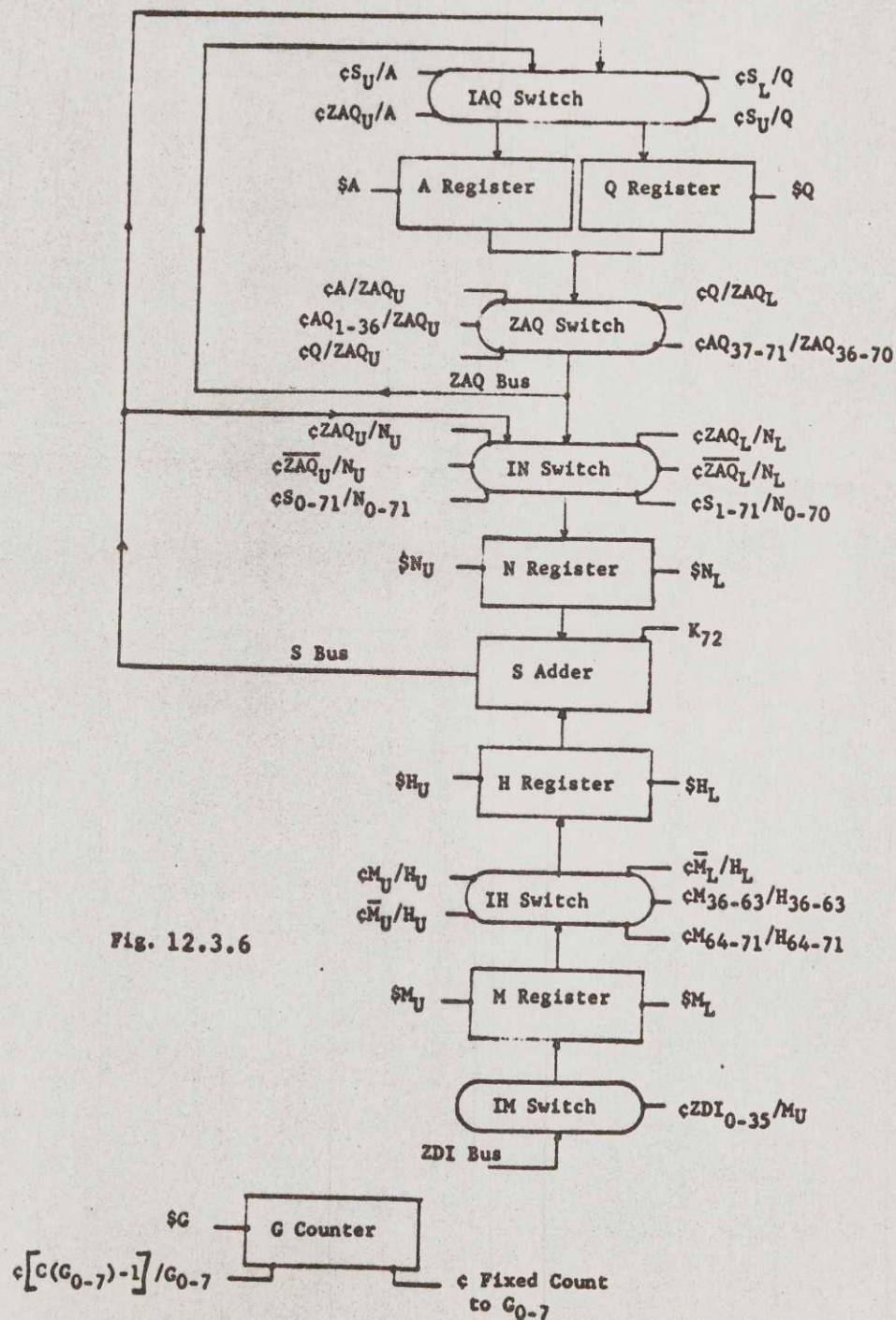
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Spec. No. M50EB00107

Cont. on Sh.12-120 Sh. No.12-119

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

Major Data Paths and Control Points for the Fixed Point Divide
Instructions (OU)



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COMPUTER EQUIPMENT DEPARTMENT
PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh.12-121 Sh. No.12-120

TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR

12.3.6 - contd

0	0 0 → 0 0 35
+1	0 0 → 1 0 35
-1	1 1 → 1 0 35
$[(+2^{35})-1]$	0 1 → 1 0 35
-2^{35}	1 0 → 0 0 35

The divide algorithm used for these instructions makes it necessary that the dividend always be positive and the divisor always be negative before the division is executed. The operands are converted, when necessary, prior to entering the operate (GO) cycles.

To illustrate the control used in the execution of these instructions, one (DIV) will be explained in detail. For the detailed control of both instructions in this group, refer to the OU Specification Chart 43D140232, page 9.

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COMPUTER EQUIPMENT DEPARTMENT
PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh.12-122 Sh. No.12-121

TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR

12.3.6 - contd

In the explanation of the example instruction, the following conditions will be assumed:

- 1) The instruction code has been strobed into the O-register.
- 2) The GS cycle flip-flop has been set.
- 3) The DDF flip-flop has been set indicating the operation decode has settled.

NOTE: Reference to Fig 12.3.6 and the partial timing diagram at the end of the example will aid in understanding of the instruction execution and implementation.

Example 1: Divide Integer (DIV)

During this instruction a 35-bit integer dividend plus sign in the Q-register is divided by a 35-bit integer divisor plus sign from a memory location Y to produce a 35-bit quotient plus sign and a 35-bit remainder plus sign. The contents of the A-register are destroyed by this instruction as a result of the remainder being stored in A at the completion of the instruction.

The load path for the divisor operand into the M-register places ZDI_{0-35} into M_{0-35} . The generation of \$ SET GS and \$ START are as developed in paragraph 12.2.

GS

During GS, the ZAQ and IN switches are enabled to convert $C(Q)$ to a positive dividend. If the sign of the dividend in Q is already positive ($Q_0 = 0$), the control points activated are $\phi AQ_{36-71}/ZAQ_{0-35}$, $\phi ZAQ_{0-35}/N_{0-35}$, and

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GENERAL ELECTRIC COMPANY
COMPUTER EQUIPMENT DEPARTMENT
PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh.12-123 Sh. No.12-122

TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR

12.3.6 - contd

$\phi ZAQ_{36-71}/N_{36-71}$. If the sign of the dividend is negative ($Q_0 = 1$), the control points $\phi AQ_{36-71}/ZAQ_{0-35}$, $\phi ZAQ_{0-35}/N_{0-35}$, $\phi ZAQ_{36-71}/N_{36-71}$, and $\phi SET K_{72}$ are enabled to complement Q and convert the dividend to positive.

When the \$ START pulse propagates the medium delay elements, the first operate strobe \$ occurs. This allows the following events:

- 1) The GS cycle to reset and the GD1 cycle to set.
- 2) The Quotient Sign flip-flop (QSF) and Zero Indicator to reset.
- 3) \$N strobes either ZAQ or $\overline{Z}AQ$ into the N-register.
- 4) \$H is generated, but since no IH switch is enabled, all zeros are loaded into H.
- 5) The K_{72} adder control flip-flop is set if it is necessary to complement Q to produce a positive dividend.
- 6) The Sign Indicator is set if $Q_0 = 1$ or reset if $Q_0 = 0$.
- 7) The \$ strobe re-enters the Timing Pulse Generator delay line network to produce another \$ strobe in about 400 nanoseconds.

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GENERAL ELECTRIC COMPANY
COMPUTER EQUIPMENT DEPARTMENT
PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh.12-124 Sh. No.12-123

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

12.3.6 - contd

GD1

During GD1 the positive dividend will become available at the adder output. Switches are enabled during this time to restore the positive dividend into Q, clear A to zero and set up conditions for a negative divisor to be available during GD2 and the G0 cycles.

The IAQ switch is enabled by $\phi S_{0-35}/AQ_{36-71}$. The IH switch is enabled by $\phi M_{0-35}/H_{0-35}$ if $M_0 = 1$ or by $\phi M_{0-35}/H_{0-35}$ and $\phi M_{36-71}/H_{36-71}$ if $M_0 = 0$. When the ϕ strobe occurs at the end of GD1, the following events take place:

- 1) The GD1 cycle is reset and GD2 cycle is set.
- 2) ϕN is generated, but since no IN switch is enabled, all zeros are loaded into N.
- 3) ϕH is generated transferring the divisor into H.

If the original divisor was positive, the one's complement of M is strobed into H at this time. The negative divisor is obtained by leaving K_{72} set and the one's complement of M in H until $G = 2$ time. For this case, the H-register does not contain the full negative divisor.

- 4) ϕAQ is generated which loads a positive dividend into Q and clears A to all zeros.
- 5) The K_{72} adder control flip-flop is set if it is necessary to complement M to produce a negative divisor. K_{72} will remain set until $G = 2$.
- 6) The Quotient Sign Flip-flop (QSF) is set if the signs of the original dividend and divisor were different.
- 7) The ϕ strobe re-enters the Timing Pulse Generator delay line network to produce another ϕ in about 400 nanoseconds.

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PHOENIX, ARIZONA

Spec. No. M50EB00107
Cont. on Sh.12-125 Sh. No.12-124

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

12.3.6 - contd

GD2

During GD2 the negative divisor will be produced in the adder and become available on the S bus. Switches are enabled during this time to transfer the positive dividend with a left shift of one from AQ to N, set the G-counter to a count of 38, set the Compare Magnitude flip-flop for the compare of the dividend and divisor during GO, and set the Zero Indicator and Divide Check Fault trap if the divisor is zero.

The ZAQ and IN switches are enabled by $\phi AQ_{1-36}/ZAQ_{0-35}$, $\phi AQ_{37-71}/ZAQ_{36-70}$, $\phi ZAQ_{0-35}/N_{0-35}$, and $\phi ZAQ_{36-71}/N_{36-71}$. This left shift of one of the dividend is done so that only one magnitude comparison is done in order to determine whether the quotient will be greater than $(2^{35}-1)$ and therefore not representable with a 35-bit word plus sign.

When the \$ strobe occurs at the end of GD2, the following events take place:

- 1) The GD2 cycle to reset and the GO cycle to set.
- 2) \$N is generated which strobes the divisor left shifted by one into N.
- 3) \$G is generated which strobes the count of 38 into the G-counter.
- 4) The Zero Indicator is set and the Divide Check Fault strobe (\$DVCK) is sent to the CU if the negative divisor is zero. The Abort flip-flop is set in the OU and the OU is reset to an initialized state.
- 5) The Compare Magnitude flip-flop (CMFF) is set.
- 6) If an Abort did not occur because of a zero divisor, the \$ strobe re-enters the Timing Pulse Generator to produce another \$ strobe in about 400 nanoseconds.

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GENERAL ELECTRIC COMPANY
COMPUTER EQUIPMENT DEPARTMENT
PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh. 12-126 Sh. No. 12-125

TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR

12.3.6 - contd

(GO) (CMFF)

During this 400 nanosecond period the first GO cycle is true. The magnitude of the divisor and dividend are compared in the S-adder at this time to determine if a valid quotient will be produced as a result of the DIV execution. If a carry is generated out of bit zero of the adder, then a Divide Check Fault will occur and the divide aborted. Also, during this cycle the control is established to prepare a dividend for the first divide operation which will occur in the second GO cycle if the divide trap does not get set (that is, $SC_0 = 0$). The control points enabled for this are $\phi N_{1-35}/N_{0-34}$, $\phi N_{36}/N_{35}$, and $\phi N_{37-71}/N_{36-71}$. This control will allow a left shift of the dividend by one bit which will produce a dividend to guarantee that the final quotient will not be greater in magnitude than $(2^{35}-1)$.

The fixed count decrement (ϕFCD) lines are enabled at this time to allow the G-counter to be decremented by one on the next strobe.

When the \$ strobe occurs at the end of the first GO cycle, the following events occur:

- 1) The GO cycle is strobed, but since the G count is not zero it is not reset.
- 2) The Compare Magnitude flip-flop is reset.
- 3) The Divide Check Fault strobe ($\phi DVCK$) is sent to the CU if a carry is generated out of bit zero of the adder (that is, $SC_0 = 1$). The Abort flip-flop is set in the OU and the OU is reset to an initialized state.
- 4) ϕN is generated which initiates the left shift of the dividend by one.
- 5) ϕG decrements the G count to 37.
- 6) ϕAQ is generated if there is no carry from bit zero of the adder and clears the AQ-register to zeros.
- 7) If an Abort did not occur, the \$ strobe re-enters the Timing Pulse Generator to produce another \$ in about 320 nanoseconds.

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GENERAL ELECTRIC COMPANY
COMPUTER EQUIPMENT DEPARTMENT
PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh.12-127 Sh. No.12-126

TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR

12.3.6 - contd

(GO)(G > 3)

During the next 34 GO cycles or until the G count equals 3, all but the last of the divide subcycles is performed to produce the quotient. For each of these 34 GO cycles, the contents of the dividend in N and the divisor in H are subtracted in the S-adder. At the end of each cycle a test is made on the carry from bit zero of the adder. If there is a carry (that is, remainder $\geq$ divisor), then the adder result is shifted left one bit and transferred to the N-register to form a new dividend for the next divide.operation. The control points enabled for this are $\phi S_{1-36}/N_{0-35}$ and $\phi S_{37-71}/N_{36-70}$. If there is no carry from bit zero of the adder (that is, remainder $<$ divisor), then the contents of the N-register are shifted left one bit to form a new dividend for the next divide operation. The control points enabled for this are $\phi N_{1-35}/N_{0-34}$, $\phi N_{36}/N_{35}$, and $\phi N_{37-71}/N_{36-70}$.

At the end of each of the 34 GO cycles, the contents of the AQ-register are shifted left one bit and carry from bit zero of the adder is transferred to bit 35 of the A-register. This allows the quotient to be generated on a one bit basis with the most significant bit being produced first. The control points enabled for this are $\phi AQ_{1-36}/ZAQ_{0-35}$, $\phi AQ_{37-71}/ZAQ_{36-70}$, $\phi ZAQ_{0-35}/AQ_{0-35}$, and $\phi SC_0/AQ_{35}$.

When the \$ strobe occurs at the end of each of the 34 GO cycles, the following events occur:

- 1) \$N loads a new dividend into the N-register depending on the state of the carry from the adder bit zero.
- 2) \$A shifts the partial quotient left one bit and loads in a new quotient bit.
- 3) \$G decrements the G-counter by one.
- 4) The \$ strobe re-enters the Timing Pulse Generator to produce a subsequent \$.

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COMPUTER EQUIPMENT DEPARTMENT
PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh.12-128 Sh. No.12-127

TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR

12.3.6 - contd

(GO (G = 3))

The above procedure is repeated until the G-counter equals 3. When $G = 3$, the same events occur as for $G > 3$ except that if the carry from bit zero of the adder is one, the adder result is transferred to N with no left shift, and if the carry was zero, the contents of N are not changed. Also, the H-register is cleared to zero at the end of (GO) ($G = 3$). The control points enabled if the adder carry is one are $\phi S_{0-35}/N_{0-35}$ and $\phi S_{36-71}/N_{36-71}$.

When the \$ strobe occurs at the end of (GO) ($G = 3$), the same events occur as for $G > 3$ except:

- 1) \$N is generated only if the carry from bit zero of the adder was a one.
- 2) \$H clears the H-register.
- 3) The K_{72} adder control flip-flop is unconditionally reset.
- 4) The \$ strobe re-enters the Timing Pulse Generator to produce a subsequent \$.

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GENERAL ELECTRIC COMPANY
COMPUTER EQUIPMENT DEPARTMENT
PHOENIX, ARIZONA

Spec. No. M50EB00107
Cont. on Sh.12-129 Sh. No.12-128

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

12.3.6 - contd

(GO) (G = 2)

During (GO) (G = 2) the quotient and remainder are exchanged between the A-register and the N-register. The quotient is transferred into N in such a manner that the quotient sign may be connected if necessary. The transfer of the remainder in N to A is done via the adder by enabling $\phi S_{0-35}/AQ_{0-35}$. The transfer of the quotient in the A-register to N is done as a function of the Quotient Sign flip-flop (QSF) which may have been set in GD1. If QSF is set, the control is established to transfer the one's complement of AQ to N and set K_{72} . The control points enabled are $\phi AQ_{0-35}/ZAQ_{0-35}$, $\phi AQ_{36-71}/ZAQ_{36-71}$, $\phi \overline{ZAQ}_{0-35}/N_{0-35}$ and $\phi \overline{ZAQ}_{36-71}/N_{36-71}$. If QSF is not set, AQ is transferred straight through into N via $\phi AQ_{0-35}/ZAQ_{0-35}$, $\phi AQ_{36-71}/ZAQ_{36-71}$, $\phi \overline{ZAQ}_{0-35}/N_{0-35}$, and $\phi \overline{ZAQ}_{36-71}/N_{36-71}$.

When the \$ strobe occurs at the end of (GO)(G = 2), the same strobes that were generated for $G > 3$ are produced. The only exception is that K_{72} is set or reset depending on the state of QSF. After this strobe, N will contain the quotient and A the remainder.

(GO) (G = 1)

During (GO) (G = 1), the final sign corrected quotient is produced in the S-adder and will be restored to the Q-register. The control enabled for this is $\phi S_{0-35}/AQ_{36-71}$. Also, during this time the remainder is transferred from the A-register to N as a function of the Sign Indicator which may have been set during GS if the original dividend was negative. If the Sign Indicator is set, the control points $\phi AQ_{0-35}/ZAQ_{0-35}$, $\phi AQ_{36-71}/ZAQ_{36-71}$, $\phi \overline{ZAQ}_{0-35}/N_{0-35}$, and $\phi \overline{ZAQ}_{36-71}/N_{36-71}$ are enabled to transfer the one's complement of the remainder into N; control is established to set K_{72} . If the Sign Indicator is reset, control points $\phi AQ_{0-35}/ZAQ_{0-35}$, $\phi AQ_{36-71}/ZAQ_{36-71}$, $\phi \overline{ZAQ}_{0-35}/N_{0-35}$, and $\phi \overline{ZAQ}_{36-71}/N_{36-71}$ are enabled to transfer AQ straight through to N; K_{72} is reset for this case.

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Spec. No. M50EB00107

Cont. on Sh.12-130 Sh. No.12-129

TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR

12.3.6 - contd

When the \$ strobe occurs at the end of (GO) ($G = 1$), the same strobes that were generated for $G > 3$ are produced except that \$AQ₃₆₋₇₁ is generated instead of \$AQ₀₋₃₅. Other differences are:

- 1) The K₇₂ adder control flip-flop is set if the Sign Indicator is set; otherwise K₇₂ is reset.
- 2) The Sign Indicator is set if bit zero of the adder output is a one; otherwise reset the Sign Indicator.
- 3) The Zero Indicator is set if the adder output is zero; otherwise, reset the Zero Indicator.
- 4) The GO cycle is reset and the GF cycle is set.
- 5) The \$ strobe re-enters the Timing Pulse Generator to produce another \$ in about 400 nanoseconds.

At the end of (GO) ($G = 1$) the quotient with the correct sign is contained in Q₃₆₋₁₇.

GF

During GF the sign correct remainder is produced in the S-adder and the control is established to transfer the remainder into A₀₋₃₅. The control enabled is $\phi S_{0-35}/AQ_{0-35}$. When the \$ strobe occurs at the end of GF, the following events occur:

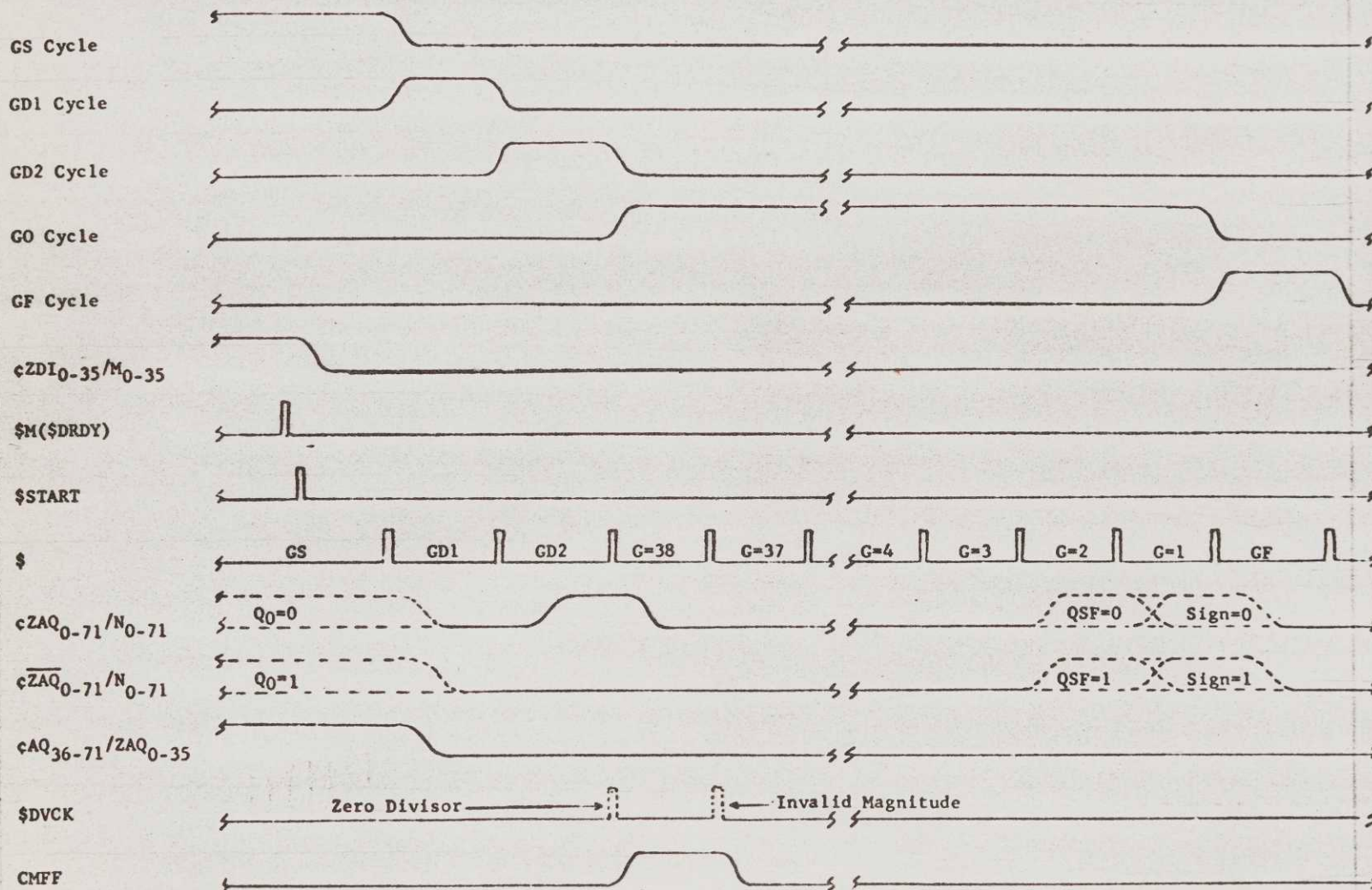
- 1) The GF cycle is reset.
- 2) The \$AQ₀₋₃₅ is generated to load the remainder with its sign equal to that of the dividend into A.
- 3) It generates \$ LAST, which is sent to the CU to signal completion of the DIV instruction.

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Spec. No. M50EB00107

Cont. on Sh.12-131 Sh. No.12-130

TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR



DIV -- Major OU Control Points and Strokes (Part 1)

FIG. 12.3.6a DIV Instruction, Timing Diagram
 (Sheet 1 or 2)

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Spec. No. M50EB00107

Cont. on Sh.12-132 Sh. No.12-131

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ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

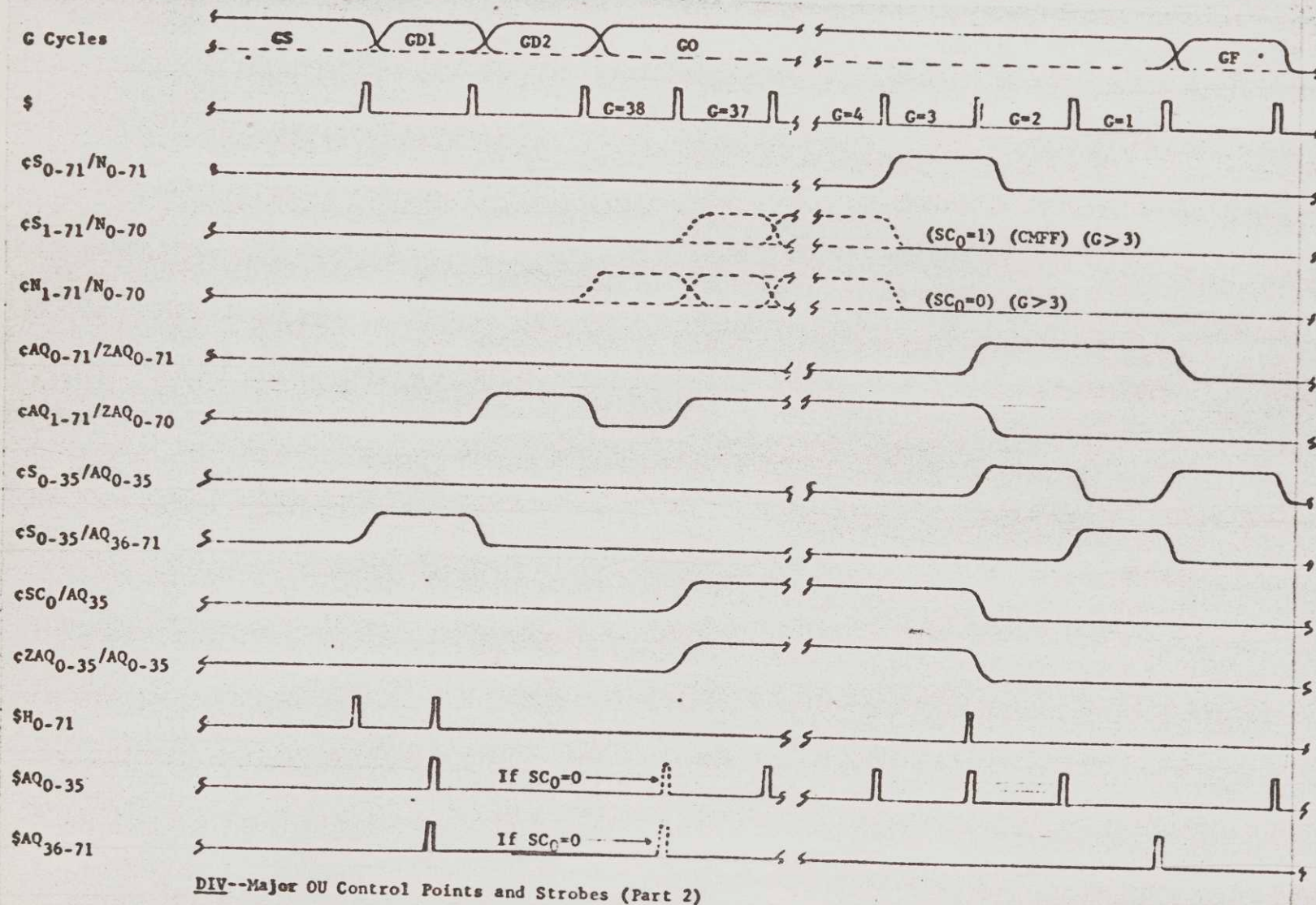


FIG. 12.3.6a DIV Instruction, Timing Diagram
(Sheet 2 of 2)

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Spec. No. M50EB00107

Cont. on Sh.12-1332 Sh. No.12-132

TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR

12.3.7 FIXED POINT SPECIAL INSTRUCTION GROUP

This group of nine instructions complete the fixed point repertoire. They are:

CWL, CMK, RPT, RPD, RPL, BCD, GTB, LREG, and SREG.

All of these instructions except CWL and CMK could be considered a subset of one of the six fixed point groups already discussed. CWL and CMK are unique in that they are the only fixed point instructions that use a GS - GO - GF sequence for their execution. The other seven instructions and the groups they are similar to are:

- a) RPT, RPD, RPL - add group, single precision
- b) BCD - divide group
- c) GTB - shift group
- d) LREG - add group, double precision
- e) SREG - store group, double precision

Each of these instructions will be explained to point out the things that make them special.

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Spec. No. M50EB00107

Cont. on Sh.12-134 Sh. No.12-133

TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR

12.3.7.1 RPT and RPL (Repeat and Repeat Link)

The RPT and RPL instructions are executed with the same sequence as those instructions in the single precision add group. The special feature of these two instructions is that a repeat mode flag is set during their execution which will enable the OU to keep track of the number of times the instruction to be repeated has been processed by the OU. The repeated instruction follows the RPT or RPL instruction. The repeat mode flag being set also allows the OU to detect a condition which will cause termination of the execution of the instruction being repeated. The termination may result from the instruction being repeated a specified number of times; or the state of the zero, sign, overflow, or carry indicator may cause a conditional terminate; or for RPL a Link Address = 0 will cause a terminate.

After the Repeat instruction is executed, the CU will continually send the OU the instruction to be repeated, with the correct operand, until a terminate condition occurs. After a termination condition has been detected, the OU will Abort. Abort is necessary because the instruction being repeated is overlapped and the OU will have started the execution of the repeated instruction one more time before terminate is recognized by the CU. Abort resets the OU to an initialized state to accept the next intended instruction.

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Spec. No. M50EB00107
Cont. on Sh.12-135 Sh. No.12-134

TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR

12.3.7.1 - contd

The execution of the RPT and RPL is accomplished by transferring the operand from the ZDI bus into the M-register on \$DRDY and from M to H on the first \$ at the end of GS. During GF the operand is made available to the inputs of the X₀ index register via the S-adder. On the \$ at the end of GF, and if bit 10 of H is a one, the operand is strobed into X₀. Bits 0-7 are the tally count and 11-17 are the terminate conditions. When \$ LAST occurs for RPT or RPL, the Repeat/Repeat Link mode flip-flop (FTL) and the Sense Terminate flip-flop (STR) are set. These flip-flops set allow the repeated instruction to be processed until a terminate occurs. The tally is decremented by (GS) (GF) (\$) during each repetition of the repeated instruction. When the terminate occurs the terminate flag ϕ TRMF to the CU goes high and this flag allows the next \$ LAST to set the TRMF flip-flop in the CU. The \$ that resets GF when ϕ TRFM is high will set Abort in the OU.

When executing RPL, the CU does not permit overlap between an execution of the repeated instruction and the address modification for the next execution of the repeated instruction. Thus, if a Link Address = 0 condition occurs in the YS adder (bits 0-17) while the present repeated instruction is being processed, a terminate will be generated prior to executing the repeated instruction again using address zero for an operand fetch.

For the detailed control of these two instructions refer to the OU Specification Chart 43D140232, page 11. A partial timing diagram for the RPT/RPL mode is shown on the following page.

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Spec. No. M50EB00107

Cont. on Sh.12-136 Sh. No.12-135

TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR

RPT/RPL - Major OU Control and Strobes for Repeat Mode

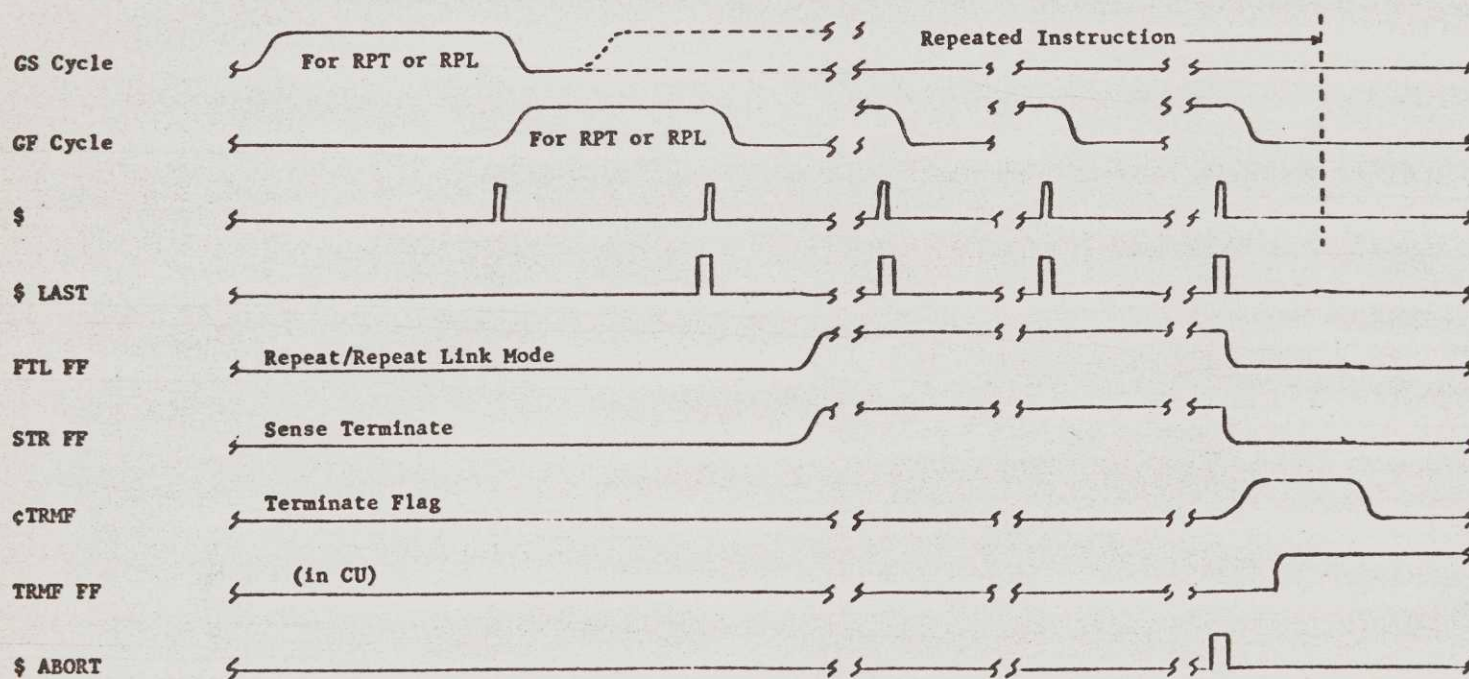


Fig 12.3.7.1

FIG. 12.3.7.1 RPT/RPL Instructions, Timing Diagram

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Spec. No. M50EB00107

Cont. on Sh.12-137 Sh. No.12-136

TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR

12.3.7.2 RPD (Repeat Double)

When in the Repeat Double mode the repeated pair of instructions is always an even/odd pair and each instruction of the pair is executed the same number of times. The tally count is only decremented at the end of the GS cycle of the odd instruction, and a terminate condition is recognized only after completion of the odd instruction. As with RPT and RPL, the RPD is executed by transferring the operand from the ZDI bus into the M-register on \$DRDY and from M to H on the first \$ at the end of GS. During GF the operand is made available to the inputs of the X_0 index register via the S-adder. On the \$ at the end of GF, and if bit 10 of H is a one, the operand is strobed into X_0 . Bits 0-7 are the tally count and 11-17 are the terminate conditions. On \$ LAST of the RPD, the Repeat Double mode flip-flop (FRD) is set and remains set until a terminate occurs. The Sense Terminate flip-flop (STR) will set on \$ LAST of each even repeated instruction and reset on \$ LAST of each odd. This forces the terminate flag cTRMF to the CU to come high only if a terminate condition exists during the odd repeated instruction. \$ABORT is generated the same as for RPT and RPL.

For the detailed control of RPD, refer to the OU Specification Chart 43D140232, page 11. A partial timing diagram for RPD is shown on the following page.

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PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh.12-138 Sh. No.12-137

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

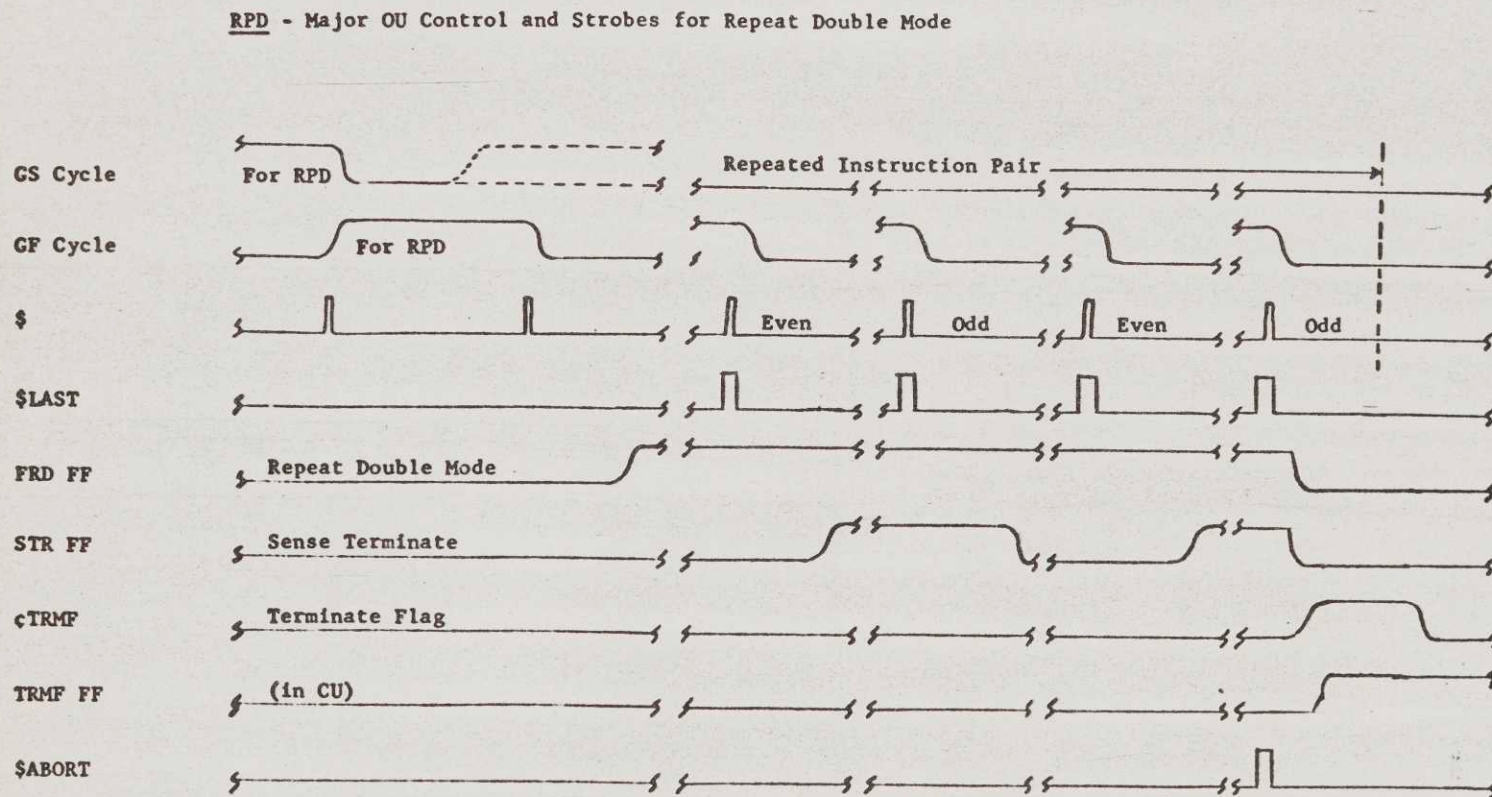


FIG. 12.3.7.2 RPD Instruction, Timing Diagram

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Spec. No. M50EB00107

Cont. on Sh. 12-139 Sh. No. 12-138

TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR

12.3.7.3 BCD (Binary to Binary-Coded-Decimal)

The BCD algorithm used in this machine makes it possible to make the BCD execution a subset of the fixed point divide group. Each time the BCD instruction is executed, a 6-bit binary-coded-decimal digit is generated. The BCD number generated is in an (8, 4, 2, 1) code and the first two bits of the 6-bit number are always zero. Only valid BCD numbers $(000000)_2 = (0)_{10}$ through $(001001)_2 = (9)_{10}$ are generated.

The magnitude of the binary contents of the A-register are converted to a BCD digit by the use of a conversion constant from memory. Because of the BCD algorithm, if the binary number in A is a negative quantity, it is two's complemented and converted to the same positive number before the BCD conversion and the sign is retained in the sign indicator. After the BCD conversion the Q-register will hold the magnitude of the BCD sign. At the end of the execution of the BCD instruction, the A-register will contain the remainder of the original binary number with the original sign restored. If the BCD instruction is issued again, the remainder will now be the binary number used in the generation of the next BCD digit. Each time the BCD instruction is issued in the conversion of a binary number to a BCD digit, a new conversion constant is required from memory.

Because of the conversion constants necessary for the BCD conversion, the largest binary number that can be converted to BCD is $\pm (9,999,999,999)_{10}$. Although a binary number of -2^{35} or $-(34,359,738,368)_{10}$ can be contained in a 36-bit register, a conversion constant of 8×10^{10} which would be necessary to convert this number can not be represented with 36 bits. This implies that the 2^{34} bit should never be a one in the binary number that is to be converted.

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Spec. No. M50EB00107

Cont. on Sh.12-140 Sh. No.12-139

TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR

12.3.7.3 - contd

Although the BCD conversion uses the divide hardware, the divide check fault will not set during BCD; that is, a divisor of zero (the conversion constant) or a magnitude check on the number to be converted is not performed.

GS

Execution of the BCD instruction is initiated by transferring the conversion constant on the ZDI bus into the M-register during GS when \$DRDY is received from the CU. Also during GS the control is established to load the N-register with the contents of A (the number to be converted) in such a manner that a positive dividend will be guaranteed. The control enabled is $\phi AQ_0-35/ZAQ_0-35$ and $\phi ZAQ_0-71/N_0-71$ if the binary number is already positive, or $\phi AQ_0-35/ZAQ_0-35$, $\phi ZAQ_0-71/N_0-71$, ϕ Set K72, and ϕ Set Sign Indicator if the number is negative and needs to be two's complemented. On the ϕ strobe at the end of GS the N-register is loaded with A or $\bar{A}$, the H-register is cleared, K72 and the Sign Indicator will set if $A_0 = 1$, the QSF flip-flop and Zero Indicator will reset, and the GD1 cycle will be entered.

GD1

During GD1 control is established to load the S-adder output (positive dividend) into N, load a negative divisor (conversion constant) into H, and shift the AQ-register left one bit to form the first zero bit of the BCD digit. The controls enabled for these operations are $\phi S_0-71/N_0-71$, $\phi AQ_1-71/ZAQ_0-70$, $\phi ZAQ_0-71/AQ_0-71$, $\phi ZAQ_0-71/AQ_0-71$, $\phi M_0-35/H_0-35$ if $M_0 = 1$, ϕM_0-71 if $M_0 = 0$, and ϕ Set K72 if $M_0 = 0$ or reset if $M_0 = 1$. On the ϕ strobe at the end of GD1 the N-register is loaded

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Spec. No. M50EB00107

Cont. on Sh.12-141 Sh. No.12-140

TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR

12.3.7.3 - contd

with the positive dividend, the H-register and K72 are strobed to make up the negative divisor, and the AQ-register is strobed for a left shift of one to force Q35 to zero. GD2 is set at this time.

GD2

During GD2 control is established to do another left shift of the AQ by one and load the G-counter with a count of 6. The control for the AQ left shift is the same as that used in GD1. When the strobe occurs at the end of GD2 and AQ is shifted to make Q34 and Q35 zero. The \$G strobe is produced to load a fixed count of 6 into the G-counter and the GO cycle is set.

(GO) (G > 3)

For the first three GO cycles or while $G = 6, 5,$ and 4 , three bits of the BCD digit are formed using the S-adder. Each carry out of bit zero of the adder becomes a bit of the BCD digit at the end of each GO cycle in the same manner that a quotient is generated for divide. At the end of each GO for $G = 6, 5,$ and 4 and if $C_0 = 1$, the adder sum is shifted left one bit and loaded into N to form a new remainder by $\phi S_{1-71}/N_{0-70}$; or if $C_0 = 0$ the N-register itself is shifted left one bit to form a new remainder by $\phi N_{1-34}/N_{0-34}$, $\phi N_{36}/N_{35}$, and $\phi N_{37-71}/N_{36-70}$. For each GO the AQ is shifted left one bit the same as above and the new C_0 is inserted into Q35 by $\phi C_0/AQ_{71}$ to form a new bit of the BCD inserted into Q35 by $\phi C_0/AQ_{71}$ to form a new bit of the BCD inserted digit. The G count is decremented at the end of each GO cycle.

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Spec. No. M50EB00107

Cont. on Sh.12-142 Sh. No.12-141

TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR

12.3.7.3 - contd

(GO) (G = 3)

During (GO) (G = 2), the last or fourth BCD digit is generated in the adder. This cycle is also similar to divide in that if $C_0 = 1$ the adder output is transferred into N with no shift by $\phi S_{0-71}/N_{0-71}$; or if $C_0 = 0$ the contents of N are unaltered. Again on the \$ at the end of GO, the AQ is shifted left one bit as above and the new C_0 is inserted into Q_{35} . The H-register is cleared to zero and the G count decremented to 2. At this time the 6-bit decimal digit is contained in Q_{30-35} and a positive remainder is in N.

(GO) (G > 2)

During (GO) (G = 2), a set of redundant transfers take place to make the BCD instruction compatible with divide. The BCD digit in Q is transferred into the upper end of N, and the binary positive remainder in N is transferred into A via the adder. These transfers take place on \$ at the end of GO and the G count is decremented to one.

(GO) (G = 1)

During (GO) (G = 1), the BCD character in N is returned to Q via the adder. The remainder in A is placed back in N in such a fashion to allow the remainder to be corrected in sign if necessary during GF. If the original binary number in A was positive, no sign correction is necessary so $\phi AQ_{0-35}/ZAQ_{0-35}$ and $\phi ZAQ_{0-71}/N_{0-71}$ are enabled to place the remainder as is into N. If the original number was negative, $\phi AQ_{0-35}/ZAQ_{0-35}$,

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Spec. No. M50EB00107

Cont. on Sh.12-143 Sh. No.12-142

TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR

12.3.7.3 - contd

$\phi ZAQ_{0-71}/N_{0-71}$, and ϕ Set K_{72} are enabled. The complete BCD character in N is restored to Q via $\phi S_{0-35}/AQ_{36-71}$. On the \$ strobe at the end of (GO) ($G = 1$), the G-counter is decremented to zero, the BCD character is loaded in Q, the remainder is loaded in N, K_{72} is set if required, and the GF cycle is set.

GF

During GF the remainder with correct sign is produced in the adder and $\phi S_{0-35}/AQ_{0-35}$ is enabled to restore the remainder to A. On the \$ strobe at the end of GF the remainder is restored to A and K_{72} is unconditionally reset. The Zero Indicator is set if the adder output is zero which means that there is no remainder and the total binary to BCD conversion is complete.

For the detailed control of BCD, refer to the OU Specification Chart 43D140232, page 9.

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Spec. No. M50EB00107

Cont. on Sh.12-144 Sh. No.12-143

TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR

12.3.7.4 GTB (Gray Code to Binary)

The GTB algorithm used in this machine made it possible to make the GTB instruction a subset of the Shifted Group. The major differences between the shifts and GTB are that the GTB always has 36 shifts, there can be no overshift and therefore no GN cycle. GTB is comparable to the Rotate A instruction with special bit control on bit 35. Also, during GTB the G-counter is used as a full 8-bit decrement counter. The GTB conversion is defined by the following algorithm, where R_i and S_i denote the contents of the i^{th} bit of the number before and after conversion:

$$S_0 = R_0$$

$$S_i = (R_i \cdot \overline{S_{i-1}}) \oplus (\overline{R_i} \cdot S_{i-1})$$

where $\oplus$ = exclusive "OR"

This GTB instruction will give meaningful results only if the gray coded number to be converted is of the cyclic (gray or reflected) code where only one bit of the coded number changes for adjacent numbers. Specifically, the numbers are:

<u>Gray Code</u>	<u>Binary</u>	<u>Decimal</u>
0000	0000	0
0001	0001	1
0011	0010	2
0010	0011	3
0110	0100	4
0111	0101	5
0101	0110	6
0100	0111	7
1100	1000	8
1101	1001	9
1111	1010	10
etc.	etc.	etc.

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Spec. No. M50EB00107

Cont. on Sh.12-145 Sh. No.12-144

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

12.3.7.4 - contd

The GTB conversion is accomplished with an exclusive OR, and the shift capabilities of the N-register. The gray coded number originally in the A-register is transferred into N for the conversion. The first shift is a simple rotation to preserve the sign bit. The next 35 left shifts are used to accumulate the correct binary bits which are inserted into N_{35} at the end of each GO cycle. Each bit generated is determined by the exclusive OR of bits N_0 and N_{35} that exist after the previous shift.

GS

This instruction is executed by transferring the gray coded number in the A-register into N by enabling $\phi A_{Q0-35}/Z_{AQ0-35}$ and $\phi Z_{AQ0-35}/N_{0-35}$ during GS. Also, during GS the control is established to load the G-counter with a count of 36. On the $\$$ strobe at the end of GS, the N-register and G-counter are loaded, the H-register is cleared to zero, and the Zero and Sign Indicators are reset. The GS cycle is reset and GO is set.

(GO) (G = 36)

During (GO) (G = 36), control is established to left rotate N one bit and decrement the G-count by one. The control points enabled are $\phi N_{1-35}/N_{0-34}$, $\phi N_0/N_{35}$, and ϕFCD . On the $\$$ strobe, the sign bit is rotated and the G-count becomes 35.

(GO) (G < 36)

During (GO) (G = 35), control points are enabled to left shift N by one bit and load the first generated binary bit into N_{35} . These controls are $\phi N_{1-35}/N_{0-34}$ and $\phi N_0 \oplus N_{35}/N_{35}$. On the $\$$ strobe at the end of (GO) (G = 35), the binary bit is loaded in N, the G-count is decremented, and a new GO cycle is entered. This process is repeated 34 times until the complete binary word is formed and the GF cycle is set.

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Spec. No. M50EB00107

Cont. on Sh.12-146 Sh. No.12-145

TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR

12.3.7.4 - contd

GF

During GF the binary word in N is restored to A via the S-adder. The control point enabled is $\phi S_0-35/AQ_0-35$. On the ϕ strobe at the end of GF the Sign Indicator will set if bit one of the adder is a one, and the Zero Indicator will set if the adder output is zero.

For the detailed control of GTB, refer to the OU Specification Chart, 43D140232, page 7. An example of GTB is shown on the following page.

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Spec. No. M50EB00107

Cont. on Sh.12-147 Sh. No.12-146

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

EXAMPLE: Assume a 6-bit register holding a $(+10)_{10}$ gray coded number.

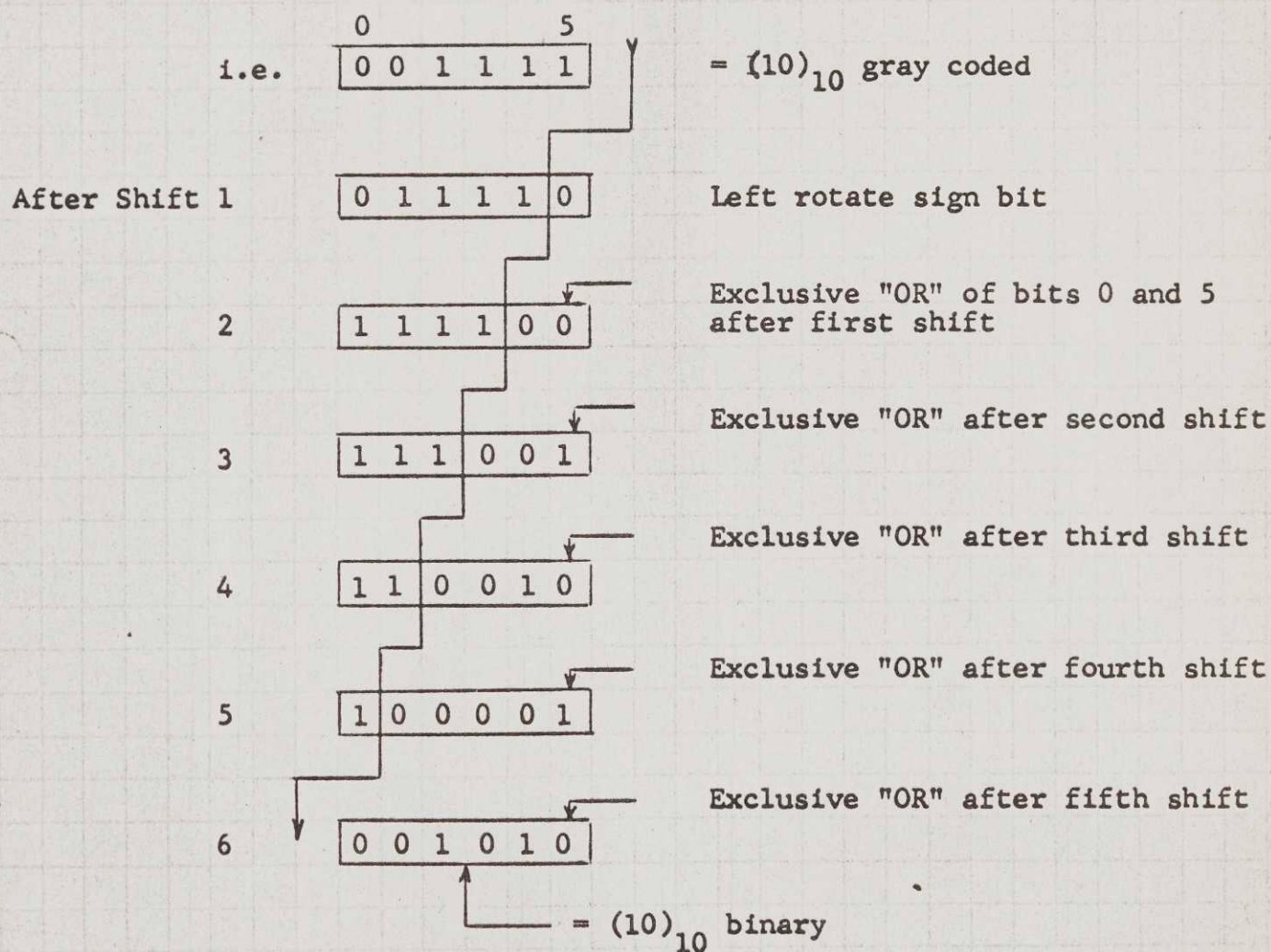


FIG. 12.3.7.4 GTB Instruction Example

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Spec. No. M50EB00107

Cont. on Sh.12-148 Sh. No.12-147

TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR

12.3.7.5 LREG (Load Registers)

This instruction is executed with the same sequence of G cycles as those instructions in the double precision portion of the ADD Group. The special feature of LREG is that four consecutive double precision loads take place with only one operation code. In this respect LREG looks like the instruction referred to by a Repeat Instruction, where the repeat is to be done four times. That is, the CU will send the LREG instruction to the OU four times, followed each time by the appropriate double precision operands. Not until the OU is processing the fourth LREG instruction will the CU send a new instruction to the OU.

The AQ-register, E-register, Timer Register, and Index Registers 0-7 will be loaded with one instruction. The complete operation is done under control of the GRU flip-flops*. The GRU flip-flops are used to determine the order of loading the registers as follows:

GRU 3, 2, 1

000 = Load X₀, X₁, X₂, and X₃ registers

100 = Load X₄, X₅, X₆, and X₇ registers

010 = Load AQ-register

001 = Load E Register

The Index Registers are each 18 bits in length. Therefore, it is possible to load all index registers with two double precision operations. The load AQ portion of this instruction will be done much the same as (LDAQ), and is completely loaded in one double precision operation.

*See paragraph 12.8.12 for a description of the GRU flip-flops.

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Spec. No. M50EB00107

Cont. on Sh.12-149 Sh. No.12-148

TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR

12.3.7.5 contd

The E-register is only 8 bits in length. However, it is loaded as a double precision operation. The E-register data is left justified in the operand word but is loaded into M_{64-71} during the first half of the double precision operation.

When the LREG decode comes true for the first operation, the control points $\phi ZDI_{0-35}/M_{0-35}$ become enabled. On the first \$DRDY strobe for this double precision load, ϕM_{0-71} is generated to load the first half of the memory operand into the M-register. This \$DRDY strobe resets the DPFF, and is turned around as \$YRY and returned to the CU to signal that the next double precision pair may be prepared. This sequence is repeated for the remaining three double precision pairs. Upon entering the GS cycle for each pair the $\phi M_{0-71}/H_{0-71}$ becomes enabled.

GRU = 000

When the \$ START pulse propagates the medium delay elements, the first operate strobe \$ occurs. This allows the following events:

- 1) The GS cycle to reset and the GF cycle to set.
- 2) \$H loads the first double precision operand into H.
- 3) The N-register is cleared to zero by \$N.
- 4) The ORB flip-flop is reset.
- 5) The \$ strobe re-enters the Timing Pulse Generator delay line network to produce another \$ in approximately 400 nanoseconds.

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Spec. No. M50EB00107

Cont. on Sh.12-150 Sh. No.12-149

TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR

12.3.7.5 - contd

During this first GF cycle, the memory operand is made available on the S bus at the adder output. The GRU flip-flops being reset enable control lines for loading $X_0 - X_3$. These lines are:

a - For X_0 , $\phi S_0-17/ZRX_0-17$

b - For X_1-3 , $\phi S_0-71/IBN$

During GF, the GS cycle for the second DP pair will set allowing maximum overlap of the processing of the LREG instruction. When the \$ strobe occurs at the end of GF, the following events take place:

- 1) The GF cycle is reset.
- 2) GRU_3 is set.
- 3) $\$X_0 - \X_3 are generated to load the four upper index registers.

GRU = 100

During (LREG) ($GRU's = 100$), the same process as above is repeated except that during GF control is enabled to load $X_4 - X_7$. This control is $\phi S_0-71/IBN$. On the \$ strobe at the end of the second GF, GF is reset, GRU_3 is reset and GRU_2 set, and $\$X_4 - \X_7 are generated to load the four lower index registers.

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GENERAL ELECTRIC COMPANY
COMPUTER EQUIPMENT DEPARTMENT
PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh.12-151 Sh. No.12-150

TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR

12.3.7.5 - contd

GRU = 010

During (LREG) (GRU's = 010), the same process is again repeated except that during GF control points $\phi S_{0-71}/AQ_{0-71}$ are enabled to load the full AQ-register. On the \$ strobe at the end of GF, GF is reset, GRU_2 is reset and GRU_1 set, and ϕAQ_{0-71} is generated to load the AQ-register.

GRU = 001

During (GS) (LREG) (GRU's = 001), the same process of accumulating the double precision word in the M-register is again repeated. The first half of the double precision load is done by enabling $\phi ZDI_{0-7}/M_{64-71}$ for what will be the E-register contents. For the second half of the double precision load, the control $\phi ZDI_{0-35}/M_{0-35}$ is enabled. After the double precision operand is accumulated during (GRU's = 001), the CF may then send a new operation code to the OU to allow the normal overlap of instruction execution.

At the same time that the M-register is being loaded, control is enabled to transfer the E-register operand from M to D. This control point is $\phi M_{64-71}/D_{0-7}$.

When the \$ strobe occurs at the end of GS, the following events take place:

- 1) GS is reset and GF set.
- 2) \$D is generated to load D.

During the final GF of LREG, $\phi D_{0-7}/E_{0-7}$ are enabled to load the last operand. The \$ strobe at the end of GF will load the E-register and GF and GRU_1 will reset. The \$ will become \$ LAST to complete the LREG instruction.

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PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh.12-152 Sh. No.12-151

TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR

12.3.7.6 SREG (Store Registers)

This instruction is executed with the same sequence of G cycles as those instructions in the double precision portion of the Store Group. The special feature of SREG is that four consecutive double precision stores take place with only one operation code. In this respect, SREG looks like the instruction referred to by a Repeat Instruction, where the repeat is to be done four times. That is, the CU will send the SREG instruction to the OU four times, followed each time by the appropriate transfer from the OU of the double precision store data. Not until the OU is processing the fourth SREG instruction will the CU be able to send a new instruction to the OU.

The AQ-register, E-register, Timer Register, and Index Registers 0-7 will be stored with one instruction. The complete operation is done under control of the GRU flip-flops*. The GRU flip-flops are used to determine the order of storing the registers as follows:

GRU 3, 2, 1

000 = store X_0 , X_1 , X_2 and X_3 registers

100 = store X_4 , X_5 , X_6 and X_7 registers

010 = store AQ-register

001 = store E and Timer Registers

*See paragraph 12.8.12 for a description of the GRU flip-flops.

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GENERAL ELECTRIC COMPANY
COMPUTER EQUIPMENT DEPARTMENT
PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh.12-153 Sh. No.12-152

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

12.3.7.6 - contd

The index registers are each 18 bits in length. Therefore, it is possible to store all index registers with two double precision operations. The store AQ Portion of this instruction will be done much the same as (STAQ), and is accomplished in one double precision operation. The E-register and the Timer are stored during the last double precision operation. The exponent register is left justified in the first word and the Timer is left justified in the second word of the last double precision operation.

When the SREG decode has settled for the first time and the GS cycle is set, the GC cycle flip-flop sets. This allows the ZAQ and ZDO switches to be enabled by $\phi X_0/ZAQ_{0-17}$, $\phi Z_1/ZAQ_{18-35}$ and $\phi ZAQ_{0-35}/DO_{0-35}$. These switches enable The X_0 and X_1 Index Registers to be present at the DO bus.

When the \$ set GS pulse was generated for this instruction, it was delayed by about 40 nanoseconds to become \$YRY and it becomes \$SDY.

\$SDY is sent to the CU to initiate the memory store cycle prior to the occurrence of the first \$ strobe in the OU.

GRU = 000

When the \$ START pulse propagates the medium delay elements, the operate strobe \$ occurs. This allows the following events:

- 1) The GS cycle is reset and the GT cycle is set.
- 2) The O-register busy flip-flop ORB is reset.
- 3) A level consisting of DP Stores and GT goes high.
- 4) The \$ strobe re-enters the Timing Pulse Generator, but because a store is being executed, this will not produce a subsequent \$ strobe.

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COMPUTER EQUIPMENT DEPARTMENT
PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh.12-154 Sh. No.12-153

TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR

12.3.7.6 - contd

Within a minimum time of 300 nanoseconds after \$DSY, the first half of the store operation will be complete and the first \$DS will be received from the Interface Frame to signal this fact. \$DS will produce a \$ t strobe which will:

- 1) Reset the GC and GT cycle flip-flops.
- 2) Set the GF and GFT cycle flip-flops.
- 3) \$ will be "ANDed" with the DP Stores and GT level to produce \$DP which is delayed by approximately 270 nanoseconds before being sent to the Interface Frame to signify that the second data word is ready to be stored.

When the GF cycle was set, the ZAQ and ZDO switches are enabled by control points cX_2/ZAQ_{0-17} , cX_3/ZAQ_{18-35} and $cZAQ_{0-35}/DO_{0-35}$. This allows the X_2 and X_3 Registers to be present at the DO bus before the OU_3 sends the \$DP pulse to the Interface Frame for the second half store.

The \$DP strobes the data into the Data Out Buffer bits 36-71 and is returned as the second \$DS indicating that the second half data has been received. This \$DS will generate a \$ pulse which will:

- 1) Reset the GF and GFT cycles.
- 2) GRU_3 is set in preparation for the next double word transfer.

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PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh.12-155 Sh. No.12-154

TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR

12.3.7.6 - contd

GRU = 100

The CF will have sent the SREG instruction to the OU again by the end of the first GS cycle, so the OU is ready to go through another double word transfer. This will allow the SREG to overlap itself in the OU. The same execution procedure as above is again repeated except that for (SREG) (GRU's = 100), index registers X4 - X7 are stored into memory. At the end of the second GF cycle GRU₃ is reset and GRU₂ is set.

GRU = 010

During (SREG) (GRU's = 010), the same double precision store sequence as above is executed. This time control points are enabled to store the A- and the Q-registers via the ZAQ and ZDO switches during the first and second half of the instruction. At the end of the third GF, GRU₂ is reset and GRU₁ is set. The CF cannot send the next sequential instruction to the OU until the GRU count is 001.

GRU = 001

During the final store operations which take place for (SREG) (GRU's = 001), the E-register and Timer are stored. The E-register is stored first via $\phi E/DO_{0-7}$. The Timer is stored via $\phi TR/ZAQ_{0-23}$ and $\phi ZAQ_{0-35}/DO_{0-35}$. When the \$ strobe occurs at the end of the fourth GF cycle, GRU₁ and GF are reset. This \$ strobe becomes \$ LAST which is sent to the CF to signal completion of the SREG instruction.

For detailed control of SREG, refer to the OU Specification Chart 43D140232, page .

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PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh.12-156 Sh. No.12-155

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

12.3.7.7 CWL (Compare with Limits)

The CWL instruction is a special compare to determine the algebraic magnitude of a memory word relative to the contents of the A- and the Q-registers. The comparison will determine whether an algebraic number from memory is contained within a closed interval bounded by the algebraic contents of A on one end and the algebraic contents of Q on the other. It makes no difference if the algebraic magnitude of A is less than, equal to, or greater than Q.

that is, $C(A) \leq c(Y) \leq c(Q)$

Example $(-2) \leq (+5) \leq (+7)$ (within limits)

or $c(A) \geq c(Y) \geq c(Q)$

Example $(+7) \geq (+5) \geq (-2)$ (within limits)

If a comparison is made and the number is within the limits of A and Q, the Zero Indicator will be set. If the number is not within the limits of A and Q, the Zero Indicator will not set. The state of the Sign and Carry indicators will reflect the magnitude relationship between the C(Y) and C(Q), and the signs C(Y) and C(Q) will be known. That is,

<u>Sign</u>	<u>Carry</u>	<u>Relation between C(Q) and C(Y)</u>	<u>Signs of C(Q) and C(Y)</u>
0	0	$C(Q) > C(Y)$	$C(Q)_0 = 0,$ $C(Y)_0 = 1$
1	0	$C(Q) \geq C(Y)$	
1	1	$C(Q) < C(Y)$	$C(Q)_0 = C(Y)_0$

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Spec. No. M50EB00107

Cont. on Sh. 12-157 Sh. No. 12-156

TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR

12.3.7.7 - contd

CWL is executed with a GS-GO-GF sequence in the OU. When the CWL decode comes true, the control point $\phi ZDI_{0-35}/M_{0-35}$ on the IM switch are enabled. When the $\$M_{0-71}$ is generated to load the C(Y) into the M-register.

\$ START generation is identical to any other instruction.

GS

During GS, the IH, ZAQ, and IN switches are enabled to load the operand registers H and N for the first comparison. IH is enabled by $\phi M_{0-71}/H_{0-71}$ so that the one's complement of C(Y) will be loaded into H for use in the comparison (subtraction) with C(A) and C(Q). The ZAQ and IN switches are enabled by $\phi AQ_{0-35}/ZAQ_{0-35}$ and $\phi ZAQ_{0-35}/N_{0-35}$ in order to load the C(A) into N.

When the \$ START pulse propagates the medium delay elements, the first operate \$ occurs. This allows the following events:

- 1) The GS cycle is reset and the GO cycle is set.
- 2) $\$N_{0-71}$ and $\$H_{0-71}$ are generated to load H and N.
- 3) The K_{72} adder control flip-flop is set to complete the two's complement of the C(Y).
- 4) The Zero and Sign Indicators are reset.
- 5) The \$ strobe re-enters the Timing Generator to produce another strobe in about 400 nanoseconds.

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Spec. No. M50EB00107

Cont. on Sh.12-158 Sh. No.12-157

TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR

12.3.7.7 - contd

GO

During GO the C(Y) are subtracted from the C(A) in the S-adder. Controls to set the Sign Indicator may come high depending on the subtraction results. Also, during GO, control points $\phi AQ36-71/ZAQ0-35$ and $\phi ZAQ0-35/N0-35$ are established to load the C(Q) into N at the end of GO. When the \$ strobe occurs at the end of GO, the following events take place:

- 1) The GO cycle is reset and the GF cycle is set.
- 2) $\$N0-71$ is generated to load the C(Q) into N.

- 3) The Sign Indicator is set if

$$(\overline{S_0}) [SC_0 \overline{SC_1} + \overline{SC_0} SC_1] + (S_0) [SC_0 SC_1 + \overline{SC_0} \overline{SC_1}].$$

- 4) The \$ re-enters the Timing Generator to produce another strobe in about 400 nanoseconds.

GF

During GF the C(Y) are subtracted from the C(A) in the S-adder. Controls may come high to set the sign, zero, and/or carry indicators depending on the subtraction results. When the \$ strobe occurs at the end of GF, the following events occur:

- 1) The GF cycle is reset.
- 2) The K₇₂ flip-flop is reset.
- 3) The Sign Indicator will set for the same conditions as above.

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Spec. No. M50EB00107

Cont. on Sh.12-159 Sh. No.12-158

TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR

12.3.7.7 - contd

- 4) The Carry Indicator will set if SC_0 (a carry from bit zero of the adder) is a one.
- 5) The Zero Indicator will set if the Sign Indicator was set at the end of GO and it will not be set at the end of GF, OR if the Sign Indicator was not set at the end of GO and it will be set at the end of GF.

That is, $[(\text{Sign Ind}) (\overline{\text{Set Sign Ind}})] +$

$[(\overline{\text{Sign Ind}}) (\text{Set Sign Ind})]$

- 6) This \$ strobe becomes \$ LAST which is sent to the CU to indicate completion of the CWL instruction.

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Spec. No. M50EB00107

Cont. on Sh.12-160 Sh. No.12-159

TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR

12.3.7.7 - contd

Example 1:

Compare C(Y) = (Zero)

with C(A) = (+1) and C(Q) = (-1)

A = 0001

Q = 1111 (2's complement)

Y = (1's complement in H-register)

GO

	1	K ₇₂ set
A	0001	
<u>-Y</u>	<u>1111</u>	
	C 0001	

Sign indicator not set.

GF

	1	
Q	1111	
<u>-Y</u>	<u>1111</u>	
	C 1111	

¢ Set Sign indicator is true
because of (S₀) (SC₀SC₁)

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Spec. No. M50EB00107

Cont. on Sh.12-161 Sh. No.12-160

TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR

12.3.7.7 - contd

The Zero Indicator is set. $[(\overline{\text{SIGN}})(\text{Set Sign}) = 1]$

The Carry Indicator is set. $[\text{SC}_0 = 1]$

The Sign Indicator is set. $[(\text{S}_0)(\text{SC}_0\text{SC}_1) = 1]$

The final indicator conditions say:

- 1) The $C(Y)$ is within the limits of $C(A)$ and $C(Q)$.
- 2) The $C(Q)$ is less than $C(Y)$.
- 3) The sign of Q is negative and the sign of Y is positive.

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Spec. No. M50EB00107

Cont. on Sh.12-162 Sh. No.12-161

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

12.3.7.8 CMK (Compare Masked)

The CMK instruction compares the C(Y) with C(A) on a bit-for-bit basis. However, any number of bits may be ignored in the comparison. The bits to be ignored are denoted by "ones" in the Mask (Q) register. An exclusive "OR" is performed between C(Y) and C(A) to determine if any bits differ. This operation is followed by a logical "AND" of the results of the "EX OR" and the mask word in Q-register. All bits with "ones" in Q will become "Zeros" in the result of the logical "AND" and comparison is made only on the bits which differed and are unmasked. The final results of CMK conditionally set the Zero and Sign indicators. In the general case the zero indicator will set if the exclusive "OR" of C (y) and C(A) "AND" C(Q) equal zero; that is, Set zero if

$$[C(Y) \oplus C(A)] [C(Q)] = 0$$

Two unique cases for which the Zero Indicator will set are:

- 1) Each bit of C(Y) = each bit of C(A).
- 2) C(Q) is all ones.

That is, Set zero if $[C(Y)_{0-35} = C(A)_{0-35}]$
+ $[C(Q)_{0-35} = 1-1]$

The Sign Indicator will be set only if bit zero of Y is not the same as bit zero of A "AND" bit zero of Q is a zero.

That is, Set sign if $(A_0 \neq Y_0) (Q_0 = 0)$

The CMK instruction is executed with a GS - GO--GF sequence as is CWL. The loading of C(Y) into M-register and \$ START generation is per normal procedure.

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Spec. No. M50EB00107

Cont. on Sh.12-163 Sh. No.12-162

TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR

12.3.8 Floating Point Add Group

This group of 17 instructions consists of floating point additions, subtractions, loads, and compares. The major data paths and control points for these instructions are shown in Fig. 12.3.8. In the execution of these instructions, adder registers H and N are loaded from some source, the exponent registers D and E are loaded from some source, the S-adder performs an operation determined by the adder control flip-flops, K₁, K₂, K₃, and K₇₂, the ES-adder performs the required operation, and the results of these operations are strobed into a designated register and/or examined for the purpose of setting Arithmetic Indicators. (For detailed description of the S-adder operation see 12.10.)

To illustrate the control used in the execution of these instructions, several instructions will be explained in detail. For the detailed control of all instructions in this group, refer to the OU Specification Charts 43D140232, page 6.

In the explanation of all the example instructions, the following conditions will be assumed:

- 1) The instruction has been strobed into the 0-register.
- 2) The GS cycle flip-flop has been set.
- 3) The DDF flip-flop has been set indicating the operation decode has settled.

NOTE: Reference to Fig. 12.3.8 and the partial timing diagram at the end of each example will aid in the understanding of the instruction execution and implementation.

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PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh.12-164 Sh. No. 12-163

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

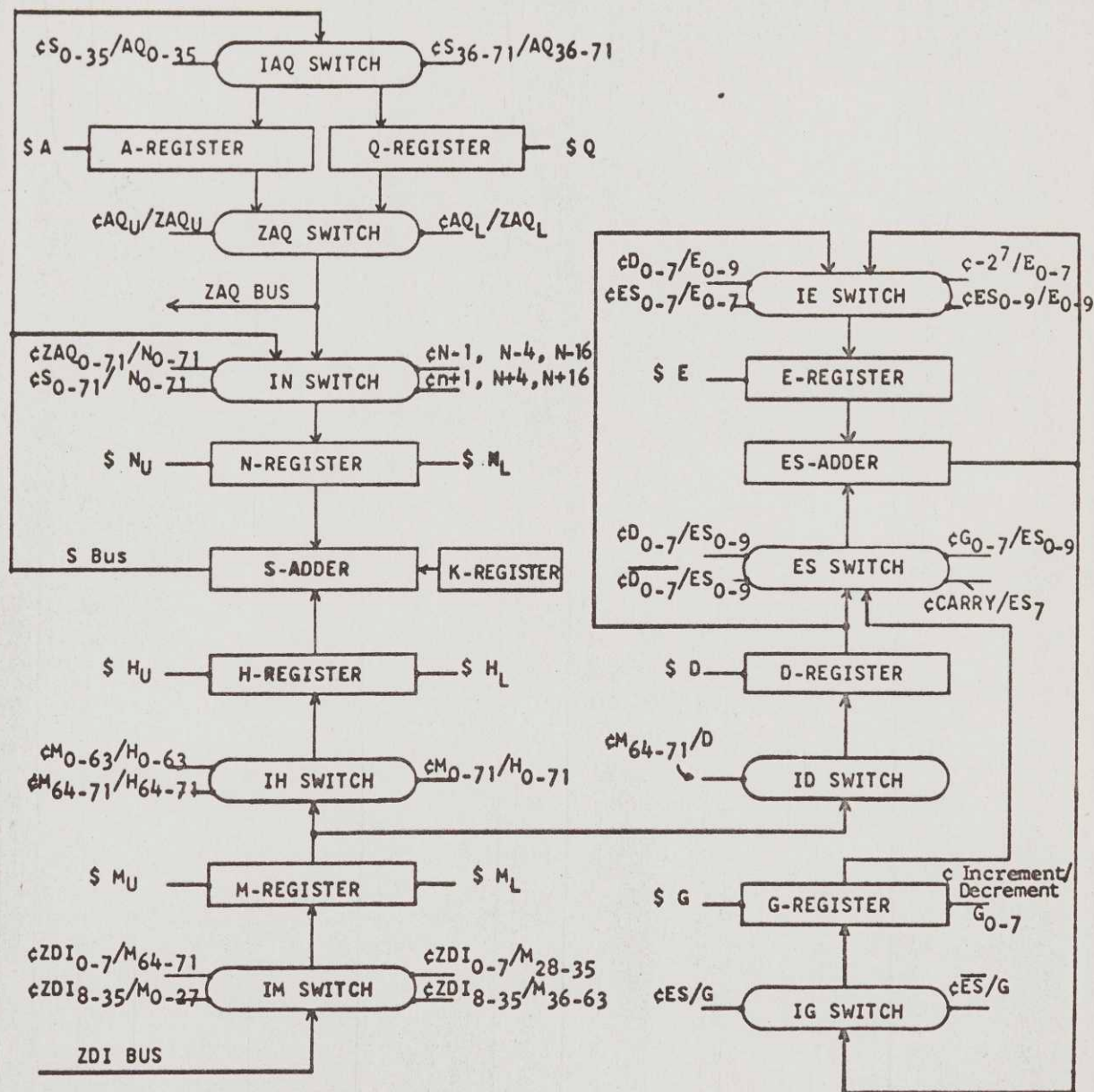


FIG. 12.3.8

- NOTES: (1) c = Control
(2) \$ = Strobe
(3) U = Upper
(4) L = Lower

FIG. 12.3.8 Floating Point Add Group, Major Flowchart

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Spec. No. M50EB00107

Cont. on Sh.12-165 Sh. No.12-164

TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR

12.3.8.1 Single Precision

The instructions comprising the single precision floating point add group can be defined by two classifications:

- 1) Instructions requiring normalization (FAD, FSB).
- 2) Instructions that do not require normalization (ADE, FCMG, FCMP, FLD, FSZN, LDE, UFA, UFS).

Normalized

Under this heading fall the two instructions FAD and FSB.

Example 1: Add (FAD)

During this instruction a floating point number in a memory location Y is added to the contents of the Floating Register (EAQ). This is done by first comparing the exponents, aligning the mantissas, add the mantissas, normalize the result, and store the results in EAQ.

The presence of the FAD instruction code on the ZOR lines together with DPFF reset, BCFF reset, and DIC reset, enable the IM-switch. The control points cZDI0-7/M64-71, and cZDI8-35/M0-27 are enabled presenting the operand lines (ZDI bus) to the proper M-register inputs. When the operand ready strobe (\$ DRDY) is received from the C, the DPFF not being set allows the M-register strobe (\$ M0-71) to be generated and strobe the FAD operand into the M-register. The \$ DRDY pulse is turned around as \$ YRY and returned to the CU to signal that a new instruction may be prepared. \$ YRY sets the operand ready flip-flop (YRY) to allow a \$ START to be generated by a last of three pulse detectors. \$ START sets the OU Busy flip-flop (OUB), resets YRY and DDF, and transfers the operation code from the O-register to the C-register. It also enters the timing pulse generator delay line network.

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Spec. No. M50EB00107

Cont. on Sh.12-166 Sh. No.12-165

TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR

GS

The IH-switch is enabled by $\phi M0-63/H0-63$ and the ID-switch is enabled by $\phi M64-71/D$. These enabled switches allow the mantissa from memory to be present at the inputs to the H-register and the exponent to be present at the inputs to the D-register.

When the \$ START pulse propagates the medium delay elements, the operate strobe (\$) occurs. This pulse causes the following events:

- 1) A \$ H to strobe the mantissa from M into H.
- 2) A \$ N to clear the N-register to zero.
- 3) A \$ D to strobe the exponent from M into D.
- 4) ZERO and SIGN to reset.
- 5) GS to reset and GE to set.
- 6) \$ enters the timing pulse generator delay line network to produce another \$ pulse in approximately 400 nanoseconds.

GE

During the GE cycle the two exponents are compared by subtracting D from E, the difference if any is stored in G, the mantissa with the lesser exponent is stored in N, the other mantissa is stored in H, and the larger exponent is stored in E. The control lines that become enabled to accomplish this are:

- 1) $\phi AQ0-71/ZAQ0-71$ unconditionally
- 2) $\phi ZAQ0-71/H0-71$ unconditionally

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Spec. No. M50EB00107

Cont. on Sh.12-167 Sh. No.12-166

TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR

12.3.8.1 - contd

3) $\phi D/E$	unconditionally
4) $\phi \bar{D}/ES$	unconditionally
5) $\phi CARRY/ES_7$	unconditionally
6) $\phi ZAQ_0-71/N_0-71$	if $ES_9 + (S=0) + (ES=0)$
7) $\phi S_0-71/N_0-71$	if $\overline{ES_9} + (S=0) + (ES=0)$
8) $\phi ES/G$	if $(ES_0) [(ES \neq 0) (/ES/ < 72) (ES_9 + S \neq 0)]$
9) $\phi \overline{ES}/G$	if $(\overline{ES_0}) [(ES \neq 0) (/ES/ < 72) (ES_9 + S \neq 0)]$

At the end of 400 nanoseconds a \$ pulse will cause the following events:

- 1) A \$ H to strobe the mantissa from AQ into H if $(\overline{ES_9} + S = 0 + ES = 0)$.
- 2) A \$ N to strobe a mantissa into N if $(/ES/ < 72) + (ES = 0) + (S=0) (ES_9)$.
- 3) A \$ E to strobe the exponent from D into E if ES_9 .
- 4) A \$ G to strobe the proper count into G_{0-7} unconditionally.
- 5) GE to reset unconditionally.
- 6) GA to set if $(ES \neq 0) (/ES/ < 72) (ES_9 + S = 0)$.

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GENERAL ELECTRIC COMPANY
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PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh.12-168 Sh. No.12-167

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

12.3.8.1 - contd

- 7) GO to set if $(ES = 0) + (/ES/>71) + (\overline{ES_9}) (S = 0)$.
- 8) \$ enters the timing pulse generator delay line network to produce another \$ strobe.

GA

During this cycle the mantissa in N is aligned so that its binary point falls at the same place as that of the mantissa in H. This is accomplished by shifting N right the number of places indicated by the G-counter. The control lines that become enabled to accomplish these events are:

- 1) $\phi N-16$ ($\phi N_0-55/N_{16-71}$, $\phi N_0/N_0-15$) if $G > 14$.
- 2) $\phi N -4$ ($\phi N_0-67/N_4-71$, $\phi N_0/N_0-3$) if $15 > G > 2$.
- 3) $\phi N-1$ ($\phi N_0-70/N_1-71$, $\phi N_0/N_0$) if $3 > G > 0$.
- 4) $\phi N+1$ ($\phi N_1-71/N_0-70$) if REV is set.
- 5) LSA enabled if $(G = 1) + (G = 4) + (G = 16) + (REV)$.

At the end of approximately 230 nanoseconds a \$ strobe will cause the following events.

- 1) A \$ N to strobe the shifted contents of N back into N.
- 2) A \$ G to decrement G by 16 if $\phi N-16$, by 4 if $\phi N-4$, by 1 if $\phi N-1$.
- 3) REV to set if $(G = 15) + (G = 3)$.

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Spec. No. M50EB00107

Cont. on Sh.12-169 Sh. No.12-168

TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR

- 4) GA to reset and GO to set if LSA enabled.
- 5) \$ enters the timing pulse generator delay line network to produce another \$ strobe.

GA will be repeated as many times as required to align the mantissa. The GA sequence will terminate on the first \$ pulse following the enabling of LSA.

GO

During this cycle the contents of N and H are added in the S-adder, the sum is stored in N, and H is cleared to zero. The control line that becomes enabled is:

$\phi S_{0-71}/N_{0-71}$ to transfer the output of the S-adder to N.

At the end of 400 nanoseconds a \$ pulse will cause the following events:

- 1) A \$ H that clears H to zero.
- 2) A \$ N to strobe the output of the S-adder into N.
- 3) REV to set if an overflow occurred.
- 4) SIGN to set if the sum is negative.
- 5) ZERO to set if the sum is zero.
- 6) CARRY to set if there is a carry out of bit position zero.
- 7) CARRY to reset if there is no carry out of bit position zero.

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- 8) K72 to reset.
- 9) G0 to reset.
- 10) GN to set if an overflow occurred or S_0 and S_1 are the same.
- 11) GF to set if no overflow occurred and S_0 and S_1 are different.
- 12) \$ enters the timing pulse generator delay line network to produce another \$ strobe.

GN

During this cycle the mantissa in N is normalized. If an overflow occurred the mantissa is shifted one place right and the G-counter is decremented by 1. In all other cases the mantissa is shifted left until N_0 and N_1 are not alike and the G-counter is incremented by 1 for each place that the mantissa is shifted. The control lines that become enabled to accomplish this are:

- 1) $\phi N_{0-70}/N_{1-71}$, complement N_0) if REV set.
- 2) $\phi N+16$ ($\phi N_{16-71}/N_{0-55}$) if N_0 through N_{15} are all the same.
- 3) $\phi N+4$ ($\phi N_{4-71}/N_{0-67}$) if $\overline{\phi N+16}$ and N_0 through N_3 are all the same.
- 4) $\phi N + 1$ ($\phi N_{1-71}/N_{0-70}$) if $(\overline{\phi N+16})(\overline{\phi N+4})$ and N_0 and N_1 are the same.
- 5) LSN enabled if $(\phi N+16) (N_{15} = N_{16} \neq N_{17})$
+ $(\phi N+4) (N_3 = N_4 \neq N_5)$ + $(\phi N+1) (N_0 = N_1 \neq N_2)$
+ (REV).

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Spec. No. M50EB00107

Cont. on Sh.12-171 Sh. No.12-170

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

At the end of 230 nanoseconds a \$ pulse will cause the following events:

- 1) A \$ N to strobe the shifted contents of N back into N.
- 2) A \$ G to increment the G-counter by 16 if $\phi N+16$, by 4 if $\phi N+4$, by 1 if $\phi N+1$, or decrement G by 1 if REV is set.
- 3) REV to set if $(\phi N+16) (N_{15} \neq N_{16}) + (\phi N+4) (N_3 \neq N_4)$
- 4) REV to reset if REV is set.
- 5) GN to reset and GF to set if LSN enabled.
- 6) \$ enters the timing pulse generator delay line network to produce another \$ strobe.

GN will be repeated as many times as required to normalize the mantissa and will terminate on the first \$ pulse following the enabling of LSN.

GF

During this cycle the mantissa in N is transferred to AQ, the count in G is subtracted from the exponent in E, and EOFL and EUFL are set if required. If the mantissa is zero, the exponent will be forced to -128. The control lines that become enabled to accomplish this are:

- 1) $\phi S_0-71/AQ_0-71$.
- 2) $\phi \bar{G}/ES$ and $\phi CARRY/ES_7$.
- 3) $\phi ES/E$ if mantissa $\neq$ zero.
- 4) $\phi - 2^7/E$ if mantissa = zero.

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Cont. on Sh.12-172 Sh. No.12-171

TITLE: ENGINEERING PRODUCT SPECIFICATION
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At the end of 400 nanoseconds a \$ pulse will cause the following events:

- 1) A \$ AQ to strobe the mantissa into AQ.
- 2) A \$ E to strobe the exponent into E.
- 3) EOFL to set if the subtraction of G from E caused the exponent to exceed +127.
- 4) EUFL to set if the subtraction of G from E caused the exponent to become smaller than -128.
- 5) GF to reset.
- 6) OUBF to reset if no other instruction has been initiated.
- 7) \$ will generate a \$ LAST, which is sent to the CU to indicate completion of the FAD instruction.

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Cont. on Sh. 12-173Sh. No.12-172

TITLE:

ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

FAD - Major OU Control Points and Strokes

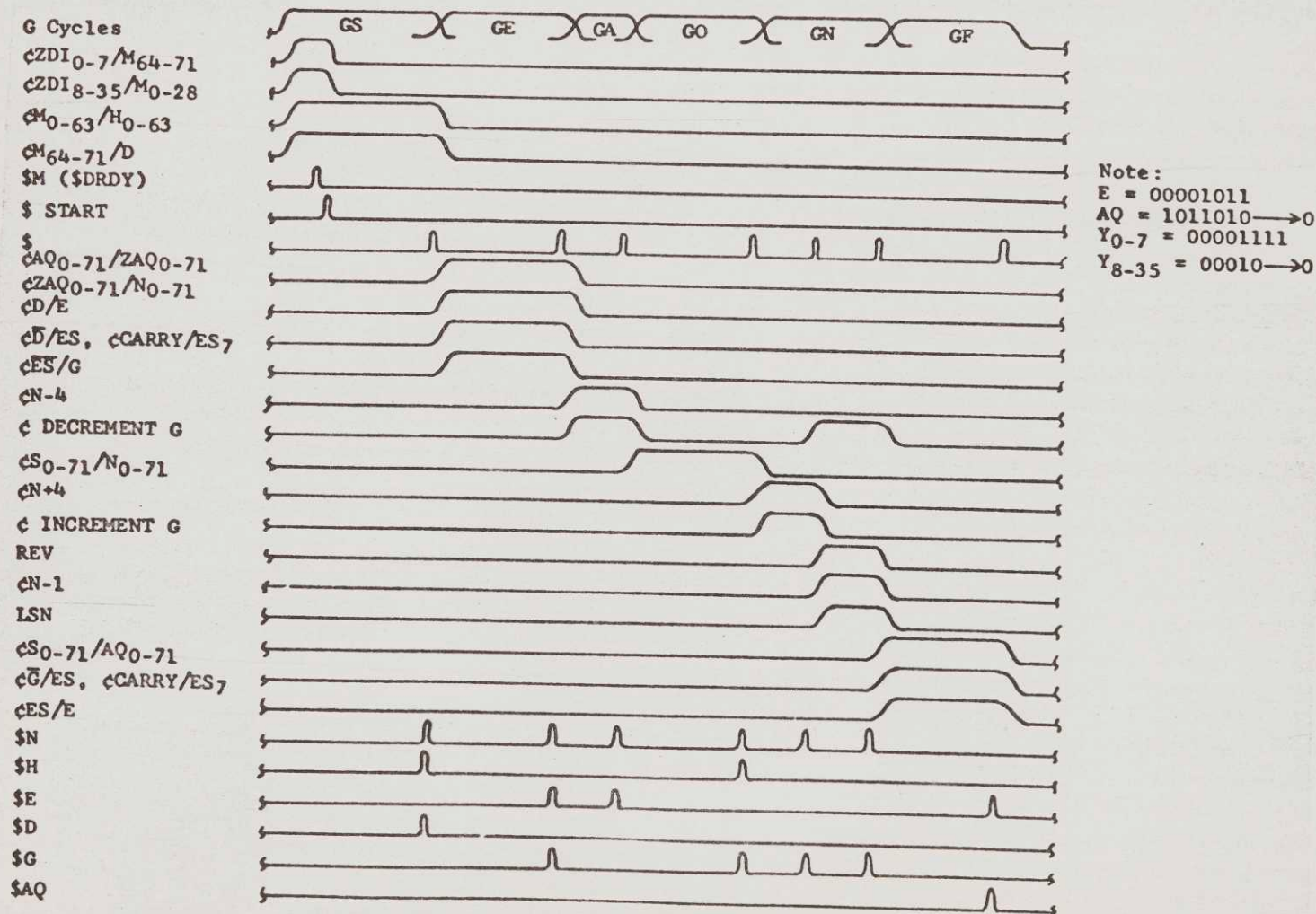


FIG. 12.3.8.1 FAD Instruction, Timing Diagram

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Cont. on Sh. 12-174 Sh. No. 12-173

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

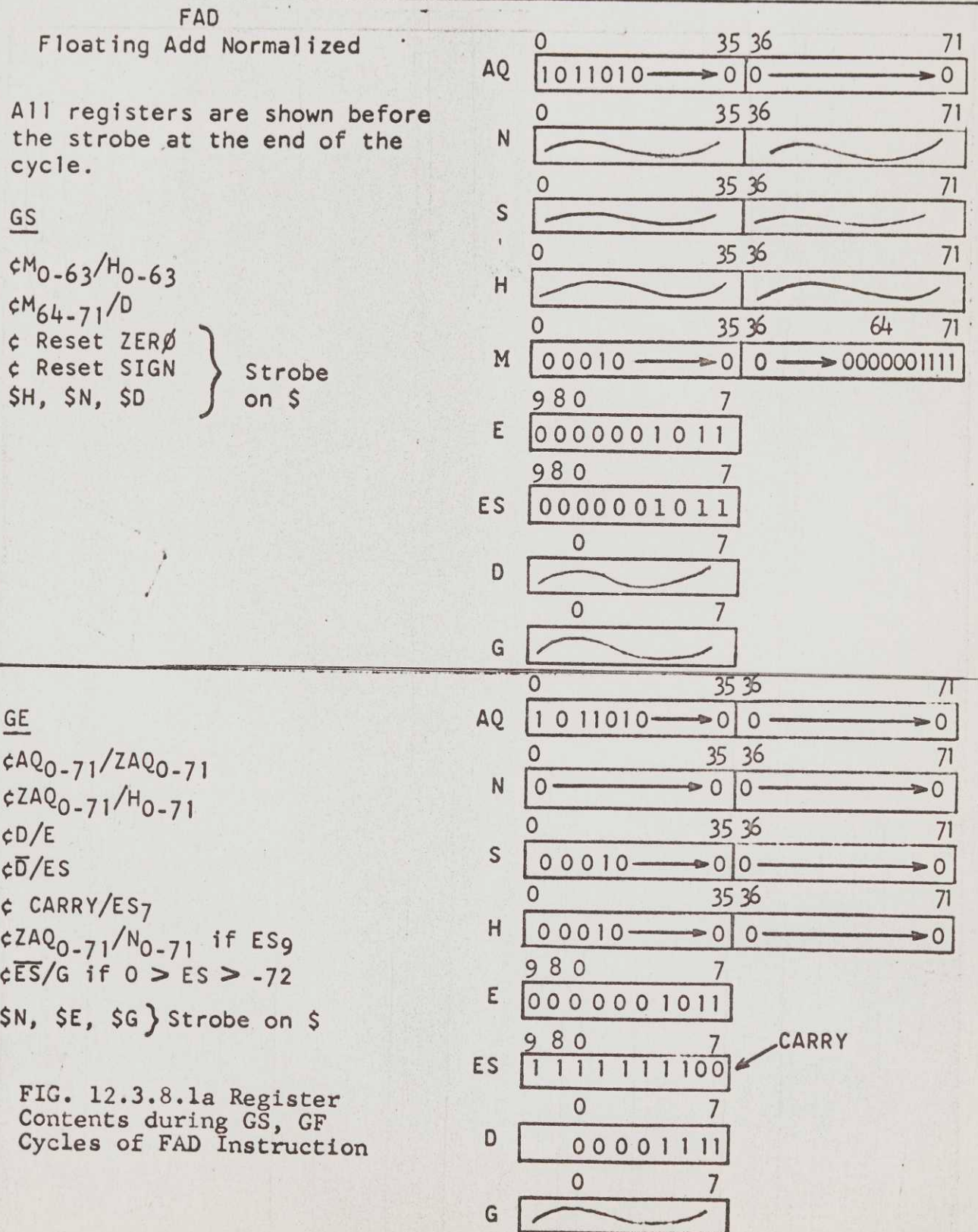


FIG. 12.3.8.1a Register Contents during GS, GF Cycles of FAD Instruction

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Spec. No. M50EB00107

Cont. on Sh.12-175 Sh. No.12-174

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

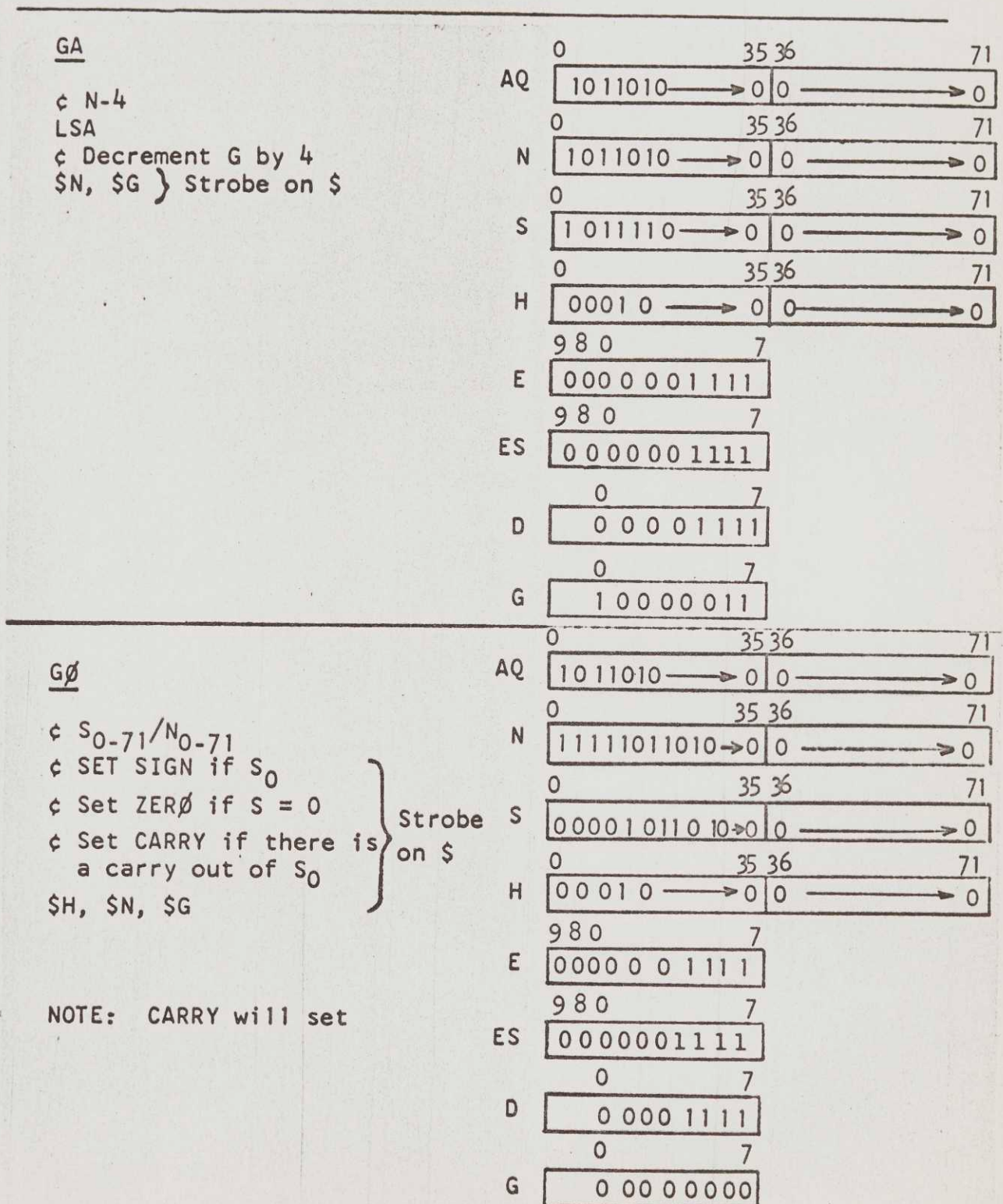


FIG. 12.3.8.1b Register Contents during GA, GØ Cycles of FAD Instruction

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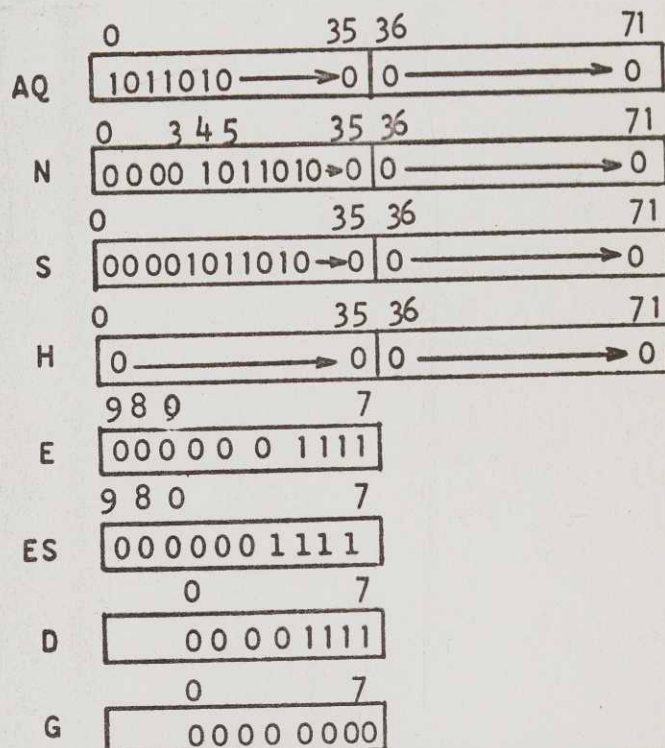
Spec. No. M50EB00107

Cont. on Sh.12-176 Sh. No.12-175

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

GN (first)
¢ N+4
¢ Increment G by 4
¢ Set REV } Strobe on \$
\$N, \$G

NOTE: REV will set



GN (second)
¢ N-1
¢ Decrement G by 1
LSN
¢ Reset REV } Strobe on \$
\$N, \$G

NOTE: Last GN cycle

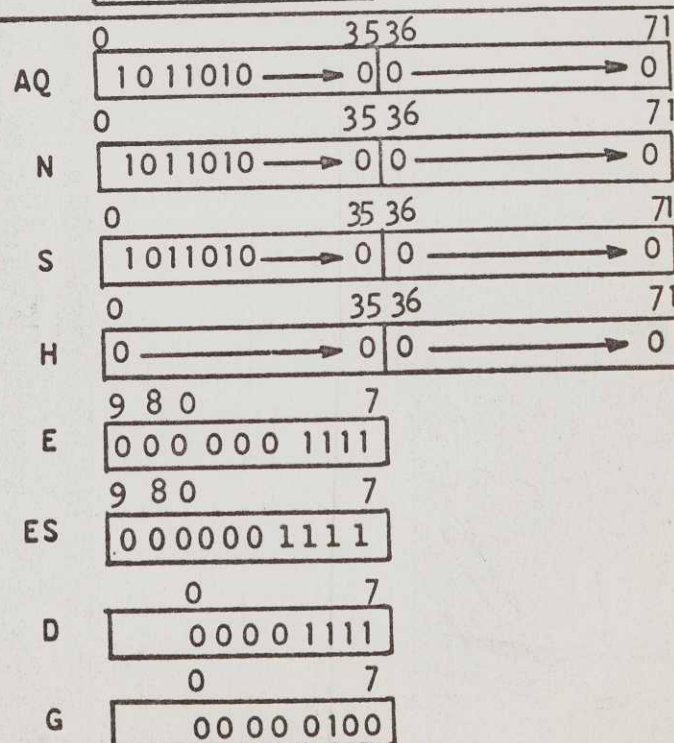


FIG. 12.3.8.1c Register Contents during GN Cycle of FAD Instruction

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Cont. on Sh. 12-177 Sh. No. 12-176

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

GF

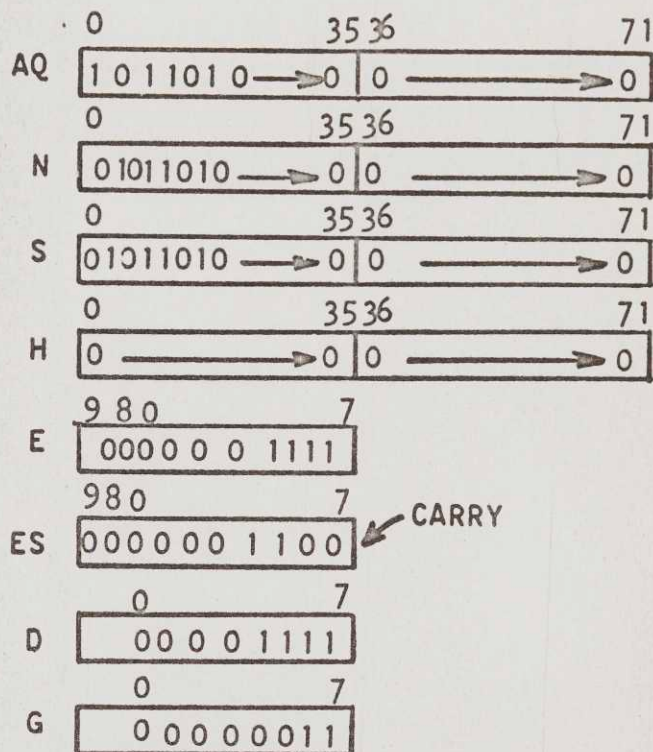
$\phi S_{0-71}/AQ_{0-71}$

$\phi \bar{G}/ES$

ϕ CARRY to ES_7

ϕ ES/E

$\$AQ, \E } Strobe an \$



Contents of the registers
upon completion of the FAD
operation.

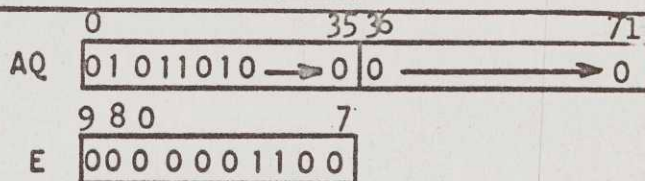


FIG. 12.3.8.1d Register Contents during GF Cycle of FAD Instruction

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TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR

12.3.8.1 - contd

Unnormalized

Within this grouping are the eight instructions ADE, FCMG, FCMP, FLD, FSZN, LDE, UFA, and UFS.

Example 1: Load (FLD)

During this instruction the contents of a memory location Y are loaded into the Floating Register. That is, the exponent (Y0-7) is loaded into the E-register and the mantissa (Y8-35) is loaded into the A-register bits 0-27. The remaining bits of the A-register and all bits of the Q-register are cleared to zero. The presence of the FLD instruction code on the ZOR lines together with the Double Precision flip-flop (DPFF) reset and the Multiply flip-flop (DIC) reset, enables the IM-switch. The control points $\phi ZDI_{0-7}/M_{64-71}$ and $\phi ZDI_{8-35}/M_{0-27}$ are enabled presenting the operand lines (ZDI bus) to the proper M-register inputs. When the operand ready strobe ($\$ DRDY$) is received from the CU, DPFF reset allows the M-register strobe ($\$ M_{0-71}$) to be generated and strobe the FLD operand into the M-register. The $\$ DRDY$ pulse is turned around as $\$ YRY$ and returned to the CU to signal that a new instruction may be prepared. $\$ YRY$ also sets the operand ready flip-flop (YRY) in the OU. When YRY is set, the conditions exist to allow $\$ START$ to be generated by a last of three pulse detectors. $\$ START$ sets the OU Busy flip-flop (OUB), resets YRY and DDF, and transfers the operation code from the O-register to the C-register. It also enters the timing pulse generator delay line network.

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Spec. No. M50EB00107

Cont. on Sh.12-179 Sh. No.12-178

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

GS

When the \$ START pulse propagates the medium delay elements, the operate strobe (\$) occurs. This causes the following events:

- 1) A \$ H which will strobe the FLD mantissa into the H-register bits 0-27 and clear all other bits to zero.
- 2) A \$ D which will strobe the FLD exponent into the D-register.
- 3) A \$ N which will strobe all zeros into the N-register since the IN-switch is not enabled.
- 4) The ZERO and SIGN indicators to reset.
- 5) ORB to reset, indicating that the O-register is free to receive the operation designator for the next instruction.
- 6) GS to reset and GF to set.

GF

The \$ pulse will re-enter the timing pulse generator delay line network. GF being set will delay the pulse 400 nanoseconds before another \$ is generated.

During this 400 nanoseconds the contents of H and N are added together in the S-adder. The add function takes place because none of the K flip-flops are set. The addition of H (mantissa) and N (zeros) produces the mantissa at the S-adder output. The following control points will also be enabled:

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Cont. on Sh.12-180 Sh. No.12-179

TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR

- 1) ¢ S0-35/AQ0-35: Transfer the output of the upper portion of the S-adder to the A-register.
- 2) ¢ S35-71/AQ35-71: Transfer the contents of the lower portion of the S-adder to the Q-register.
- 3) ¢ D/E: Transfer the contents of the D-register to the E-register.

The next \$ strobe will cause the following events:

- 1) \$ AQ which will strobe the mantissa into AQ0-27 and zeros into AQ28-71.
- 2) \$ E which will strobe the exponent into the E-register.
- 3) ZERO to set if the contents of AQ = zero.
- 4) SIGN to set if bit position zero of AQ is a "one".
- 5) GF to reset.
- 6) OUBF to reset if no other instruction has been initiated.

\$ will generate a \$ LAST, which is sent to the CU to indicate completion of the FLD instruction.

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Spec. No. M50EB00107

Cont. on Sh.12-181 Sh. No.12-180

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

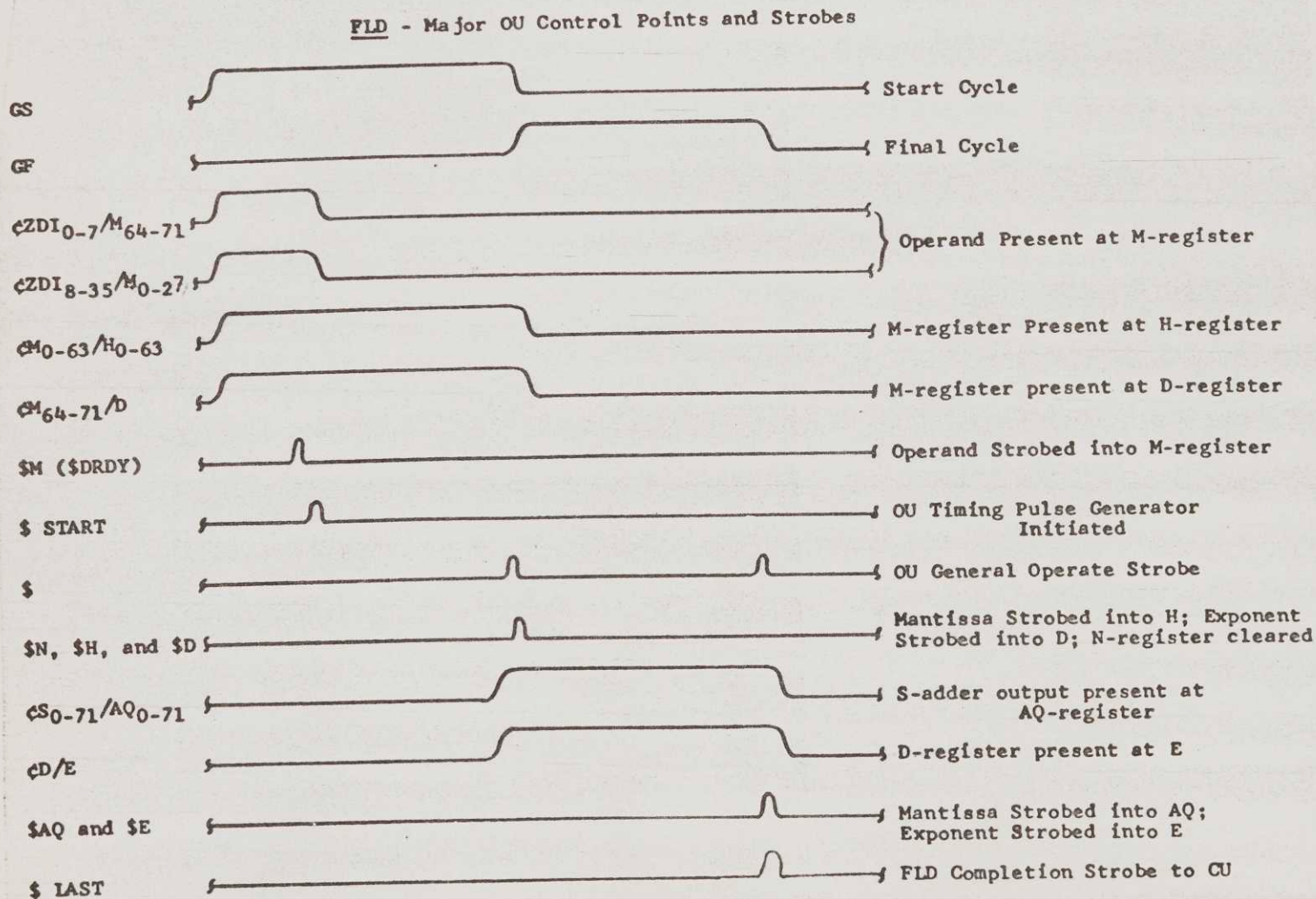


FIG. 12.3.8.1e FLD Instruction, Timing Diagram

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Cont. on Sh. 12-182 Sh. No. 12-181

TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR

Example 2: Add to Exponent Register (ADE)

During this instruction the contents of bits 0-7 of a memory location Y are added to the contents of the E-register and the results are placed in E. The presence of the ADE instruction code on the ZOR lines together with DPFF reset and DIC reset enables the IM-switch. The control points $\phi ZDI_{0-7}/M_{64-71}$ and ZDI_{8-35}/M_{0-28} are enabled presenting the operand lines (ZDI bus) to the proper M-register inputs. When the operand ready strobe (\$ DRDY) is received from the CU, DPFF reset allows the M-register strobe (\$ M₀₋₇₁) to be generated and strobe the ADE operand into the M-register. The \$ DRDY pulse is turned around as \$ YRY and returned to the CU to signal that a new instruction may be prepared. \$ YRY also sets YRY in the OU. When YRY is set the conditions exist to allow \$ START to be generated by a last of three pulse detectors. \$ START sets OUB, resets YRY and DDF, and transfers the operation code from the O-register to the C-register. It also enters the timing pulse generator delay line network.

GS

When the \$ START pulse propagates the medium delay elements, the operate strobe (\$) occurs. This causes the following events:

- 1) \$D which will strobe the ADE exponent into the D-register.
- 2) ZERO and SIGN to reset.
- 3) ORB to reset, indicating that the O-register is free to receive the operation designator for the next instruction.
- 4) GS to reset and GF to set.

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Spec. No. M50EE00107

Cont. on Sh.12-183 Sh. No.12-182

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

GF

The \$ pulse will re-enter the timing pulse generator delay line network. GF being set will delay the pulse 400 nanoseconds before another \$ pulse is generated.

During this 400 nanoseconds control point ϕ D/ES is enabled, which will cause the contents of the E-register and the D-register to be added in the ES-adder. At the same time control point ϕ ES/E is enabled, which will place the sum output of the ES-adder on the inputs to the E-register. The \$ pulse causes the following events:

- 1) A \$ E is generated, which will strobe the new exponent into the E-register.
- 2) EOFL to set if an exponent overflow occurred.
- 3) EUFL to set if an exponent underflow occurred.
- 4) GF to reset.
- 5) OUBF to reset if no other instruction has been initiated.

\$ will generate a \$ LAST, which is sent to the CU to indicate completion of the ADE instruction.

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Spec. No. M50EB00107

Cont. on Sh.12-184 Sh. No.12-183

TITLE:

ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

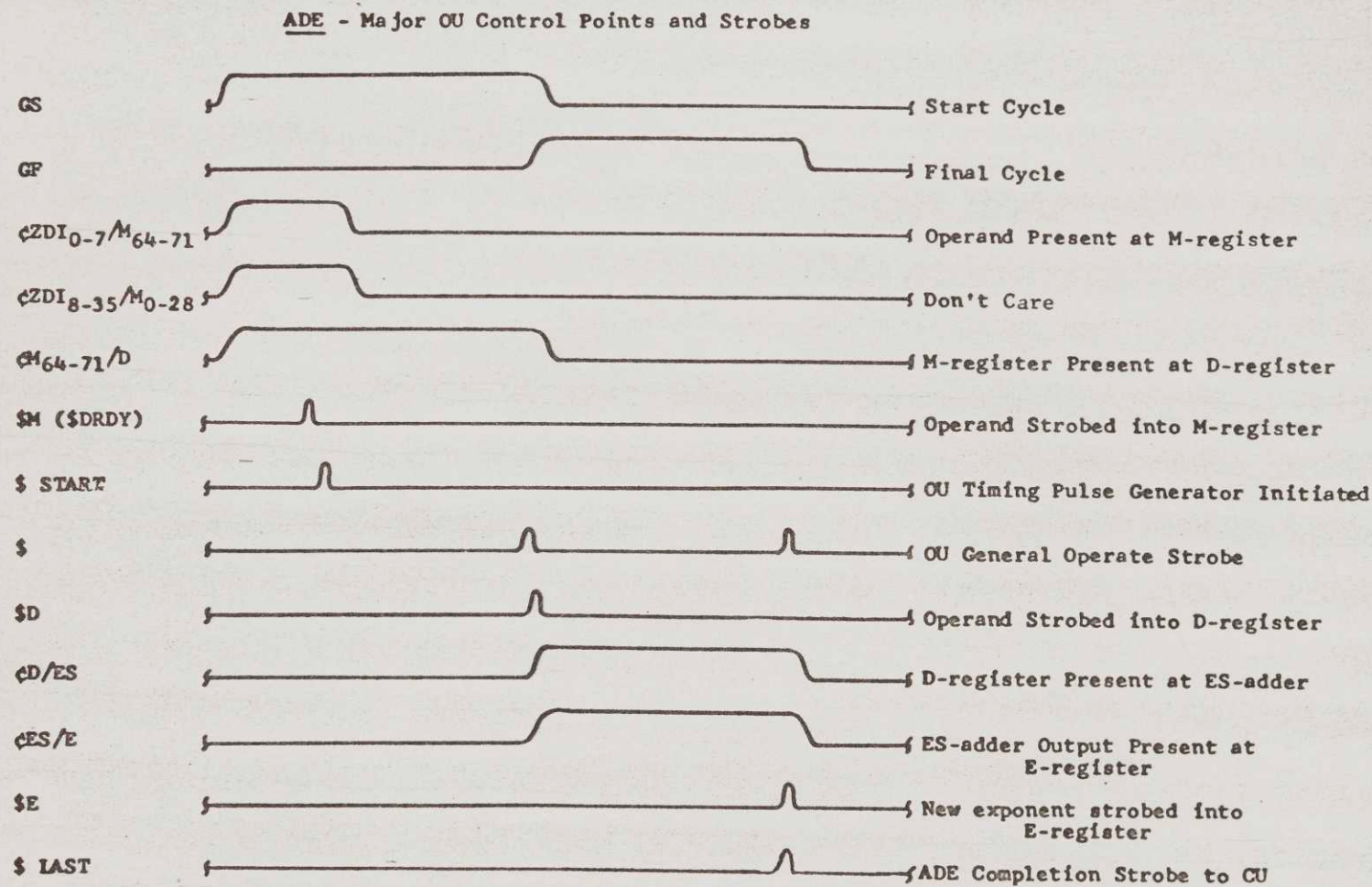


FIG. 12.3.8.1f ADE Instruction, Timing Diagram

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Cont. on Sh.12-185 Sh. No.12-184

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

Example 3: Compare (FCMG)

During this instruction the contents of a memory location Y are magnitude compared with the contents of the Floating Register (EAQ) and the ZERO and SIGN Indicators are set depending on the comparison. In general, this is accomplished by comparing the exponents of both numbers, select the number with the lesser exponent and shift its mantissa right as many places as the difference of the exponents states, then compare the absolute value of the mantissas, and set the indicators accordingly. The effective length of both mantissas is 28 bits (including the sign). A compare is a subtract operation where the register contents are not altered. Since this operation is a compare magnitude, the operands to be compared must be of unlike signs. If the mantissas to be compared are of like signs, the memory mantissa must be two's complemented before the compare is actually made.

The data path from ZDI/M and the generation of \$ START are the same as for the FLD instruction.

GS

During GS the signs of the mantissas (M_0 and A_0) are used to control the transfer of data from M to H. Because of the compare algorithm used, these signs must be opposite. Therefore, if these signs are not different, the IH-switch is enabled by $\phi M_{0-71}/H_{0-71}$ and $\phi M_{64-71}/H_{64-71}$; if the signs are different, the IH-switch is enabled by $\phi M_{0-63}/H_{0-63}$. At the same time $\phi M_{64-71}/D$ enabled causes the exponent to be presented at the inputs to the D-register.

When the \$ START pulse propagates the medium delay elements, the operate strobe (\$) occurs. This causes the following events:

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Cont. on Sh.12-186 Sh. No.12-185

TITLE: ENGINEERING PRODUCT SPECIFICATION
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- 1) \$H is generated, which strobes the mantissa from M into H.
- 2) \$N is generated, which clears N to zero.
- 3) \$D is generated, which strobes the exponent from M into D.
- 4) If the signs of A and M are the same, K₇₂ control flip-flop will be set to force an initial carry into the S-adder.
- 5) ZERO and SIGN to reset.
- 6) ORB to reset.
- 7) GS to reset and GE to set.
- 8) \$ enters the timing pulse generator delay line network to produce another \$ strobe in approximately 400 nanoseconds.

GE

During the GE cycle the two exponents are compared by subtracting D from E. The difference, if any, is stored in the G-counter. The results of this comparison will produce the following results:

- 1) If the difference is equal to zero, transfer the mantissa in AQ to N, leave H as is, and go to GF cycle.
- 2) If the difference is greater than +71, clear N, transfer the mantissa in AQ to H, and go to GF cycle.
- 3) If the difference is less than -71, clear N, leave H as is, and go to GF cycle.

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Cont. on Sh.12-187 Sh. No.12-186

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

- 4) If the difference is positive and less than +72, transfer the mantissa in AQ to H, store the difference in the G-counter and go to GA cycle.
- 5) If the difference is negative and greater than -72 transfer the mantissa in AQ to N, leave H as is, store the one's complement of the difference with the sign bit on in the G-counter and go to GA cycle.

The control lines that become enabled to accomplish these events are:

- 1) $\phi AQ_{0-71}/\phi ZAQ_{0-71}$ unconditionally
- 2) $\phi ZAQ_{0-71}/H_{0-71}$ unconditionally
- 3) $\phi \overline{D_{0-7}}/ES_{0-9}$ unconditionally
- 4) $\phi CARRY/ES_7$ unconditionally
- 5) $*\phi ZAQ_{0-35}/N_{0-35}$ if $[(ES_9) + (S = 0) + (ES = 0)] = 1$

*ZQA bits 28 through 35 are forced to zero.

- 6) $\phi S_{0-71}/N_{0-71}$ if $[(ES_9) + (S = 0) + (ES = 0)] = 1$
- 7) $\phi ES/G$ if $(ES_0) [(ES \neq 0) (/ES / < 72) (ES_9 + S \neq 0)]$
- 8) $\phi \overline{ES}/G$ if $(\overline{ES_0}) [(ES \neq 0) (/ES / < 72) (ES_9 + S \neq 0)]$

At the end of 400 nanoseconds a \$ strobe will cause the following events:

- 1) A \$ H to strobe the mantissa from AQ into H if $\overline{ES_9 + S = 0 + ES = 0}$

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Cont. on Sh.12-188 Sh. No.12-187

TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR

- 2) A \$ N to strobe a mantissa into N if $(/ES/ < 72) + (ES = 0) + (S = 0) (\overline{ES}_9)$
- 3) A \$ G₀₋₇ to strobe the proper count into the G-counter unconditionally.
- 4) LAFF to set if a maximum negative mantissa was two's complemented and transferred to N.
- 5) K₇₂ to reset if the two's complemented mantissa was transferred to N.
- 6) GE to reset unconditionally.
- 7) GA to set if $(ES \neq 0) (/ES/ < 72) (ES_9 + S \neq 0)$.
- 8) GF to set if $(ES = 0) + (/ES/ > 71) + (\overline{ES}_9 \cdot S = 0)$.
- 9) \$ enters the timing pulse generator delay line network to produce another \$ strobe.

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Cont. on Sh.12-189 Sh. No.12-188

TITLE: ENGINEERING PRODUCT SPECIFICATION
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GA

During this cycle the mantissa in N is aligned so that its binary point falls at the same place as that of the mantissa in H. This is accomplished by shifting it right the number of places indicated by the G-counter. The control lines that become enabled to accomplish these events are;

- 1) $\phi N-16$ ($\phi N_0-55/N_{16-71}$, $\phi N_0/N_0-15$) if $(G > 14)$ ($\overline{LAFF}$)
- 2) $\phi N-4$ ($\phi N_0-67/N_{4-71}$, $\phi N_0/N_0-3$) if $(15 > G > 2)$ ($\overline{LAFF}$)
- 3) $\phi N-1$ ($\phi N_0-70/N_{1-71}$, $\phi N_0/N_0$) if $(3 > G > 0)$ ($\overline{LAFF}$)
- 4) $\phi N-1$ ($\phi N_0-70/N_{1-71}$, $\phi \overline{N_0}/N_0$) if LAFF.
- 5) $\phi N+1$ ($\phi N_{1-71}/N_0-70$) if REV set.
- 6) LSA enabled if $(G = 1) + (G = 4) + (G = 16) + (REV)$

At the end of approximately 230 nanoseconds a \$ strobe will cause the following events:

- 1) A \$ N to strobe the shifted contents of N back into N.
- 2) A \$ G to decrement G by 16, if $\phi N = 16$, by 4 if $\phi N-4$, by 1 if $\phi N-1$, or decrement G to zero (0) if $G = 1, 4, \text{ or } 15$.
- 3) LAFF to reset.
- 4) REV to set if $(G = 15) + (G = 3)$
- 5) GA to reset and GF to set if LSA enabled.
- 6) \$ enters the timing pulse generator delay line network to produce another \$ strobe.

GA will be repeated as many times as required to align the mantissa as indicated by LSA enabled.

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Spec. No. M50EB00107

Cont. on Sh.12-190 Sh. No. 12-189

TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR

GF

During GF the contents of the N-and H-registers are subtracted in the S-adder.

On the occurrence of the next \$ strobe, an indicator may be set depending upon the compare. If the mantissa in AQ is equal to the mantissa in Y, the ZERO Indicator is set. If the mantissa in AQ is greater than the mantissa in Y, no indicators are set. If the mantissa in AQ is smaller than the mantissa in Y, the SIGN Indicator is set. This \$ strobe also:

- 1) Resets the GF cycle flip-flop.
- 2) Resets the OUB flip-flop if no other instruction has been initiated.
- 3) Resets the K₇₂ flip-flop.
- 4) Will generate a \$ LAST, which is sent to the CU to indicate completion of the FCMG instruction.

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TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

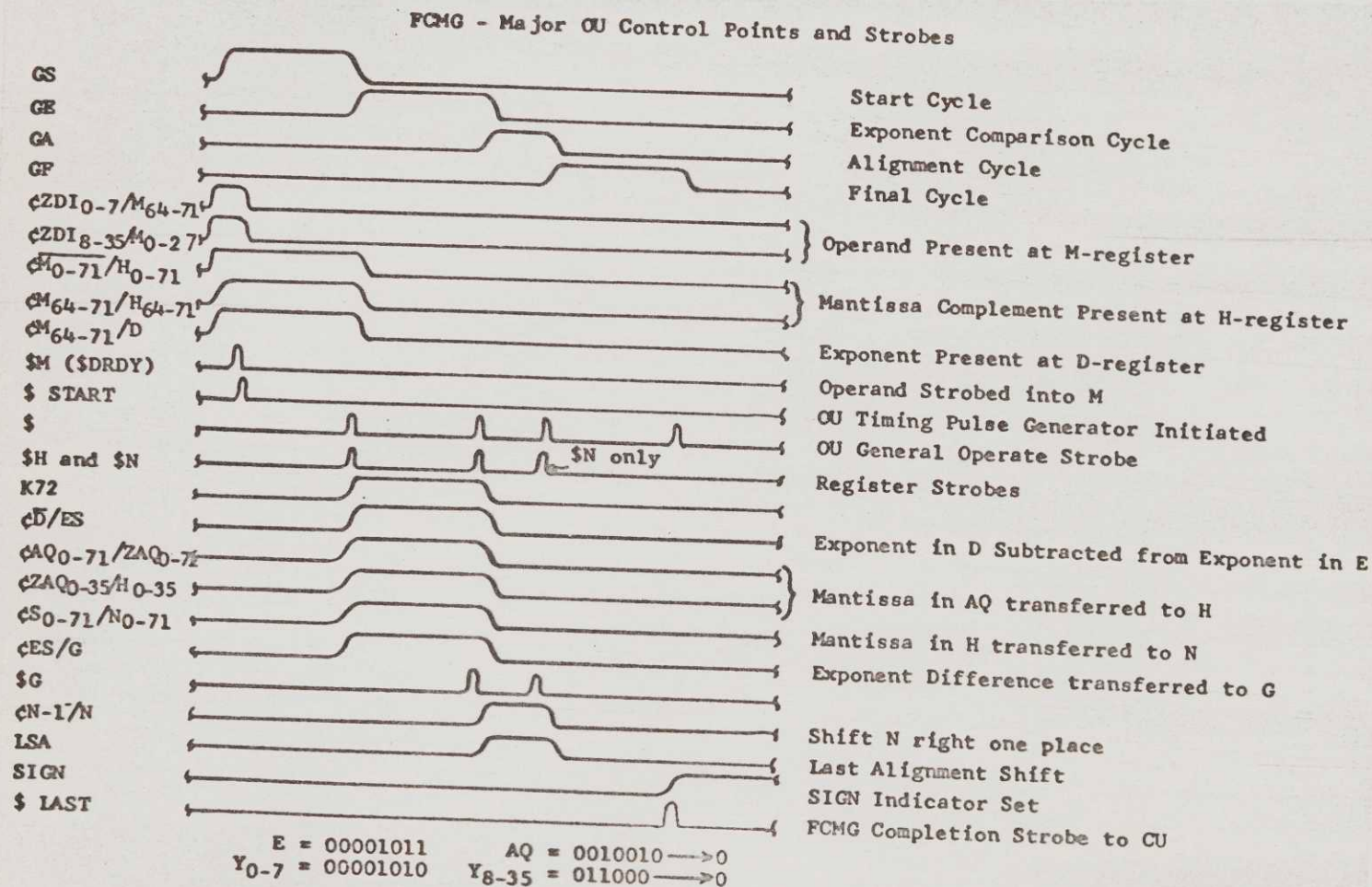


FIG. 12.3.8.1g FCMG Instruction, Timing Diagram

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TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

FCMG

Floating Compare Magnitude

All registers are shown before the strobe at the end of the cycle.

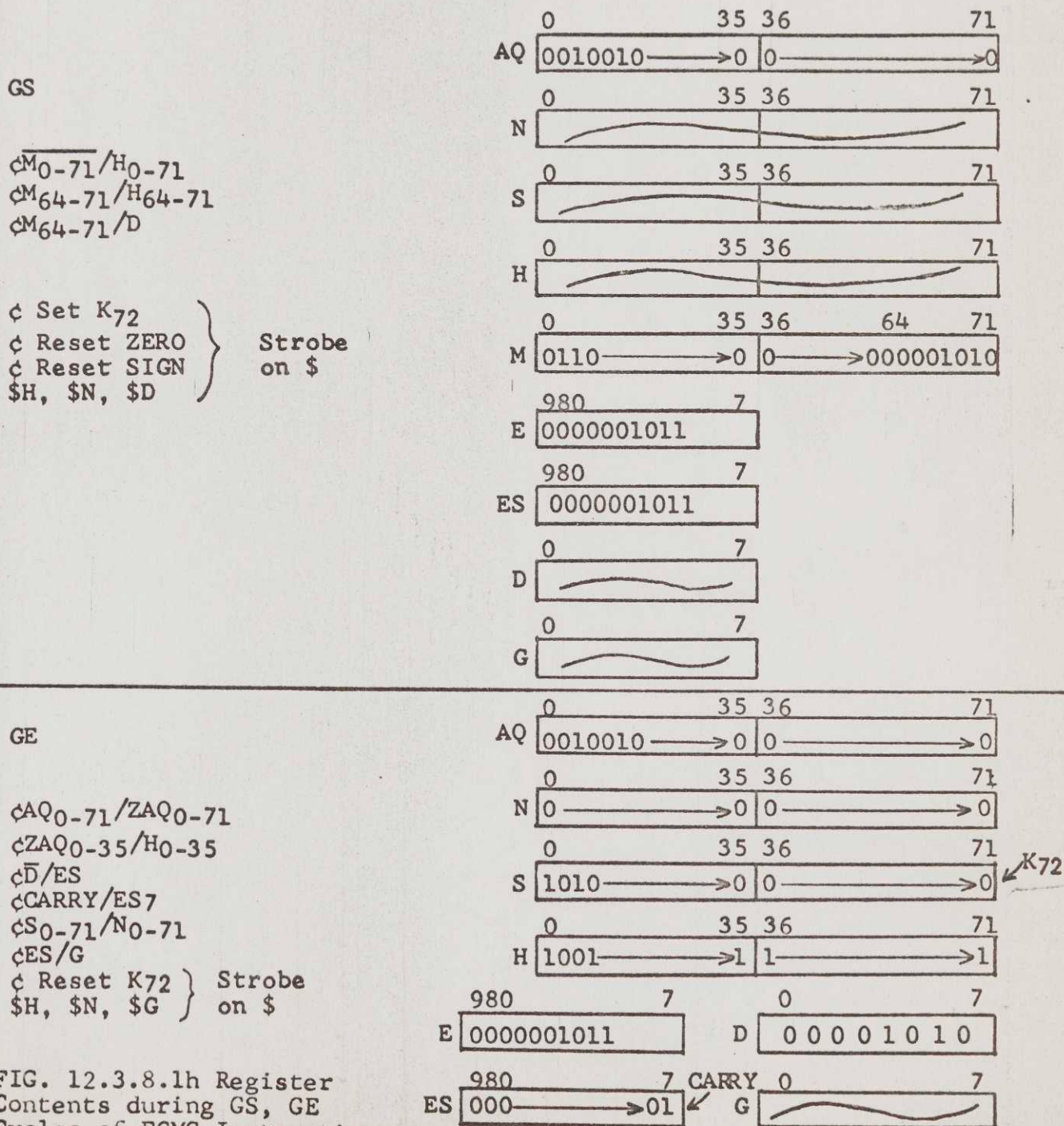


FIG. 12.3.8.1h Register Contents during GS, GE Cycles of FCMG Instruction

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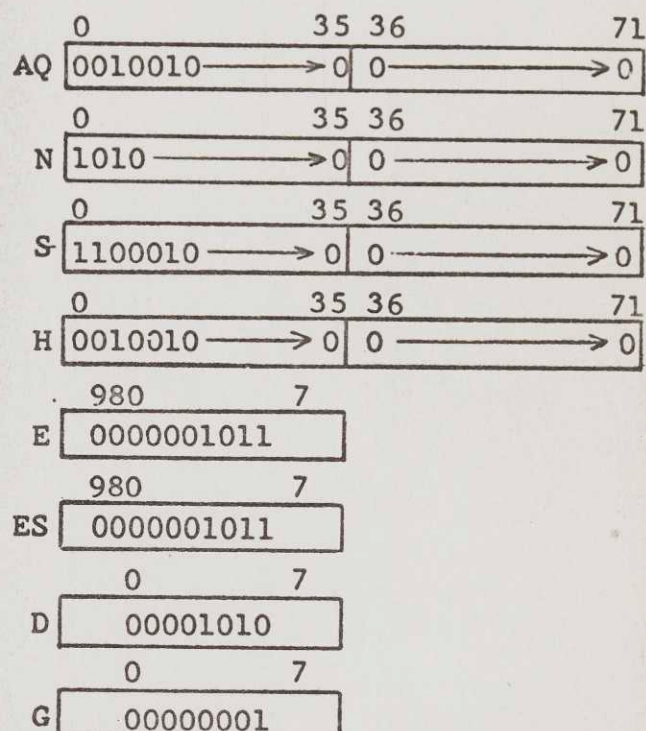
Spec. No. M50EB00107

Cont. on Sh.12-193 Sh. No.12-192

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

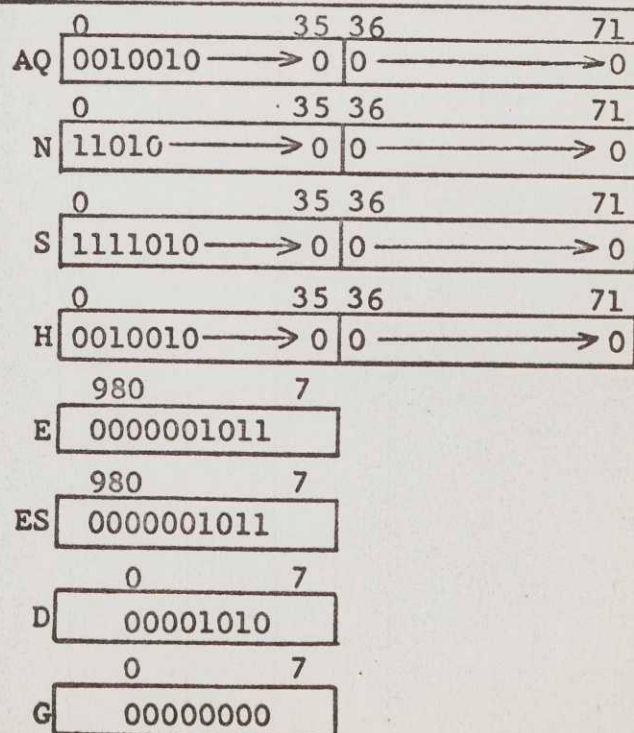
GA

cN-1
c Decrement G by 1 } Strobe
\$N \$G on \$



GF

c Set ZERO if }
S=0 Strobe
c Set SIGN if }
S0=1 on \$



Note: SIGN will set

Fig. 12.3.8.1i Register
Contents during GA, GE
Cycles of FCMG Instruction

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Cont. on Sh. 12-194 Sh. No.12-193

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GE-645 PROTOTYPE PROCESSOR

Example 4: Unnormalized Floating Subtract (UFS)

During this instruction a floating point number in a memory location Y is subtracted from the contents of the Floating Register (EAQ). This is done by first comparing the exponents, then aligning the mantissas, then subtract the mantissas, and then store the difference in EAQ. In this instruction the resultant mantissa is not normalized.

The data path from ZDI/M and the generation of \$ START are the same as for the FLD instruction.

GS

During GS the complement of the mantissa in M is transferred to H, the exponent in M is transferred to D, and the proper indicator and control flip-flops are set up. The control lines that become enabled to accomplish this are:

- 1) $\overline{cM_{0-71}}/H_{0-71}$ and cM_{64-71}/H_{64-71}
- 2) cM_{64-71}/D

When the \$ START propagates the medium delay elements the operate strobe (\$) occurs. This causes the following events:

- 1) A \$ H strobes the complement of the mantissa in M into H.
- 2) A \$ N clears N to zero.
- 3) A \$ D strobes the exponent in M into D.
- 4) ZERO and SIGN to reset.
- 5) K₇₂ to set.
- 6) GS to reset and GE to set.

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Cont. on Sh.12-195 Sh. No.12-194

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

- 7) \$ enters the timing pulse generator delay line network to produce another \$ pulse in approximately 400 nanoseconds.

During the GE cycle the two exponents are compared by subtracting D from E, the difference if any is stored in G, the mantissa is stored in H, and the larger exponent is stored in E. The control lines that become enabled to accomplish this are:

- 1) $\phi \text{AQ0-71/ZAQ0-71}$ unconditionally
- 2) $\phi \text{ZAQ0-71/H0-71}$ unconditionally
- 3) $\phi \text{D/E}$ unconditionally
- 4) $\phi \bar{\text{D}}/\text{ES}$ unconditionally
- 5) $\phi \text{ CARRY/ES}_7$ unconditionally
- 6) $\phi \text{ZAQ0-71/N0-71}$ if $\text{ES}_9 + \text{S} = 0 + \text{ES} = 0$
- 7) $\phi \text{S0-71/N0-71}$ if $\overline{\text{ES}_9 + \text{S} = 0 + \text{ES} = 0}$
- 8) $\phi \text{ES/G}$ if $(\text{ES}_0) [(\text{ES} \neq 0) (/ \text{ES} / < 72) (\text{ES}_9 + \text{S} \neq 0)]$
- 9) $\phi \overline{\text{ES}}/\text{G}$ if $(\overline{\text{ES}_0}) [(\text{ES} \neq 0) (/ \text{ES} / < 72) (\text{ES}_9 + \text{S} \neq 0)]$

At the end of 400 nanoseconds a \$ pulse will cause the following events:

- 1) A \$ H to strobe the mantissa from AQ into H if $\overline{ES}_9 + S = 0 + \overline{ES} = 0$
- 2) A \$ N to strobe a mantissa into N if $/\overline{ES}/ < 72 + \overline{ES} = 0 + (S = 0) (\overline{ES}_9)$

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Spec. No. M50EB00107

Cont. on Sh.12-196 Sh. No.12-195

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

- 3) A \$ E to strobe the exponent from D to E if ES_9
- 4) A \$ G to strobe the proper count into G_{0-7} unconditionally
- 5) LAFF to set if a maximum negative number was two's complemented and transferred to N
- 6) K_{72} to reset if the two's complemented mantissa was transferred to N
- 7) GE to reset
- 8) G_0 to set if $(ES = 0) + (/ES/ > 71) + (ES_9)(S = 0)$
- 9) G_A to set if $(ES \neq 0) (/ES/ < 72) (ES_9 + S \neq 0)$
- 10) \$ enters the timing pulse generator delay line network to produce another \$ pulse.

G_A

During this cycle the mantissa in N is aligned so that its binary point falls at the same place as that of the mantissa in H. This is accomplished by shifting N right the number of places indicated by the G-counter. The control lines that become enabled to accomplish this are:

- 1) $\phi N-16$ ($\phi N_{0-55}/N_{16-71}$, $\phi N_0/N_{0-15}$) if $(G > 14)(\overline{LAFF})$
- 2) $\phi N-4$ ($\phi N_{0-67}/N_{4-71}$, $\phi N_0/N_{0-3}$) if $(15 > G > 2)(\overline{LAFF})$
- 3) $\phi N-1$ ($\phi N_{0-70}/N_{1-71}$, $\phi N_0/0$) if $(3 > G > 0)(\overline{LAFF})$
- 4) $\phi N-1$ ($\phi N_{0-70}/N_{1-71}$, $\phi \overline{N}_0/N_0$) if LAFF
- 5) $\phi N+1$ ($\phi N_{1-71}/N_{0-70}$) if REV

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Spec. No. M50EB00107

Cont. on Sh.12-197 Sh. No.12-196

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

6) LSA enabled if $(G = 1) + (G = 4) + (G = 16) + (REV)$

At the end of approximately 230 nanoseconds a \$ pulse will cause the following events:

- 1) A \$ N to strobe the shifted contents of N back into N.
- 2) A \$ G to decrement G by 16 if $\phi N - 16$, by 4 if $\phi N - 4$, by 1 if $\phi N - 1$, or increment G by 1 if $\phi N + 1$.
- 3) REV to set if $(G = 15) + (G = 3)$.
- 4) GA to reset and GO to set if LSA enabled.
- 5) \$ enters the timing pulse generator delay line network to produce another \$ pulse.

GA will be repeated as many times as required to align the mantissa as indicated by LSA enabled.

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Cont. on Sh. 12-198 Sh. No. 12-197

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

GO

During this cycle the complemented mantissa is added to the other mantissa in the S-adder producing the difference. This difference is stored in N, H and G are cleared to zero, and the proper indicators are set. The control line that becomes enabled to accomplish this is:

$\phi S_{0-71}/N_{0-71}$ to transfer the output of the S-adder to N.

At the end of 400 nanoseconds a \$ pulse will cause the following events:

- 1) A \$ H that clears H to zero.
- 2) A \$ N that strobes the mantissa difference into N.
- 3) REV to set if an overflow occurred.
- 4) SIGN to set if the difference is zero.
- 6) CARRY to set if there is a carry out of bit position zero.
- 7) CARRY to reset if there is no carry out of bit position zero.
- 8) K₇₂ to reset.
- 9) GO to reset.
- 10) GN to set if an overflow occurred.
- 11) GF to set if no overflow occurred.
- 12) \$ enters the timing pulse generator delay line network to produce another \$ pulse.

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Spec. No. M50EB00107

Cont. on Sh.12-199 Sh. No.12-198

TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR

GN

During this cycle a mantissa that has overflowed is shifted one place right and the G-counter is decremented by one. The control line that becomes enabled to accomplish this is:

$\phi N-1 (\phi N_{0-70}/N_{1}/N_{71}, \phi \overline{N_0}/N_0)$

At the end of 230 nanoseconds a \$ pulse will cause the following events:

- 1) A \$ N to strobe the shifted contents of N back into N.
- 2) A \$ G to decrement the G-counter by one.
- 3) REV to reset.
- 4) GN to reset and GF to set.
- 5) \$ enters the timing pulse generator delay line network to produce another \$ pulse.

GF

During this cycle the mantissa in N is transferred to AQ, the count in G is subtracted from the exponent in E, and EOFL is set if required. If the mantissa is zero, the exponent will be forced to -128. The control lines that become enabled to accomplish this are:

- 1) $\phi S_{0-71}/AQ_{0-71}$
- 2) $\phi G/ES$ and $\phi CARRY/ES_7$

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Cont. on Sh.12-200 Sh. No.12-199

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

- 3) $\phi ES/E$ if mantissa $\neq$ zero
- 4) $\phi -2^7 /E$ if mantissa = zero

At the end of 400 nanoseconds a \$ pulse will cause the following events to happen:

- 1) A \$ AQ to strobe the mantissa into AQ.
- 2) A \$ E to strobe the exponent into E.
- 3) EOFL to set if the subtraction of G from E caused the exponent to exceed +127.
- 4) GF to reset.
- 5) OUBF to reset if no other instruction has been initiated.
- 6) \$ will generate a \$ LAST, which is sent to the CU to indicate completion of the UFS instruction.

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Spec. No. M50EB00107

Cont. on Sh.12-201 Sh. No.12-200

TITLE:

ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

UFS - Major OU Control Points and Strobes

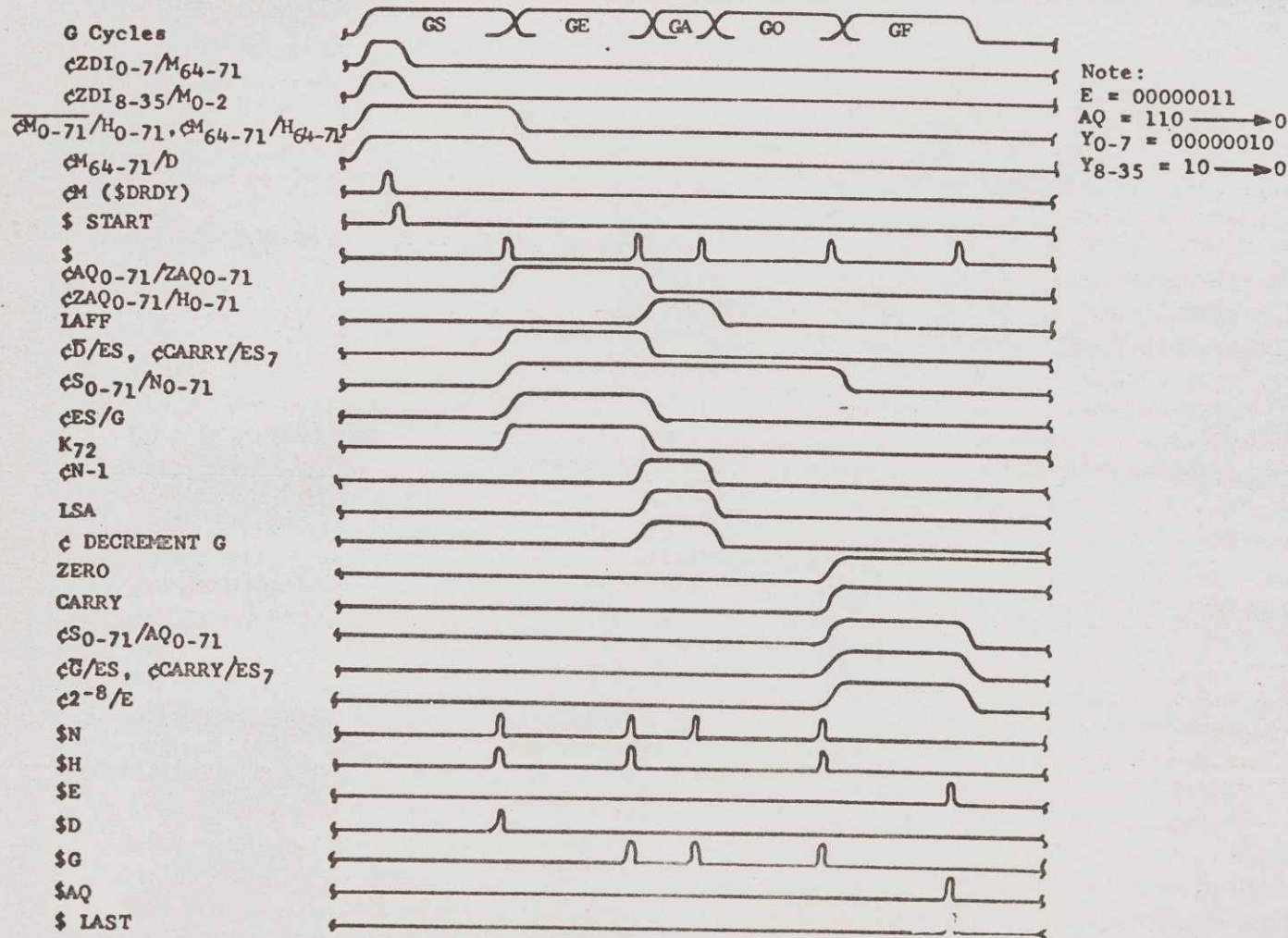


FIG. 12.3.8.1j UFS Instruction, Timing Diagram

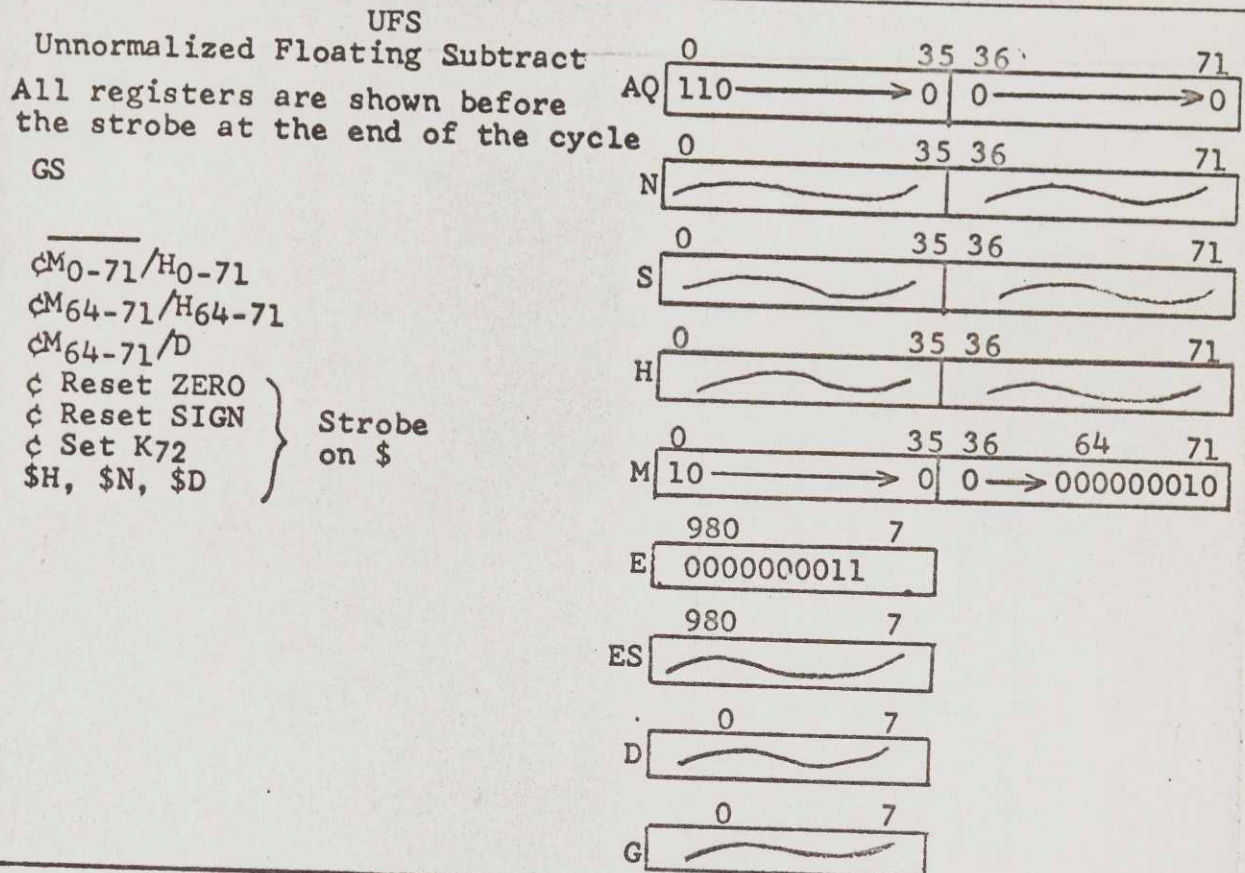
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Spec. No. M50EB00107

Cont. on Sh.12-202 Sh. No.12-201

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR



GE

$\overline{CAQ}0-71/ZAQ0-71$
 $\overline{CZAQ}0-71/H0-71$
 $\overline{CD}/E$
 $\overline{CD}/ES$
 $\overline{C}$ CARRY/ES7
 $\overline{CS}0-71/N0-71$ of $\overline{ES}9$
 $\overline{CES}/G$ if $0 < ES < 72$
 $\overline{C}$ Set LAFF
 $\overline{C}$ Reset K72
 $\$H, \$N, \$G$

} Strobe on \$

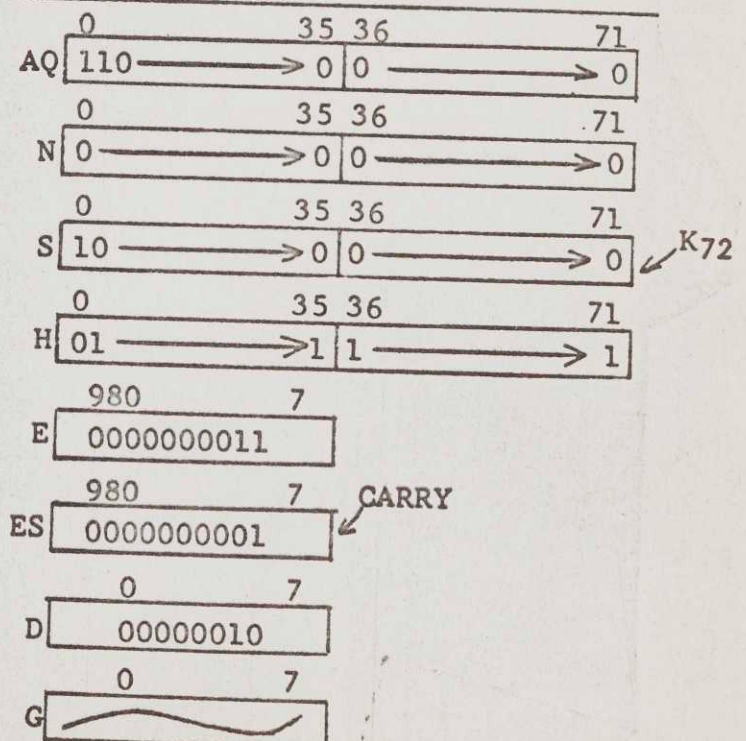


FIG. 12.3.8.1k Register Contents during GS, GE Cycles of UFS Instruction

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Spec. No. M50EB00107

Cont. on Sh.12-203 Sh. No.12-202

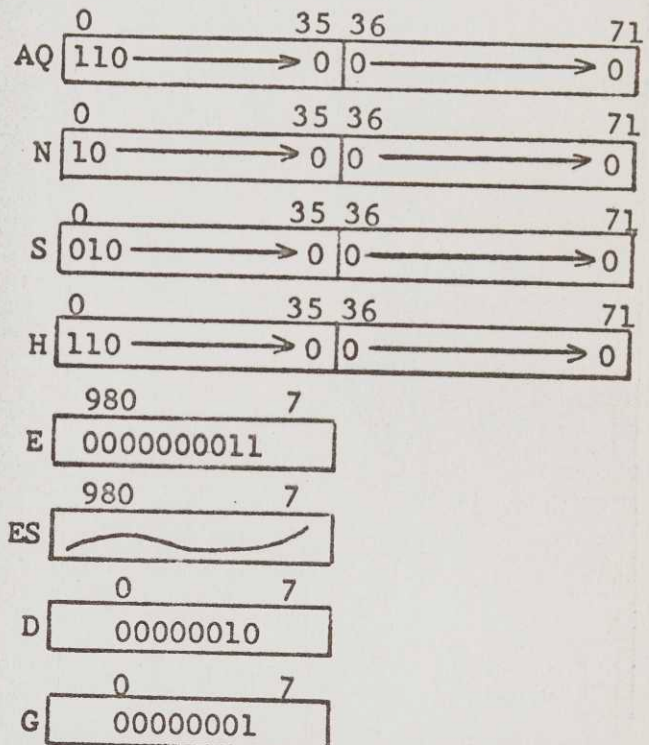
TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645v PROTOTYPE PROCESSOR

GA

$\bar{c}N-1$ ($\bar{c}N_0-70/N_1-71$, $\bar{c}\bar{N}_0/N_0$)
 $\bar{c}$ Reset LAFF
LSA
 $\bar{c}$ Decrement G by 1
\$N, \$G } Strobe on \$

Note:

Only one GA cycle



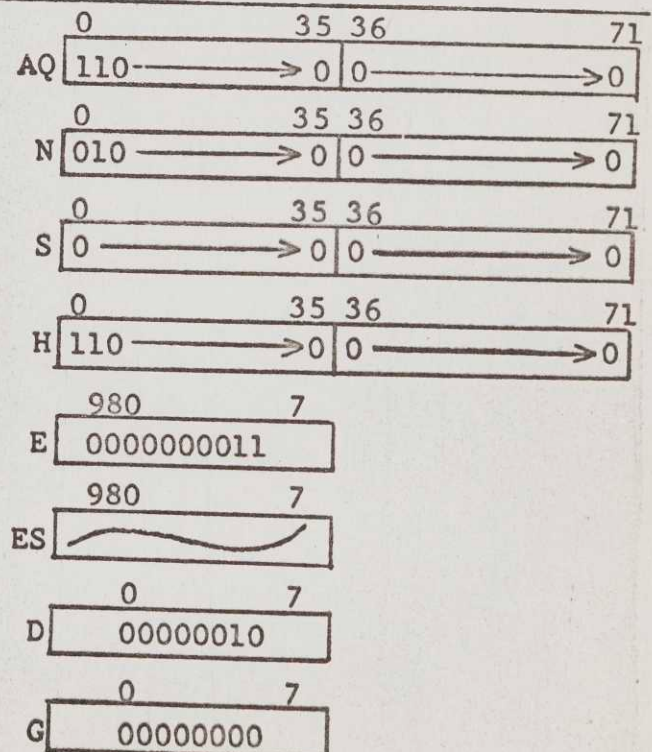
GO

$\bar{c}S_0-71/N_0-71$
 $\bar{c}$ Set ZERO if $S=0$
 $\bar{c}$ Set CARRY if there is a carry out of S_0 } Strobe on \$
\$H, \$N, \$G

Note:

ZERO and CARRY will set

FIG. 12.3.8.1m Register
Contents during GA, GO
Cycles of UFS Instruction



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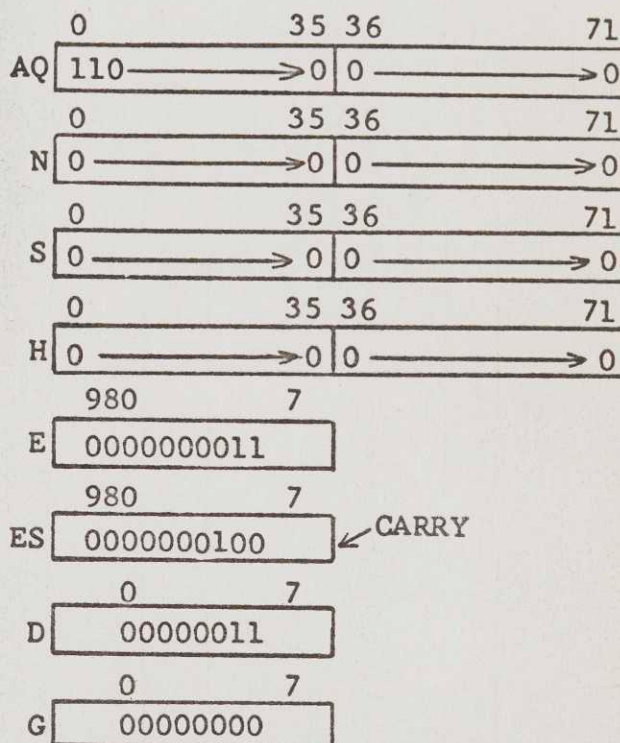
Spec. No. M50EB00107

Cont. on Sh.12-204 Sh. No.12-203

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

GF

$\bar{c}S_{0-71}/AQ_{0-71}$
 $\bar{c}G/ES$
 $\bar{c} CARRY/ES_7$
 $\bar{c}-2^7/E$ if $S=0$
\$AQ, \$E } strobe on \$



Contents of the registers upon completion of the UFS operation

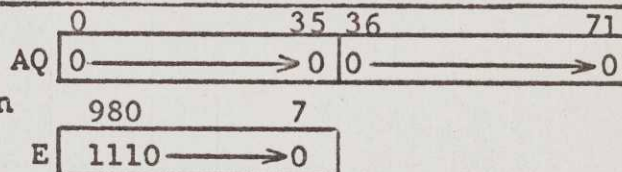


FIG. 12.3.8.1n Register Contents during GF Cycle of UFS Instruction

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TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

12.3.8.2 Double Precision

The instructions comprising the double precision floating point add group can be defined by two classifications:

- 1) Instructions requiring normalization (DFAD and DFSB).
- 2) Instructions that do not require normalization (DFCMG, DFCMP, DFLD, DUFA, and DUFS).

The only difference in the OU between these instructions and the corresponding single precision instructions in the floating point add group is that these instructions manipulate a mantissa of 64 bits instead of 28 bits, and two \$DRDYs are required instead of one.

Normalized

Under this heading fall the two instructions DFAD and DFSB.

Example 1: Subtract (DFSB)

During this instruction a double precision floating point number in a memory location Y and Y + 1 is subtracted from the contents of the Floating Register (EAQ). This is done by first comparing the exponents, then aligning the mantissas, then subtracting the mantissas, then normalize the difference, and then store the difference in EAQ.

The IM-switch is enabled by the presence of the DFSB decode together with DPFF, BCFF, and DIC all reset. The control points $\text{\textcircled{C}}\text{ZDI}_{0-7}/\text{M}_{64-71}$ and $\text{\textcircled{C}}\text{ZDI}_{8-35}/\text{M}_{0-27}$ are enabled to allow the ZDI bus to be present at the proper M-register inputs. When the first \$DRDY is received from the CU the Double Precision flip-flop (DPFF) not yet being set allows

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

\$M₀₋₇₁ to be generated and strobe the exponent and most significant 28 bits of the mantissa into the M-register. This \$DRDY will set DPFF, but will not generate a \$ START. On the setting of DPFF, the IM-switch becomes enabled by ϕ ZDI_{0-7/M28-35} and ϕ ZDI_{8-35/M35-63}.

About 250 nanoseconds after the first \$DRDY another \$DRDY will be received. When the second \$DRDY is received DPFF set allows \$M₂₈₋₆₃ to be generated and strobe the least significant 36 bits of the mantissa into the M-register. This \$DRDY pulse resets DPFF and is turned around as \$YRY and returned to the CU to signal that a new instruction may be prepared. \$YRY sets the operand ready flip-flop (YRY) in the OU. When YRY is set, the conditions exist to allow a \$START which sets OUB, resets YRY and DDF, and transfers the operation code from the O-register to the C-register. It also enters the timing pulse generator delay line network.

GS

During this cycle the complement of the mantissa in M is transferred to H, the exponent in M is transferred to D, and the proper indicator and control flip-flops are set up. The control lines that become enabled to accomplish this are:

- 1) ϕ M_{0-71/H0-71} and ϕ M_{64-71/H64-71}.
- 2) ϕ M_{64-71/D}

When the \$START propagates the medium delay elements the operate strobe (\$) occurs. This pulse causes the following events:

- 1) A \$H to strobe the complement of the mantissa in M into H.
- 2) A \$N to clear N to zero.

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Spec. No. M50EB00107

Cont. on Sh. 12-207 Sh. No. 12-206

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

- 3) A \$D to strobe the exponent in M into D.
- 4) ZERO and SIGN to reset.
- 5) K72 to set.
- 6) GS to reset and GE to set.
- 7) \$ enters the timing pulse generator delay line network to produce another \$ pulse.

GE

During this cycle the two exponents are compared by subtracting D from E, the difference if any is stored in G. the mantissa with the lesser exponent is stored in N, the other mantissa is stored in H, and the larger exponent is stored in E. The control lines that become enabled to accomplish this are:

- 1) $\phi AQ_0-71 / ZA Q_0-71$ unconditionally
- 2) $\phi ZA Q_0-71 / H_0-71$ unconditionally
- 3) $\phi D/E$ unconditionally.
- 4) $\phi \bar{D}/ES$ and $\phi CARRY/ES_7$ unconditionally
- 5) $\phi ZA Q_0-71 / N_0-71$ if $ES_9 + S = 0 + ES = 0$.
- 6) $\phi S_0-71 / N_0-71$ if $\overline{ES_9 + S = 0 + ES = 0}$.
- 7) $\phi ES/G$ if $(ES_0) (ES \neq 0)(ES \neq 71)(ES_9 + S \neq 0)$
- 8) $\phi \bar{ES}/G$ if $(\bar{ES}_0) (ES \neq 0)(ES \neq 71) (ES_9 + S \neq 0)$

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Spec. No. M50EB00107

Cont. on Sh.12-208 Sh. No.12-207

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

At the end of 400 nanoseconds a \$ pulse will cause the following events:

- 1) A \$H to strobe the mantissa from AQ into H if $ES_9 + s = 0 + ES = 0$.
- 2) A \$N to strobe a mantissa into N if $/ES/ < 72 + ES = 0 + (S = 0)(ES_9)$.
- 3) A \$E to strobe the exponent from D into E if ES_9 .
- 4) A \$G to strobe the proper count into G unconditionally.
- 5) LAFF to set if a maximum negative number was two's complemented and transferred to N.
- 6) K_{72} to reset if the two's complemented mantissa was transferred to N.
- 7) GE to reset.
- 8) GO to set if $ES = 0 + /ES/ > 71 + (\overline{ES_9})(S = 0)$.
- 9) GA to set if $(ES \neq 0) (/ES/ < 72) (ES_9 + S \neq 0)$.
- 10) \$ enters the timing pulse generator delay line network to produce another \$ pulse.

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Spec. No. M50EB00107

Cont. on Sh.12-209 Sh. No.12-208

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GA

During this cycle the mantissa in N is aligned so that its binary point falls at the same place as that of the mantissa in H. This is accomplished by shifting N right the number of places indicated by the G-counter. The control lines that become enabled to accomplish this are:

- 1) $\phi N-16$ ($\phi N_0-55/N_{16-71}$, $\phi N_0/N_0-15$) if $(G > 14)(\overline{\text{LAFF}})$
- 2) $\phi N-4$ ($\phi N_0-67/N_4-71$, $\phi N_0/N_0-3$) if $(15 > G > 2)(\overline{\text{LAFF}})$
- 3) $\phi N-1$ ($\phi N_0-70/N_1-71$, $\phi N_0/N_0$) if $(3 > G > 0)(\overline{\text{LAFF}})$
- 4) $\phi N-1$ ($\phi N_0-70/N_1-71$, $\phi \overline{N_0}/N_0$) if LAFF.
- 5) $\phi N+1$ ($\phi N_1-71/N_0-70$) if REV.
- 6) LSA enabled if $G = 1 + G = 4$, $+ G = 16 + \text{REV}$.

At the end of 230 nanoseconds a \$ pulse will cause the following events:

- 1) A \$N to strobe the shifted contents of N back into N.
- 2) A \$G to decrement G by 16 if $\phi N-16$, by 4 if $\phi N-4$, by 1 if $\phi N-1$, or increment G by 1 if $\phi N+1$.
- 3) REV to set if $(G = 15) + (G = 3)$.
- 4) GA to reset and GO to set if LSA enabled.
- 5) \$ enters the timing pulse generator delay line network to produce another \$ pulse.

GA will be repeated as many times as required to align the mantissa and will terminate on the first \$ pulse following the enabling of LSA.

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Spec. No. M50EB00107

Cont. on Sh.12-210 Sh. No.12-209

TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR

GO

During this cycle the complemented mantissa is added to the other mantissa in the S-adder producing the difference. This difference is stored in N, H is cleared to zero, and the proper indicators are set. The control line that becomes enabled to accomplish this is:

1) $\phi S_{0-71}/N_{0-71}$

At the end of 400 nanoseconds a \$ pulse will cause the following events:

- 1) A \$H to clear H to zero.
- 2) A \$N to strobe the mantissa difference into N.
- 3) REV to set if an overflow occurred.
- 4) SIGN to set if the difference is negative and no overflow occurred.
- 5) ZERO to set if the difference is zero.
- 6) CARRY to set if there is a carry out of bit position 0.
- 7) CARRY to reset if there is no carry out of bit position 0.
- 8) K₇₂ to reset.
- 9) GO to reset.
- 10) GN to set if an overflow occurred or if S₀ and S₁ are the same.
- 11) GF to set if no overflow occurred and S₀ = S₁.
- 12) \$ enters the timing pulse generator delay line network to produce another \$ pulse.

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Cont. on Sh.12-211 Sh. No.12-210

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GN

During this cycle the mantissa in N is normalized. If an overflow occurred during GO the mantissa is shifted one place right with opposite sign inserted and the G-counter is decremented to (-1). In all other cases the mantissa is shifted left until N_0 and N_1 are not alike and the G-counter is incremented by 1 for each place that the mantissa is shifted. The control lines that become enabled to accomplish this are:

- 1) $\phi N-1$ ($\phi N_{0-71}/N_{1-71}$, $\overline{\phi N_0}/N_0$) if REV set.
- 2) $\phi N+16$ ($\phi N_{16-71}/N_{0-55}$) if N_0 through N_{15} are all the same.
- 3) $\phi N+4$ ($\phi N_{4-71}/N_{0-67}$) if $\overline{\phi N+16}$ and N_0 through N_3 are all the same.
- 4) $\phi N+1$ ($\phi N_{1-71}/N_{0-70}$) if $(\overline{\phi N+16})(\overline{\phi N+4})$ and $N_0 = N_1$.
- 5) LSN enabled if $(\phi N+16) (N_{15} = N_{16} \neq N_{17}) + (\phi N+4) (N_3 = N_4 \neq N_5) + (\phi N+1) (N_0 = N_1 \neq N_2) + (REV)$.

At the end of 230 nanoseconds a \$ pulse will cause the following events.

- 1) A \$N to strobe the shifted contents of N back into N.
- 2) A \$G to increment the G-counter by 16 if $\phi N+16$, by 4 if $\phi N+4$, by 1 if $\phi N+1$, or decrement G by 1 if REV is set.
- 3) REV to set if $(\phi N+16) (N_{15} \neq N_{16}) + (\phi N+4) (N_3 \neq N_4)$.

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- 4) REV to reset if REV is set.
- 5) GN to reset and GF to set if LSN enabled.
- 6) \$ enters the timing pulse generator delay line network to produce another \$ pulse.

GN will be repeated as many times as required to normalize the mantissa and will terminate on the first \$ pulse following the enabling of LSN.

GF

During this cycle the mantissa in N is transferred to AQ, the count in G is subtracted from the exponent in E, and EOFL and EUFL are set if required. If the mantissa is zero the exponent will be forced to -128. The control lines that become enabled to accomplish this are:

- 1) $\phi S_0-71/AQ_0-71$.
- 2) $\phi \bar{G}/ES$ and $\phi CARRY/ES_7$.
- 3) $\phi ES/E$ if mantissa $\neq 0$.
- 4) $\phi -2^7/E$ if mantissa = 0.

At the end of 400 nanoseconds a \$ pulse will cause the following events:

- 1) A \$AQ to strobe the mantissa into AQ.
- 2) A \$E to strobe the exponent into E.
- 3) EOFL to set if the subtraction of G from E caused the exponent to exceed +127.

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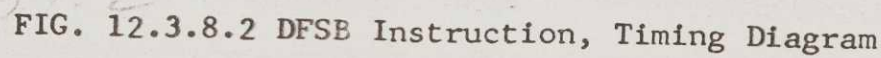
TITLE: ENGINEERING PRODUCT SPECIFICATION
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- 4) EUFL to set if the subtraction of G from E caused the exponent to become smaller than -128.
- 5) GF to reset.
- 6) OUBF to reset if no other instruction has been initiated.
- 7) \$ will generate a \$LAST, which is sent to the CU to indicate completion of the DFSB instruction.

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Cont. on Sh. 12-214 Sh. No. 12-213

ENGINEERING PRODUCT SPECIFICATION GE-645 PROTOTYPE PROCESSOR



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DFSB - Double Precision Floating Subtract Normalized

All registers are shown before the AQ strobe at the end of the cycle

GS

CM0-71/H0-71

CM64-71/H64-71

CM64-71/D

Reset ZERO

Reset SIGN

Set K72

\$H, \$N, \$D

Strobe
on \$

0 35 36 71
AQ 0110010 → 0 111010 → 0

0 35 36 71
N

0 35 36 71
S

0 35 36 71
H

0 35 36 64 71
M 01100 → 0 0 → 010000011

980 7
E 1110000011

980 7
ES

0 7
D

0 7
G

GE

CAQ0-71/ZAQ0-71

CZAQ0-71/H0-71

CD/E

CD/ES

CARRY/ES7

CZAQ0-71/N0-71 if ES = 0

\$N, \$G - Strobe on \$

0 35 36 71
AQ 0110010 → 0 111010 → 0

0 35 36 71
N 0 → 0 0 → 0

0 35 36 71
S 1010 → 0 0 → 0

0 35 36 71
H 1001 → 1 1 → 1

980 7
E 1110000011

980 7
ES 0000000000

0 7
D 10000011

0 7
G

Note:

The next cycle will be a
GO because ES = 0

FIG. 12.3.8.2a Register
Contents during GS, GE
Cycles of DFSB Instruction

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TITLE: ENGINEERING PRODUCT SPECIFICATION
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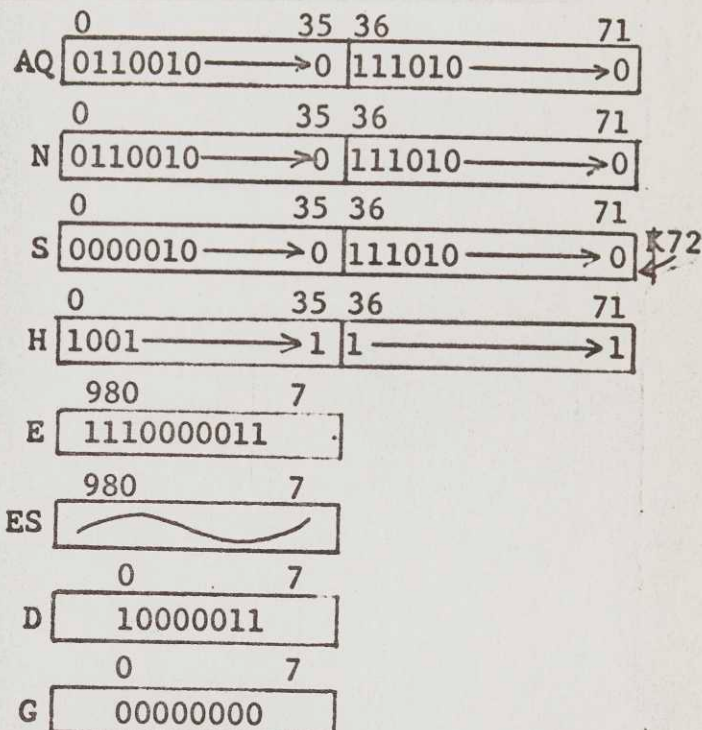
GO

$\phi S_0-71/N_0-71$

ϕ Set CARRY if carry
out of S_0
 ϕ Reset K_{72}
 $\$H, \$N, \$G$

Strobe
on $\$$

CARRY will set



GN

$\phi N+4(\phi N_4-71/N_0-67)$

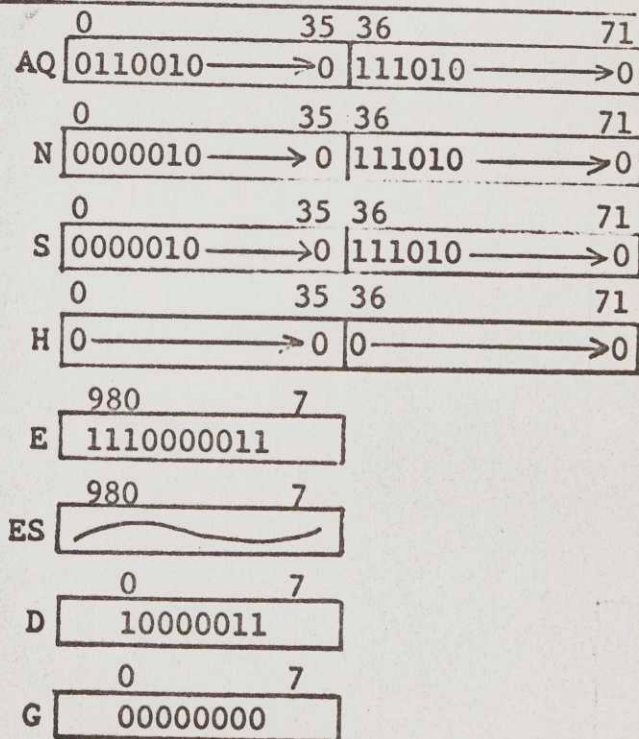
LSN

ϕ Increment G by 4
 $\$N, \G - Strobe on $\$$

Note:

Last GN cycle

FIG. 12.3.8.2b Register
Contents during GO, GN
Cycles of DFSB Instruction



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TITLE: ENGINEERING PRODUCT SPECIFICATION
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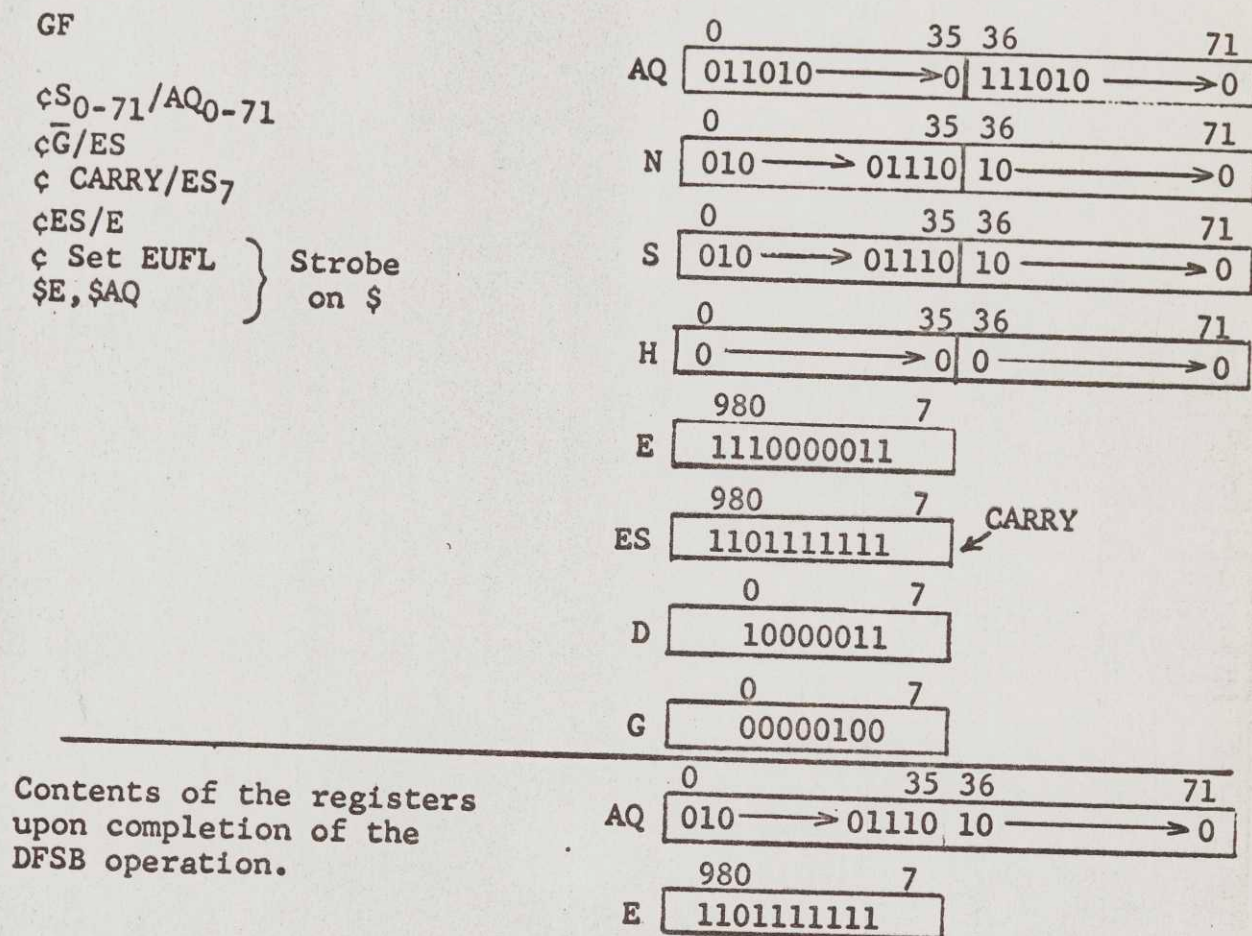


FIG. 12.3.8.2c Register Contents during GF Cycle of DFSB Instruction

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Cont. on Sh.12-218 Sh. No.12-217

TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR

12.3.8.2-contd

Unnormalized

Under this heading fall the instructions DFCMG, DFCMP, DFLD, DUFA, and DUFS.

Example 1: Compare (DFCMP)

During this instruction the contents of memory locations Y and Y + 1 are compared with the contents of the Floating Register (EAQ) bits 0 through 63 and the Zero and Sign Indicators are set depending upon the results of the comparison. In general, this is accomplished by comparing the exponents of both numbers, selecting the number with the algebraically smaller exponent and shifting its mantissa right as many places as the difference of exponents states, then compare the mantissas, and set the indicators accordingly. The effective length of both mantissas is 64 bits (including sign). A compare is a subtract operation where the register contents are not altered. Since this operation is a straight compare the mantissa from memory is two's complemented and thus subtracted from the mantissa in AQ.

The data path from ZDI/M and the generation of \$START are the same as for the DFSB instruction.

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Cont. on Sh.12-219 Sh. No.12-218

TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR

GS

During this cycle the complement of the mantissa in M is transferred to H, the exponent in M is transferred to D, and the proper indicator and control flip-flops are set up. The control lines that become enabled to accomplish this are:

- 1) $\overline{cM_{0-71}}/H_{0-71}$ and cM_{64-71}/H_{64-71} .
- 2) cM_{64-71}/D .

When the \$START propagates the medium delay elements the operate strobe (\$) occurs. This pulse causes the following events:

- 1) A \$H to strobe the complement of the mantissa in M into H.
- 2) A \$N to clear N to zero.
- 3) A \$D to strobe the exponent in M into D.
- 4) ZERO and SIGN to reset.
- 5) K_{72} to set.
- 6) GS to reset and GE to set.
- 7) \$ enters the timing pulse generator delay line network to produce another \$ pulse.

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Cont. on Sh.12-220 Sh. No.12-219

TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR

GE

During this cycle the two exponents are compared by subtracting D from E, the difference if any is stored in G, the mantissa with the lesser exponent is stored in N, and the other mantissa is stored in H. The control lines that become enabled to accomplish this are:

- 1) $\phi AQ_{0-71}/ZAQ_{0-71}$ unconditionally
- 2) $\phi ZAQ_{0-71}/H_{0-71}$ unconditionally
- 3) $\phi \bar{D}/ES$ and $\phi CARRY/ES_7$ unconditionally.
- 4) $\phi ZAQ_{0-71}/N_{0-71}$ if $ES_9 + S = 0 + ES = 0$.
- 5) $\phi S_{0-71}/N_{0-71}$ if $\overline{ES_9 + S = 0 + ES = 0}$.
- 6) $\phi ES/G$ if $(ES_0) [(ES \neq 0)(ES \neq 71)(ES_9 + S \neq 0)]$
- 7) $\phi \bar{ES}/G$ if $(\bar{ES}_0) [(ES \neq 0)(ES \neq 71)(ES_9 + S \neq 0)]$

At the end of 400 nanoseconds a \$ pulse will cause the following to happen:

- 1) A \$H to strobe the mantissa from AQ into H if $\overline{ES_9 + S = 0 + ES = 0}$.
- 2) A \$N to strobe a mantissa into N if $(/ES/ < 72) + (ES = 0) + (S = 0) (\overline{ES_9})$.
- 3) A \$G to strobe the proper count into G.
- 4) LAFF to set if a maximum negative mantissa was two's complemented and transferred to N.
- 5) K_{72} to reset if the two's complemented mantissa was transferred to N.
- 6) GE to reset unconditionally.

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Cont. on Sh.12-221 Sh. No. 12-220

TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR

- 7) GA to set if $(ES \neq 0)(/ES/ < 72) + (ES_9 + S \neq 0)$.
- 8) GF to set if $(ES = 0) + (/ES/ > 72) + (\overline{ES_9})(S = 0)$.
- 9) \$ enters the timing pulse generator delay line network to produce another \$ pulse.

GA

During this cycle the mantissa in N is aligned so that its binary point falls at the same place as that of the mantissa in H. This is accomplished by shifting N right the number of places indicated by the G-counter. The control lines that become enabled to accomplish this are:

- 1) $\phi N-16$ ($\phi N_0-55/N_{16-71}$, $\phi N_0/N_0-15$) if $(G > 14)(\overline{LAFF})$
- 2) $\phi N-4$ ($\phi N_0-67/N_{4-71}$, $\phi N_0/N_0-3$) if $(15 > G > 2)(\overline{LAFF})$
- 3) $\phi N-1$ ($\phi N_0-70/N_{1-71}$, $\phi N_0/N_0$) if $(3 > G > 0)(\overline{LAFF})$.
- 4) $\phi N-1$ ($\phi N_0-70/N_{1-71}$, $\overline{\phi N_0}/N_0$) if $(LAFF)$.
- 5) $\phi N+1$ ($\phi N_{1-71}/N_0-70$) if REV.
- 6) LSA enabled if $(G = 1) + (G = 4) + (G + 16) + (REV)$.

At the end of 230 nanoseconds a \$ pulse will cause the following events:

- 1) A \$N to strobe the shifted contents of N back into N.
- 2) A \$G to decrement G by 16 if $\phi N-16$, by 4 if $\phi N-4$, by 1 if $\phi N-1$, or increment G by 1 if $\phi N+1$, or clear G if LSA is enabled.

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Cont. on Sh.12-222 Sh. No.12-221

TITLE: ENGINEERING PRODUCT SPECIFICATION
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- 3) OREV to set if $(G = 15) + (G = 3)$.
- 4) LAFF to reset.
- 5) GA to reset and GF to set if LSA enabled.
- 6) $\$$ enters the timing pulse generator delay line network to produce another $\$$ pulse.

GA will be repeated as many times as required to align the mantissa, and will terminate on the first $\$$ pulse following the enabling of LSA .

GF

During this cycle the complemented mantissa is added to the other mantissa in the S-adder producing the difference. This difference may cause an indicator to be set. If the mantissa in AQ is equal to the mantissa in Y and $\text{Y}+1$ the difference will be zero and ZERO will set. If the mantissa in AQ is greater than the mantissa in Y and $\text{Y}+1$ the difference will be positive and no indicators will set. If the mantissa in AQ is smaller than the mantissa in Y and $\text{Y}+1$ the difference will be negative and SIGN will set.

At the end of approximately 400 nanoseconds a $\$$ pulse will cause the following events:

- 1) SIGN to set if $(S_0) (\overline{\text{Overflow}}) + (\overline{S_0}) (\text{Overflow})$.
- 2) ZERO to set if $(S = 0)$.
- 3) K_{72} to reset.
- 4) GF to reset.

$\$$ will generate a $\$ \text{LAST}$, which is sent to the CU to indicate completion of the DFCMP instruction.

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Cont. on Sh.12-223 Sh. No.12-222

TITLE:

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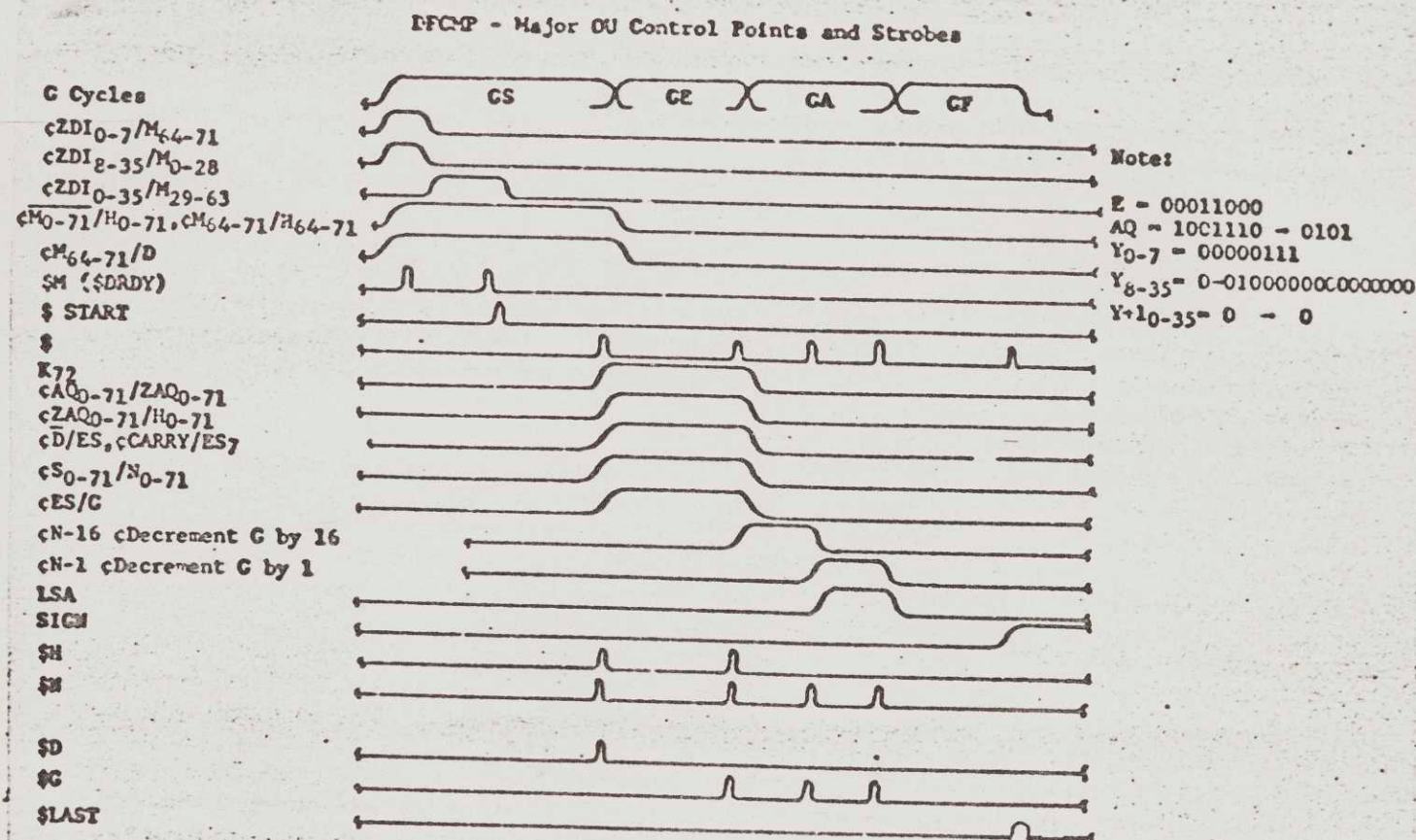


FIG. 12.3.8.2d DFCMP Instruction, Timing Diagram

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Cont. on Sh. 12-224 Sh. No. 12-223

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

DFCMP - Double Precision Floating Compare

All registers are shown before
the strobe at the end of the
cycle.

GS

$\overline{cM}_{0-71}/H_{0-71}$, cM_{64-71}/H_{64-71}

cM_{64-71}/D

c Set K_{72}

c Reset ZERO

c Reset SIGN

$\$H$, $\$N$, $\$D$

} Strobe
on $\$$

0 35 36 71
AQ 1001110 → 0 0 → 0101

0 35 36 71
N

0 35 36 71
S

0 35 36 71
H

0 21 35 36 64 71
M 0 → 010 → 0 0 → 000000111

980 7
E 0000011000

980 7
ES

0 7
D

0 7
G

GE

cAQ_{0-71}/ZAQ_{0-71}

$cZAQ_{0-71}/H_{0-71}$

$c\overline{D}/ES$ and $cCARRY/ES_7$

cS_{0-71}/N_{0-71}

cES/G

c Reset K_{72}

$\$H$, $\$N$, $\$G$

} Strobe
on $\$$

0 35 36 71
AQ 1001110 → 0 0 → 0101

0 35 36 71
N 0 → 0 0 → 0

0 21 35 36 71
S 1 → 10 → 0 0 → 0

0 21 35 36 71
H 1 → 101 → 1 1 → 1

980 7
E 0000011000

980 7
ES 0000010001

CARRY

0 7
D 00000111

0 7
G

FIG. 12.3.8.2e Register
Contents during GS, GE
Cycles of DFCMP Instruction

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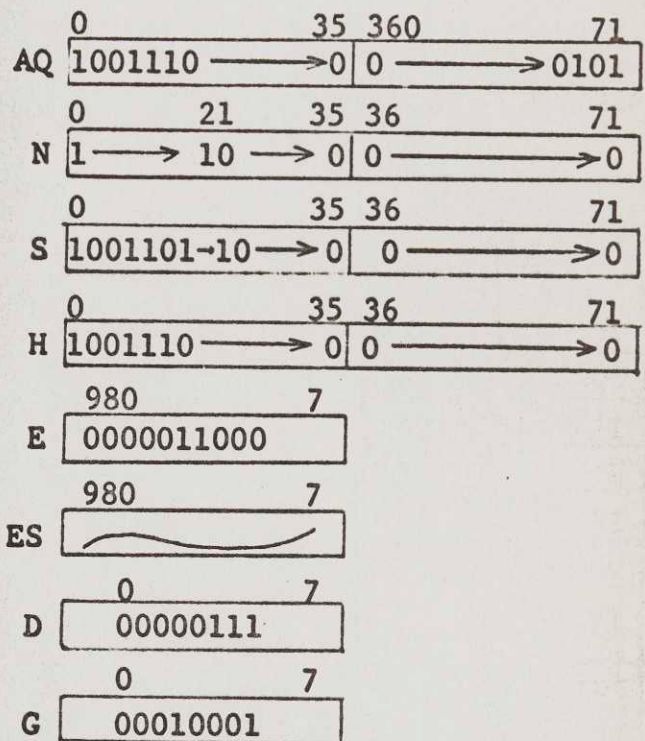
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Cont. on Sh.12-225 Sh. No.12-224

TITLE: ENGINEERING PRODUCT SPECIFICATION
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GA (first)
cN-16
c Decrement G by 16 } Strobe
\$N, \$G on \$



GA (second)

cN-1
LSA
c Decrement G by 1 } Strobe
\$N, \$G on \$

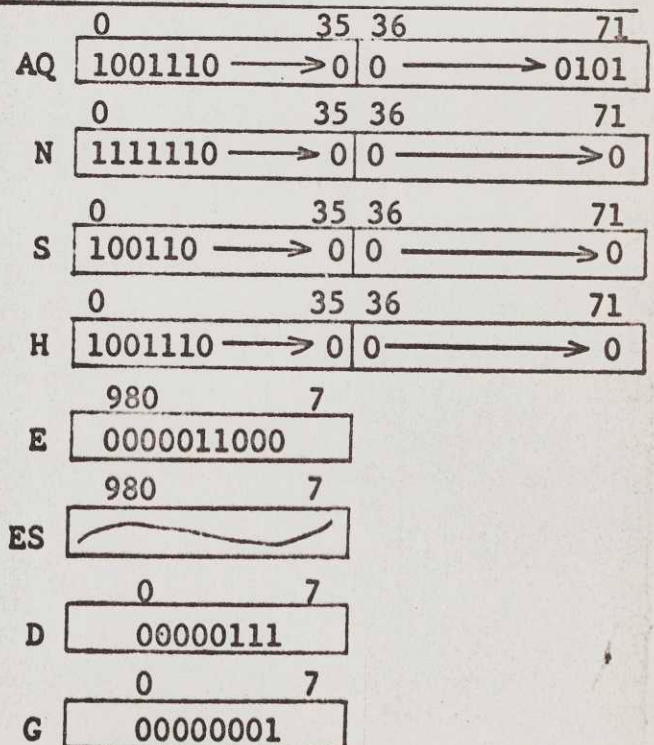


FIG. 12.3.8.2f Register
Contents during GA Cycle
of DFCMP Instruction

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 GE-645 PROTOTYPE PROCESSOR

GF

¢ SET SIGN - Strobe on \$

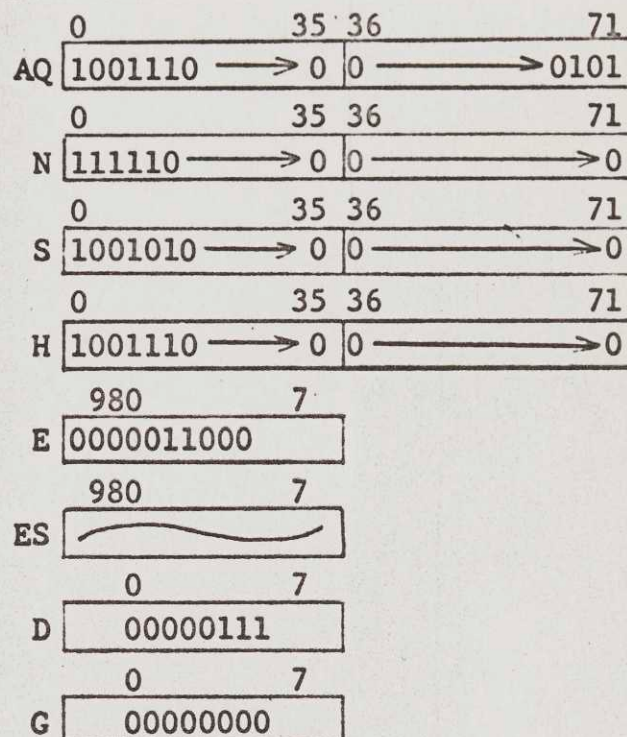


FIG. 12.3.8.2g Register Contents during GF Cycle of DFCMP Instruction

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TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR

12.3.9 Floating Point Store Group

This group consists of the three floating point store instructions FST, DFST, and STE. The major data paths and control points for these instructions are shown in Fig. 12.3.9.

To illustrate the control used in the execution of these instructions two instructions will be explained in detail. For the detailed control of all instructions in this group, refer to OU Specification Chart 43D140232, page 6.

In the explanation of all the example instructions, the following conditions will be assumed.

- 1) The instruction has been strobed into the O-register.
- 2) The GS and GC cycle flip-flops have been set.
- 3) The DDF flip-flop has been set indicating the operation decode has settled.

NOTE:

Reference to Fig. 12.3.9 will aid in the understanding of the instruction execution and implementation.

12.3.9.1 Single Precision

The instructions comprising the single precision portion of the Floating Point Store Group are FST and STE.

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Cont. on Sh.12-228 Sh. No.12-227

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

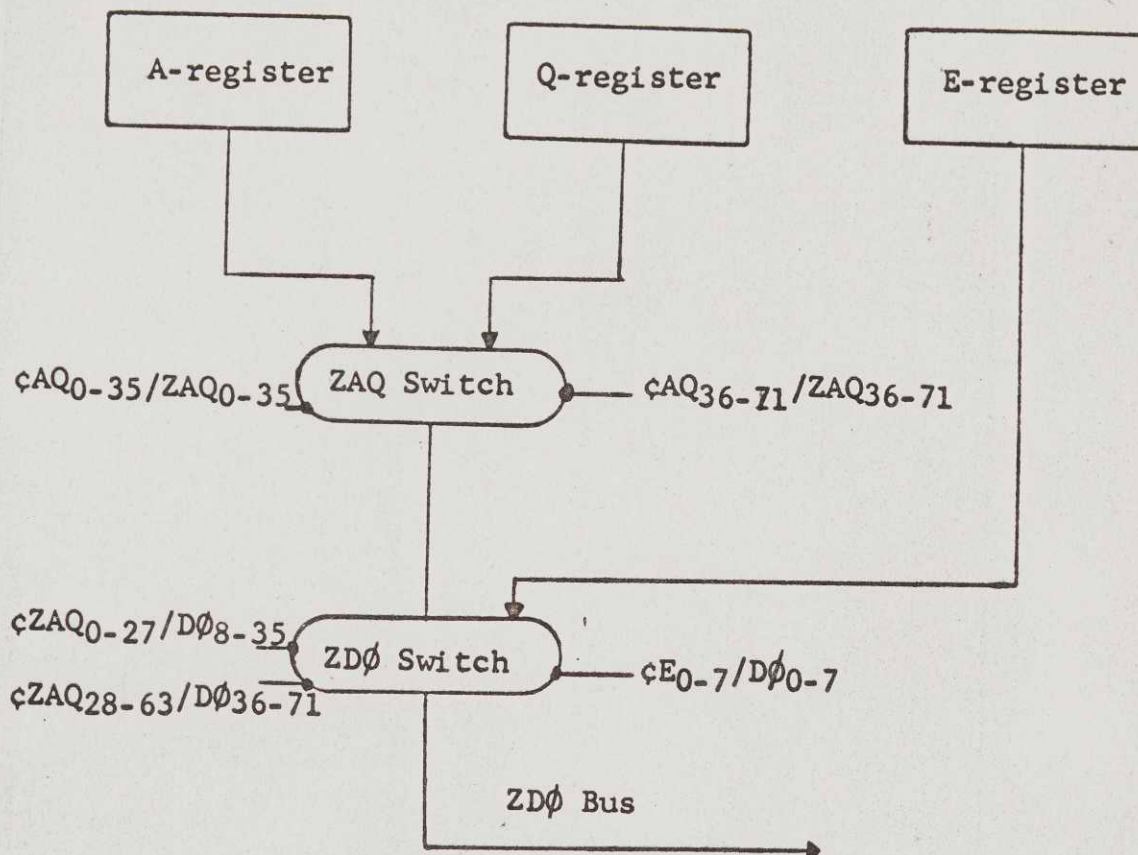


Fig. 12.3.9

Floating Point Store Group, Major Flowchart

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TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR

12.3.9.1 - contd

Example 1: Floating Store (FST)

During this instruction the contents of bits 0 through 7 of the E-register are transferred through the ZDO switch to bits 0 through 7 of a memory location Y and the contents of bits 0 through 27 of the A-register are transferred through the ZAQ and ZDO switches to bits 8 through 35 of the same memory locstion Y.

The ZAQ and ZDO switches are enabled by the presence of the FST decode together with the GS flip-flop set and the control point $\phi_{YS/ZDO}$ not enabled. The GC flip-flop will remain set from the beginning of the GS cycle to the end of the GF cycle. The ZAQ and ZDO switches are enabled by control points $\phi_{AQ0-35/ZAQ0-35}$, $\phi_{ZAQ0-27/ZDO8-35}$ and $\phi_{E0-7/ZDO0-7}$.

When the \$ Set GS pulse was generated for this instruction, it was delayed by about 40 nanoseconds to become \$YRY and it becomes \$SDY (store data ready). \$YRY sets the operand ready flip-flop, and is returned to the CU to signal that a new operation code may be sent to the OU. YRY set allows the \$ START pulse to be generated and enter the Timing Pulse Generator to later produce the first operate strobe \$. \$ START sets the OU busy flip-flop, OUB. \$SDY is sent to the CU to initiate the memory store cycle prior to the occurrence of the first \$ strobe in the OU.

When the \$ START pulse propagates the medium delay elements the first operate strobe \$ occurs. This causes the following events:

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Cont. on Sh.12-230 Sh. No.12-229

TITLE: ENGINEERING PRODUCT SPECIFICATION
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- 1) The GS cycle to reset and the GF cycle to set.
- 2) The O-register Busy flip-flop (ORB) to reset.
- 3) The \$ strobe re-enters the Timing Pulse Generator, but it is inhibited from exiting the delay line network.

The operand will be stored in the Data Out Buffer, in the Interface Frame, by \$INT. \$INT will also generate a \$DS and send it to the OU. \$DS is "OR3d" into the Timing Pulse Generator and exits on the general strobe (\$) lines. This pulse causes:

- 1) GF and GC to reset.
- 2) OUB to reset if no other instruction has been initiated.
- 3) It will generate a \$ LAST, which is sent to the CU to indicate completion of the FST instruction.

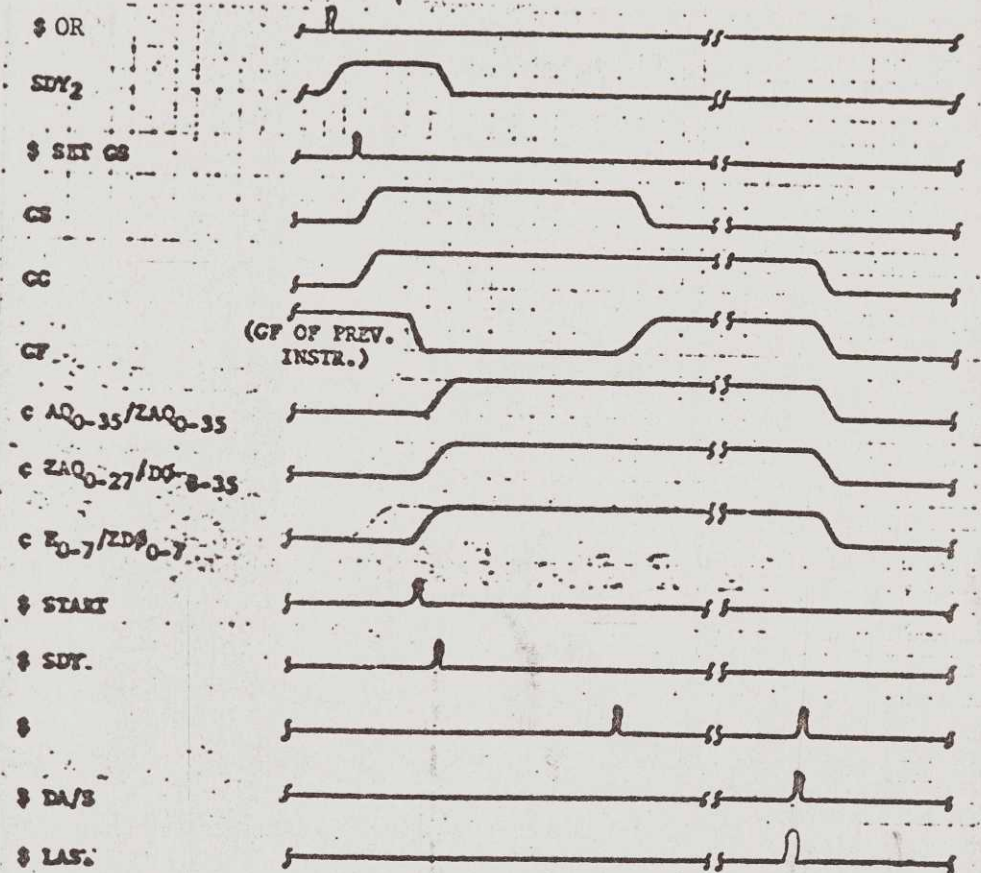
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Spec. No. M50EB00107

Cont. on Sh.12-231 Sh. No.12-230

TITLE: ENGINEERING PRODUCT SPECIFICATION
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FST - Major CPU Control Points and Strobes

FIG. 12.3.9.1 FST Instruction, Timing Diagram

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Cont. on Sh.12-232 Sh. No.12-231

TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR

12.3.9.2 Double Precision

The only instruction in the double precision portion of the Floating Point Store Group is DFST.

Example 1: Double Precision Floating Store (DFST)

During this instruction the contents of bits 0 through 7 of the E-register are transferred through the ZDO switch to bits 0 through 7 of a memory location Y and the contents of bits 0 through 63 of the AQ-register are transferred through the ZAQ and ZDO switches to bits 8 through 35 of Y and bits 0 through 35 of Y + 1.

GS

The ZAQ and ZDO switches are enabled by the presence of the DFST decode together with the GC flip-flop set and the control point $\phi_{YS/ZDO}$ not enabled. The GC flip-flop will remain set for two cycles. The ZAQ and ZDO switches are enabled by $\phi_{AQ0-71/ZAQ0-71}$, $\phi_{ZAQ0-27/ZDO8-35}$, and $\phi_{E0-7/ZDO0-7}$.

When the \$ Set GS pulse was generated for this instruction, it was delayed by about 40 nanoseconds to become \$YRY and it becomes \$SDY. \$YRY sets the operand ready flip-flop YRY, and is returned to the CU. YRY set allows the \$ START pulse to be generated and enter the OU Timing Pulse Generator to later produce the operate strobe \$. \$ START sets the OU busy flip-flop OUB.

\$SDY is sent to the CU to initiate the store cycle prior to the occurrence of the first \$ strobe in the OU.

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Cont. on Sh.12-233 Sh. No.12-232

TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR

GS

When the \$ START pulse propagates the medium delay elements the operate strobe \$ occurs. This causes the following events:

- 1) The GS cycle to reset and the GT cycle to set.
- 2) The O-register busy flip-flop ORB, to reset.
- 3) A level consisting of DP Stores and GT goes high.
- 4) The \$ strobe re-enters the Timing Pulse Generator, but since a store is being executed it is inhibited from exiting onto the general \$ lines.

GT

After a minimum time of 300 nanoseconds after \$SDY, the first half of the store operation will be complete and the first \$DS will be received from the Interface Frame to signal this fact. \$DS will produce a \$ strobe which will:

- 1) Reset the GC and GT cycle flip-flops.
- 2) Set the GF and GFT cycle flip-flops.
- 3) Cause the DP Stores and GT level to go low after about 60 nanoseconds but only after \$ strobe has "ANDed" with DPA to produce \$DP which is delayed by approximately 270 nanoseconds before being sent to the Interface Frame to signify that the second data word is ready to be stored.

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PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh.12-234 Sh. No.12-233

TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR

GF

During this cycle the last half of the double precision operand is stored in memory location $Y + 1$. The ZAQ and ZDO switches are enabled by $\phi\text{AQ}_{0-71}/\text{ZAQ}_{0-71}$ and $\phi\text{ZAQ}_{28-63}/\text{ZDO}_{0-35}$. This allows the second half of the operand to be present on the ZDO lines before the OU send the \$DP pulse to the Interface Frame for the second half store.

The \$DP strobes the data into the Data Out Buffer bits 36-71 and is returned as the second \$DS indicating the second half data has been received. This \$DS will generate a \$ Strobe pulse which will:

- 1) Rest the GF and GFT cycles.
 - 2) Reset the OUB flip-flop if no other instruction has been initiated.
 - 3) Generate \$ LAST, which is sent to the CU to indicate completion of the DFST instruction.
-

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Spec. No. M50EB00107

Cont. on Sh.12-235 Sh. No.12-234

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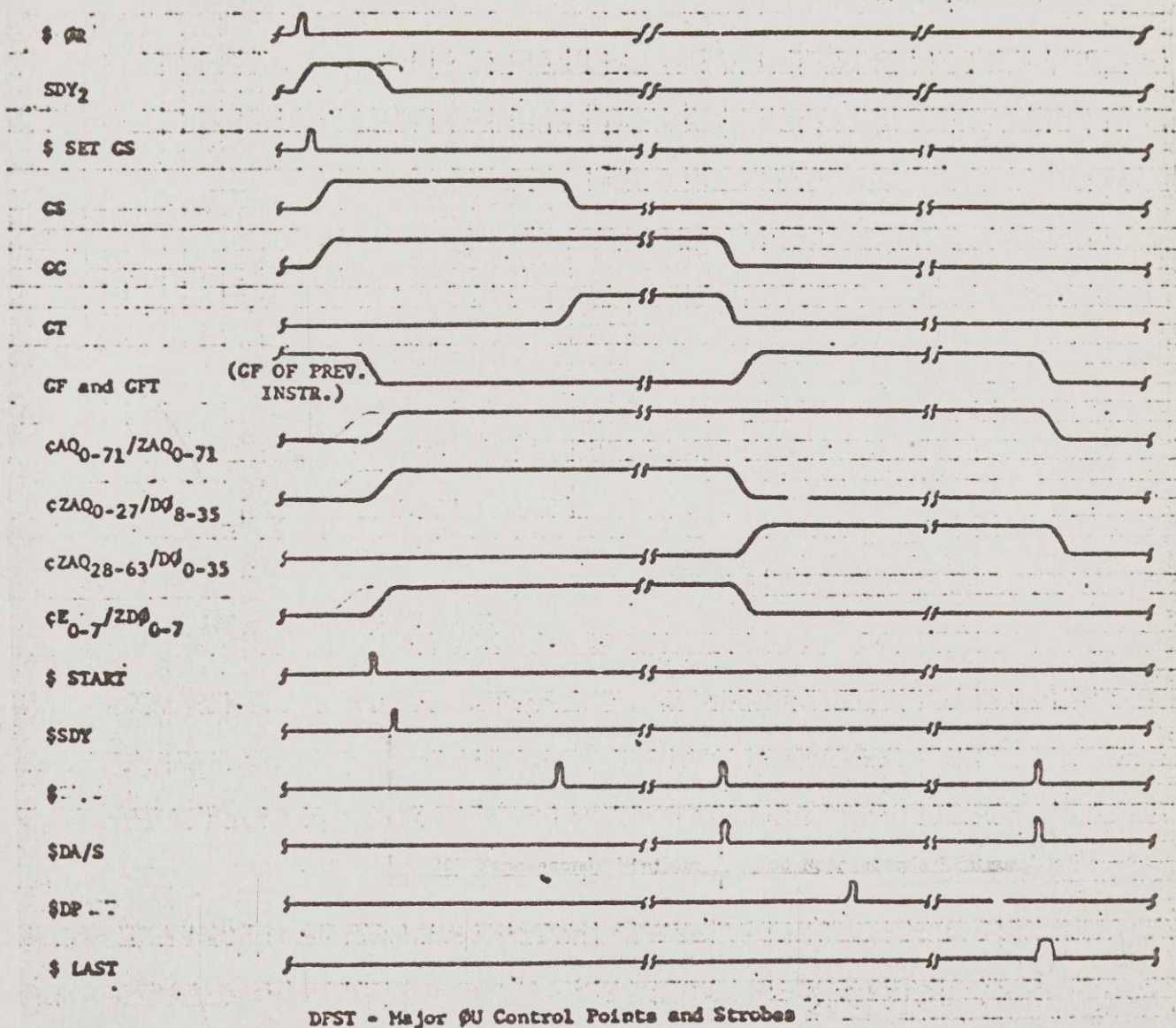


FIG. 12.3.9.2 DFST Instruction, Timing Diagram

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 GE-645 PROTOTYPE PROCESSOR

12.3.10 Floating Point Multiply Group

This group of four instructions provides the floating point multiply capabilities of this machine. The major data paths and control points for these instructions are shown in Fig. 12.3.10.

12.3.10.1 Single Precision

The instructions FMP and UFM provide single precision floating multiplication capability. For both instructions a 72-bit mantissa (multiplicand) is multiplied by a 28-bit mantissa (multiplier) to produce a 72-bit product. If a Direct Upper (DU) modifier is specified the multiplier mantissa consists of c(Y₈₋₁₇) followed by 8 zeros. If a Direct Lower (DL) modifier is specified the multiplier mantissa consists of 10 leading zeros followed by c(Y₁₈₋₃₅). The exponent for a DL multiplier is zero. In all cases the multiplier mantissa is contained in the M-register, right justified to bit 63, the multiplicand mantissa is contained in the AQ-register, the partial products are accumulated in the H-register, and the final mantissa product is stored in the AQ-register. The multiplier exponent is transferred from M₆₄₋₇₁ to D, the multiplicand exponent is contained in E, and the exponent sum is stored in E.

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PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh. 12-237 Sh. No. 12-236

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

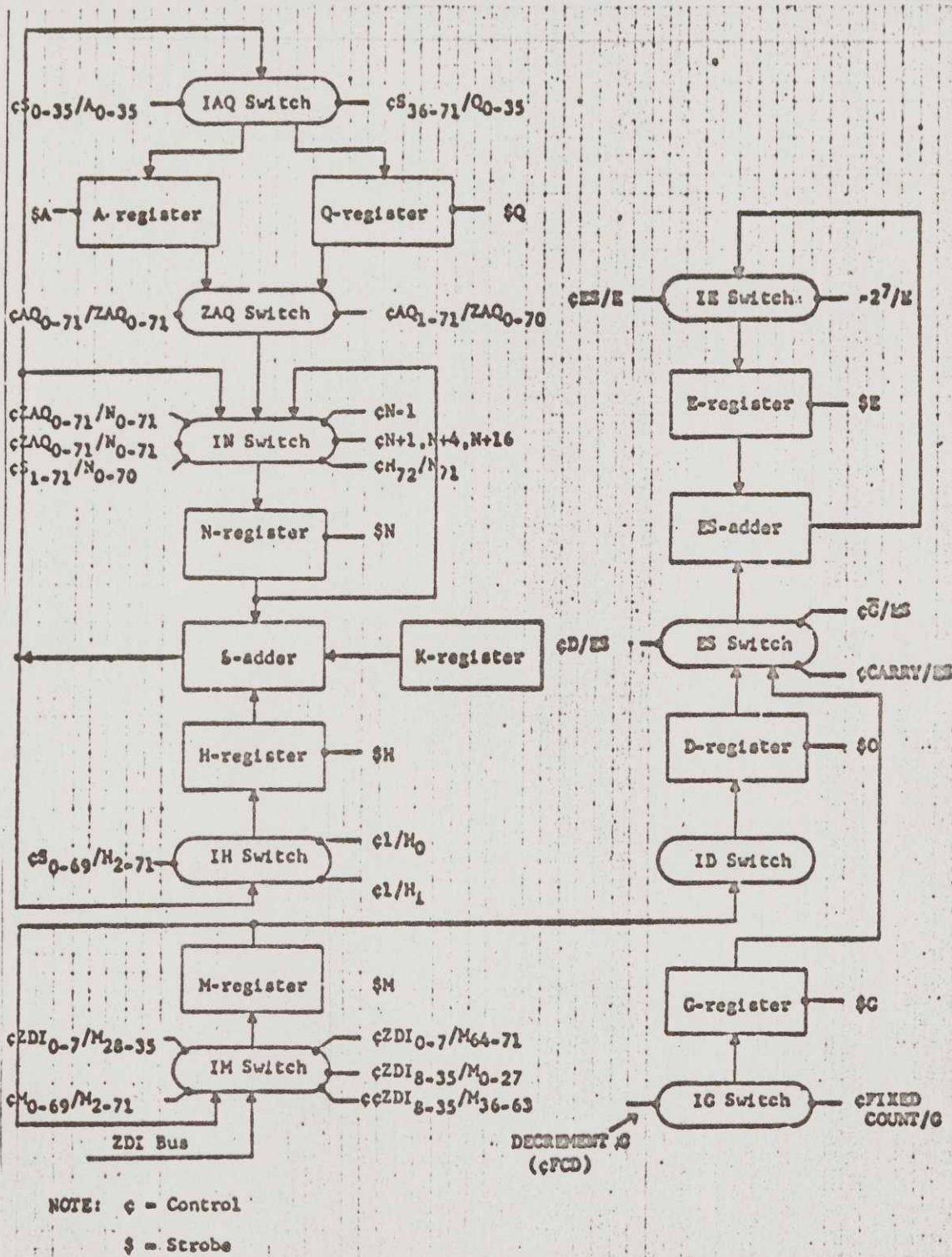


Fig. 12.3.10

Floating Point Divide Group, Major Flowchart

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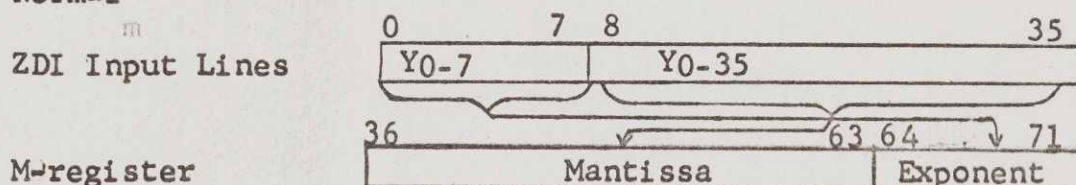
Cont. on Sh.12-238 Sh. No.12-237

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

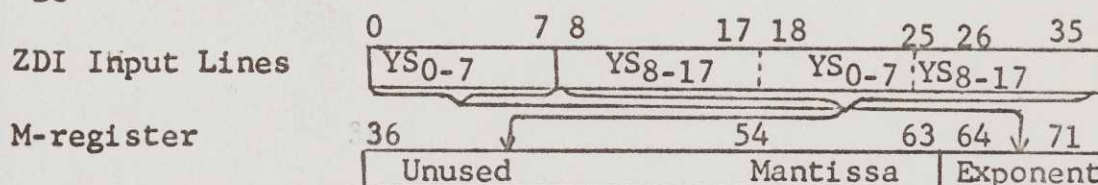
12.3.10.1 - contd

The possible multiplier configurations which may be contained in the M-register with respect to the ZDI lines from the CU are shown below:

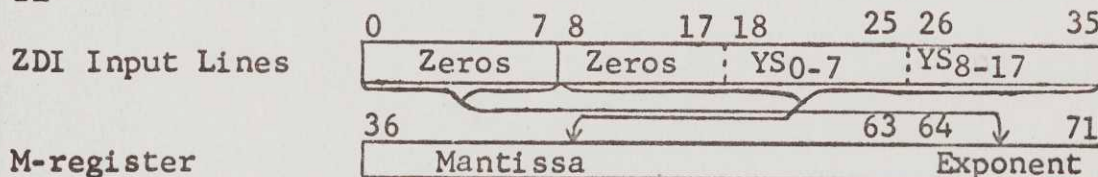
1) Normal



2) DU



3) DL



YS₀₋₁₇ is the Address Register output through the YS-adder.

The only difference between a FMP and an UFM instruction is in the handling of the mantissa product. During a FMP the mantissa product is always normalized, while during an UFM the mantissa product is normalized only if an overflow occurred.

For the detailed control of these two instructions refer to the OU Specification Chart 43D140232, page 8.

NOTE: Reference to Fig. 12.3.10 will aid in the understanding of the instruction execution and implementation.

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Spec. No. M50EB00107

Cont. on Sh.12-239 Sh. No.12-238

TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR

12.3.10.1- contd

Example 1: Floating Multiply Normalized (FMP)

During this instruction the contents of the AQ-register are multiplied by the contents of memory location Y₈₋₃₅ to produce a 72-bit (including sign) product which is stored in the AQ-register, and the contents of the E-register are added to the contents of memory location Y₀₋₇ to produce an 8-bit sum which is stored in the E-register. For this example no operands are used, but all major controls are explained.

The IM-switch is enabled by the presence of the FMP decode together with DIC and DPFF reset. The control points ϕ ZDI₀₋₇/M₆₄₋₇₁, and ϕ ZDI₈₋₃₅/M₃₆₋₆₃ are enabled to allow the ZDI bus to be present at the M-register inputs. When the operand ready strobe \$DRDY is received from the CU, DPFF reset allows the M-register strobe \$M₀₋₇₁ to be generated and strobe the multiplier into the M-register. See page 12.232 for the possible arrangements of the multiplier. If the multiplier operand being furnished by the CU is a Direct Upper, a \$DMF will be received at the same time as \$DRDY. \$DMF will set DUM. The \$DRDY pulse is turned around as \$YRY and returned to the CU to signal that a new instruction may be prepared. \$YRY also sets YRY, and because of the FMP decode sets DIC. The DIC flip-flop is used as an inhibit on the ZDI/M controls for the duration in which the multiplier is contained in M. When YRY is set, the conditions exist to allow a \$ START to be generated by a last of three pulse detector. \$ START sets the OU Busy flip-flop (OUB), resets YRY and DDF, and transfers the operation code from the O-register to the C-register. It also enters the timing pulse generator delay line network.

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Spec. No. M50EB00107

Cont. on Sh.12-240 Sh. No.12-239

TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR

12.3.10.1 contd

GS

During the 320 nanoseconds of GS from \$ START to the first \$, control is established to load the G-counter with the proper count with the first \$. If DUM is set (which defines the multiplier is a Direct Upper) Fixed Count/G control will force a count of 6 into G* (that is, set G₅ and G₆). If DUM is reset, a count of 15 is placed in G (that is, set G₄, G₅, G₆, and G₇). Also the control line $\phi M_{64-71}/D$ becomes enabled to transfer the exponent to the D-register.

As per the multiply algorithm, the low-order two bits of the multiplier M₆₂₋₆₃ are decoded during this same 320 nanoseconds of GS to indicate whether the first multiplication will be by 0, 1, 2, or 3. The decode of M₆₂₋₆₃ is interpreted as:

- 1) If M₆₂₋₆₃ = 00, this represents multiplication by zero or a pass condition (that is, no modification of the partial product in H which at this time is zero). No ZAQ or IN switch is enabled.
- 2) If M₆₂₋₆₃ = 01, this represents multiplication of the multiplicand by one. Since at this time there is no partial product. To accomplish this the ZAQ and IN switches are enabled by $\phi AQ_{0-71}/ZAQ_{0-71}$ and $\phi ZAQ_{0-71}/N_{0-71}$. These enabled switches allow the A-register multiplicand to be present at the N-register inputs.

*Refer to paragraph 12.4 for a description of the G-counter when used as a decrement counter.

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Spec. No. M50EB00107

Cont. on Sh.12-241 Sh. No.12-240

TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR

12.3.10.1-contd

- 3) If $M_{62-63} = 10$, this represents multiplication of the multiplicand by two. For a binary number this may be done by shifting the number left by one bit position. To accomplish this the ZAQ and IN switches are enabled by $\phi AQ_{1-71}/ZAQ_{0-70}$ and $\phi ZAQ_{0-71}/N_{0-71}$.
- 4) If $M_{62-63} = 11$, this represents multiplication of the multiplicand by three. This is accomplished by doing a multiply of $(4-1 = 3)$. The multiply by 4 is accomplished by adding one to the bit which will be contained in M_{63} during the next multiply cycle. Effectively this means that the bits presently contained in M_{60-61} are to be incremented by one. The minus one control is set up during the present multiply cycle and is performed by subtracting the contents of A from the partial product. The IAQ and IN switches are enabled by $\phi AQ_{0-71}/ZAQ_{0-71}$, $\phi \overline{ZAQ}_{0-71}/N_{0-71}$. These switches present the one's complement of the AQ-register to N_{0-71} .

Because a new set of multiplier bits will be needed for the next multiply cycle (the first GO cycle), the control is set up to allow a right shift of the M-register by two. The IM switch is enabled by $\phi M_{0-33}/M_{2-35}$ and $\phi M_{34-69}/M_{36-71}$ to accomplish this right shift.

When the \$ START pulse propagates the medium delay elements, the first operate strobe \$ occurs. This allows the following events:

- 1) The GS cycle to reset and the GO cycle to set.
- 2) The ZERO and SIGN Indicators to reset.

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Spec. No. M50EB00107

Cont. on Sh. 12-242 Sh. No. 12-241

TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR

12.3.10.1-contd

- 3) \$G is generated which strobes the count of 6 or 15 into the G-counter depending on the control lines enabled.
- 4) \$M is generated which strobes the M-register and executes a right shift of two to set up a new set of multiplier bits.
- 5) \$H is generated which strobes the H-register, but since no IH switch is enabled at this time all zeros are loaded into H.
- 6) \$N is generated which strobes the N-register and sets up the data to produce the first partial product in the adder. The data loaded into N depends on which controls were enabled from A into N as a function of the first set of M₆₂₋₆₃ bits.
- 7) The K₇₂ adder control flip-flop and String flip-flop (STFF) are set if the first M₆₂₋₆₃ set were 112 which called for a multiplier of 3.
- 8) The PASS flip-flop is set if the first M₆₂₋₆₃ set were 002.
- 9) The Partial Product Sign flip-flop (PPS) has the contents of A₀ strobed into it if a multiplier of 1 or 2 was called for, has A₀ strobed in if the multiplier were 3, or is left unchanged if the multiplier was zero.
- 10) A \$D is generated that strobes the exponent from M₆₄₋₇₁ into D.

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Spec. No. M50EB00107

Cont. on Sh.12-243 Sh. No.12-242

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

11) \$ enters the timing pulse generator delay line network to produce another \$ pulse.

(G0) (G > 3)

During this 320-nanosecond time the first G0 cycle is true and the S-adder is used to produce the first partial product and make it available on the S bus at the adder output. While this partial product is being developed, the control points are established to store the partial product on the S bus into H and set up the control to perform the next 2-bit multiplication.

During the G0 cycles the determination of what the next effective multiplier will be is not only a function of M62-63 as it was in GS, but it is also dependent on the state of the String flip-flop (STFF). Although there are still only four possibilities for a multiplier, there are now two conditions that cause each possibility. These are shown below in truth table form:

M62	M63	STFF	Effective Multiplier
0	0	0	00
0	1	0	+1
1	0	0	+2
1	1	0	3 (or -1)
0	0	1	+1
0	1	1	+2
1	0	1	3 (or -1)
1	1	1	0

The control points enabled as a function of the effective multiplier are the same as the ones mentioned during GS when the multiplier was 0, 1, 2, or 3.

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Spec. No. M50EB00107

Cont. on Sh.12-244 Sh. No.12-243

TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR

The IH switch is enabled during GO to allow the partial product to be strobed into H. The control points enabled for this during GO are $\phi S_{0-33}/H_{2-35}$ and $\phi S_{34-59}/H_{36-71}$.

During this GO cycle the controls on the IM switch are again enabled to allow the M-register to be right shifted by two in order to have a new set of multiplier bits for the next cycle. The Full Counter Decrement control (ϕFCD) becomes enabled so that the next \$G will decrement the count by one.

When the first \$ strobe propagates the medium delay elements, the second \$ is distributed to the OU to end the first GO cycle and the following events occur:

- 1) The GO flip-flop is strobed, but because the G count is not zero it remains set.
- 2) \$G decrements the G-counter by one.
- 3) \$M strobes the M-register and executes a right shift of two to set up a new set of multiplier bits.
- 4) \$H strobes the partial product into H_{2-71} . The content of the Partial Product Sign flip-flop (PPS) is strobed into H_0 unconditionally and into H_1 if no overflow occurred.
- 5) \$N strobes the new premultiplied multiplicand in the N-register as determined by the multiplier decode.
- 6) The K_{72} adder control flip-flop and the String flip-flop (STFF) are set if the effective multiplier is 3. STFF is reset if the effective multiplier is +1, +2, or +2 and not changed if it is zero. K_{72} is reset for values of other than 3.

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Spec. No. M50EB00107

Cont. on Sh.12-245 Sh. No.12-244

TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR

- 7) The PASS flip-flop is set for an effective multiplier of zero, or reset for 1, 2, or 3.
- 8) The PPS flip-flop is strobed and sets or resets for the same conditions listed in GS.
- 9) \$ enters the Timing Pulse Generator delay line network to produce another \$ pulse.

Up until the time when the G-counter is decremented to a count of 3 the functions performed during all of the GO cycles are iterative of the first GO cycle.

GO (G = 3)

During the GO cycle when $G = 3$ the next to last partial product is formed in the S-adder, and the last multiplicand is prepared for addition to the partial product during $G = 2$ time. The conditions to enable control points during $G = 3$ are the same as those used for $G > 3$ with these exceptions:

- 1) For the decode of $M_{62-63} = 102$ and $STFF = 0$ (multiplier = ± 2), two times the multiplicand is prepared for subtraction from the partial product during $G = 2$. This necessitates that $\phi ZAQ_{36-71}/N_{36-71}$ be enabled and the control to set K_{72} must be enabled.
- 2) When $G = 3$, a level resets the DIC flip-flop and frees the M-register.
- 3) The control on the set/reset of PPS is not a function of the (± 2) multiplier.
- 4) $STFF$ is unconditionally reset.

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Spec. No. M50EB00107

Cont. on Sh. 12-246 Sh. No. 12-245

TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR

When the \$ pulse is generated at the end of $G = 3$, the same strobes occur as for $G > 3$ with the exception of \$M. \$M is not produced because the multiplier in M has been exhausted by this time. This strobe decrements the G count to 2 and the multiply continues.

GO ($G = 2$)

During $G = 2$ the final partial product is formed in the S-adder as a function of the former partial product in H and the multiplier controlled multiplicand in N. Because this will be the last add cycle, no control points are enabled to load a new multiplicand into N on the strobe at the end of $G = 2$. The control line $\phi S_{0-69}/H_{2-71}$ will be enabled to transfer the final partial product to H. At the same time the length of the partial product will be increased by one bit by transferring the contents of S_{70} to H_{72} .

When the \$ pulse is generated at the end of $G = 2$, the same strobes are produced that occurred at the end of $G = 3$. Because no switches are enabled into N, this register is cleared to all zeros. The K_{72} flip-flop is unconditionally reset and the G count is decremented to one.

GO ($G = 1$)

During $G = 1$ the final mantissa product is contained in H_{1-72} with the binary point to the right of H_1 . Control is set up to transfer H_{1-72} N_{0-71} and thereby place the binary point to the right of N_0 . The control points enabled to accomplish this are $\phi S_{1-71}/N_{0-70}$ and $\phi H_{72}/N_{71}$. At the same time controls are set up to add the two exponents. $\phi D_{0-7}/ES_{0-9}$ and $\phi ES_{0-9}/E_{0-9}$ are enabled to accomplish this.

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Spec. No. M50EB00107

Cont. on Sh. 12-247 Sh. No. 12-246

TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR

When the \$ pulse is generated at the end of $G = 1$,
the following events occur:

- 1) \$N transfers the product with a left shift of one from H via the S-adder to N.
- 2) \$G decrements the G count to zero.
- 3) \$H clears H to zero.
- 4) \$E strobes the sum of the exponents into E.
- 5) SIGN is set if $S_0=1$.
- 6) ZERO is set if the S-adder output = 0.
- 7) REV is set if $(S_0\bar{S}_1 + \bar{S}_0S_1)$.
- 8) GN is set if $(OFL) + (S \neq 0)(S_0 = S_1)$.
- 9) GF is set if $(\overline{OFL})(S = 0) + S_0 = S_1$.
- 10) GO is reset.
- 11) \$ enters the timing pulse generator delay line network to produce another \$ pulse.

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Spec. No. M50EB00107

Cont. on Sh.12-248 Sh. No.12-247

TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR

GN

During this cycle the mantissa in N is normalized. If an overflow occurred during the last G0 cycle the mantissa is shifted one place right with opposite sign inserted and the G-counter is decremented to (-1). In all other cases the mantissa is shifted left until No and N are not alike and the G-counter is incremented by one for each place the mantissa is shifted. The control lines that become enabled to accomplish this are:

- 1) $\phi N - 1$ ($\phi N_{0-70}/N_{1-71}$) if REV set.
- 2) $\phi N + 16$ ($\phi N_{16-71}/N_{0-55}$) if N_0 through N_{15} are all the same.
- 3) $\phi N + 4$ ($\phi N_{4-71}/N_{0-67}$) if $\overline{\phi N + 16}$ and N_0 through N_3 are all the same.
- 4) $\phi N + 1$ ($\phi N_{1-71}/N_{0-70}$) if $(\overline{\phi N + 16})(\overline{\phi N + 4})$ and $N_0 = N_1$.
- 5) LSN enabled if $(\phi N + 16)(N_{15} = N_{16} \neq N_{17})$
+ $(\phi N + 4)(N_3 = N_4 \neq N_5)$ + $(\phi N + 1)(N_0 = N_1 \neq N_2)$
+ (REV).

At the end of 230 nanoseconds a \$ pulse will cause the following events:

- 1) \$N strobes the shifted contents of N back into N.
- 2) \$G to increment the G-counter by 16 if $\phi N + 16$, by 4 if $\phi N + 4$, by 1 if $\phi N + 1$, and decrement G by 1 if REV.
- 3) REV to set if $(\phi N + 16)(N_{15} \neq 16) + (\phi N + 4)(N_3 \neq N_4)$.
- 4) REV to reset if REV is set.

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Spec. No. M50EB00107

Cont. on Sh.12-249 Sh. No.12-248

TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR

12.3.10.1-contd

- 5) GN to reset and GF to set if LSN enabled.
- 6) \$ enters the timing pulse generator delay line network to produce another \$ pulse.

GN will be repeated as many times as required to normalize the mantissa and will terminate on the first \$ pulse following the enabling of LSN.

GF

During this cycle the mantissa in N is transferred to AQ, and the count in G is subtracted from E, with the resultant exponent stored in E. The control lines that become enabled to accomplish this are:

- 1) $\phi S_{0-71}/AQ_{0-71}$.
- 2) $\overline{\phi G_{0-7}}/ES_{0-7}$ and $\phi CARRY/ES_7$.
- 3) $\phi ES/E$ if mantissa $\neq 0$.
- 4) $\phi -2^7/E$ if mantissa = 0.

At the end of 400 nanoseconds a \$ pulse will cause the following events:

- 1) \$AQ will strobe the mantissa product into AQ.
- 2) \$E will strobe the exponent into E.
- 3) EOFL will set if the subtraction of G from E caused the exponent to exceed +127.
- 4) EUFL will set if the subtraction of G from E caused the exponent to become smaller than -128.

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Spec. No. M50EB00107

Cont. on Sh.12-250 Sh. No.12-249

TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR

- 5) GF will reset.
- 6) \$ will generate a \$.LAST, which is sent to the
CU to indicate completion of the FMP instruction.

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Spec. No. M50EB00107

Cont. on Sh.12-251 Sh. No. 12-250

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

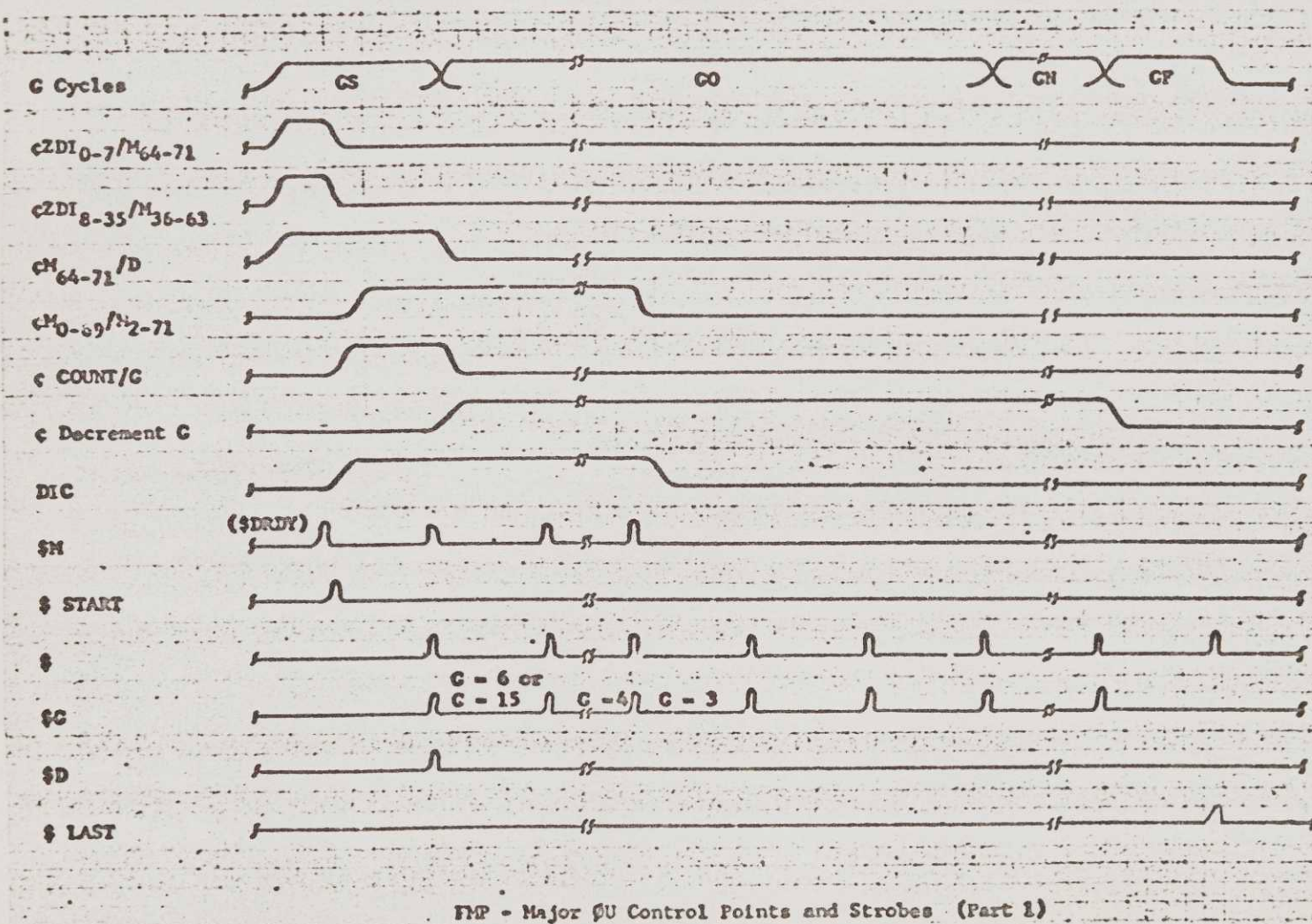


FIG. 12.3.10.1 FMP Instruction, Timing Diagram
(Sheet 1 of 2)

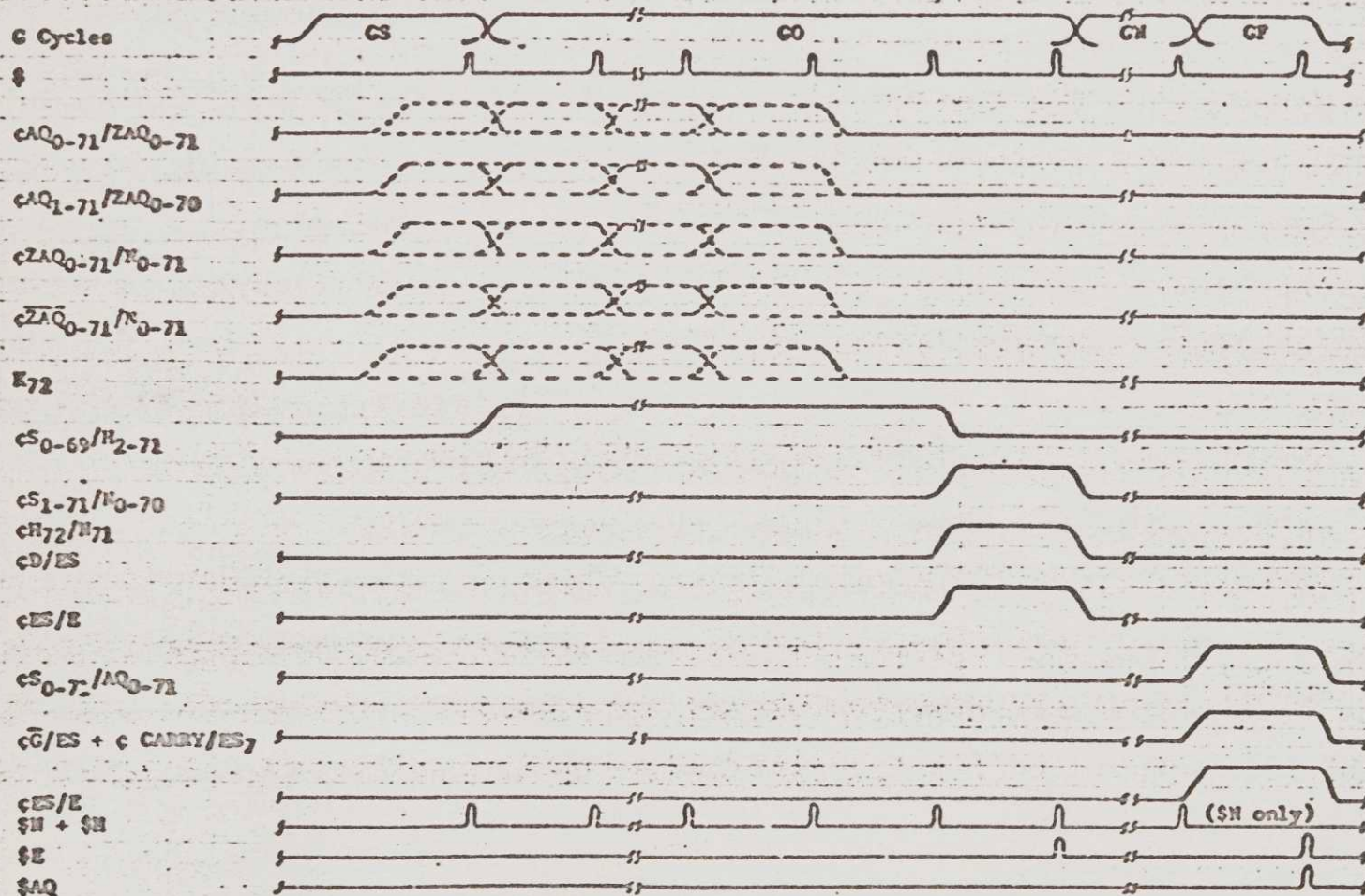
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Spec. No. M50EB00107

Cont. on Sh.12-252 Sh. No.12-251

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR



FMP - Major CPU Control Points and Strobes (Part 2)

FIG. 12.3.10.1 FMP Instruction, Timing Diagram
(Sheet 2 of 2)

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Spec. No. M50EB00107

Cont. on Sh. 12-253 Sh. No. 12-252

TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR

12.3.10.2 Double Precision

The instructions DFMP and DUFM allow double precision floating multiplication to be accomplished. For both instructions a 72-bit mantissa (multiplier) is multiplied by a 64-bit mantissa (multiplier) to produce a 72-bit mantissa (product). At the same time the two 8-bit exponents are added to produce 8-bit product exponent. The multiplier mantissa is contained in M_{0-63} , the partial products are accumulated in H_{0-72} , and the final mantissa product is stored in AQ_{0-71} . The multiplier exponent contained in M_{64-71} is transferred to D, the multiplier exponent is contained in E, and the exponent sum is stored in E.

The only difference between a DFMP and a DUFM instruction is in the handling of the mantissa product. During a DFMP the mantissa product is always normalized, while during a DUFM the mantissa product is normalized only if an overflow occurred.

For detailed control of these two instructions refer to the OU Specification Chart 43D140232 page 8.

The DFMP is identical to the FMP, as is the DUFM and UFM, except during GS. Only the GS cycle will be discussed here. Refer to 12.3.10.1 for all other cycles.

GS

The IM-switch is enabled by the presence of the DFMP or DUFM decode together with DPFF, and DIC reset. The control points $\phi ZDI_{0-7}/M_{64-71}$ and $\phi ZDI_{8-35}/M_{0-27}$ are enabled to allow the ZDI bus to be present at the proper M-register inputs.

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GENERAL ELECTRIC COMPANY
COMPUTER EQUIPMENT DEPARTMENT
PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh.12-254 Sh. No.12-253

TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR

12.3.10.2-contd

When the first \$DRDY is received from the CU, DPFF reset allows \$M₀₋₇₁ to be generated and strobe the exponent and most significant 28 bits of the mantissa into M. This \$DRDY will set DPFF, but will not generate a \$YRY. On the setting of DPFF, the IM-switch will be unabled by ϕ ZDI_{0-7/M28-35} and ϕ ZDI_{8-25/M36-63}.

About 250 nanoseconds after the first \$DRDY another \$DRDY will be received. DPFF set will allow \$M₂₈₋₆₃ to be generated and strobe the least significant 36 bits of the mantissa into the M-register. This \$DRDY resets DPFF and is turned around as \$YRY and returned to the CU to signal that a new instruction may be prepared. \$YRY also sets YRY, and because of the DFMP or DUFM decode sets DIC. The DIC flip-flop is used as an inhibit on the ZDI/M controls for the duration in which the multiplier is contained in M. When YRY is set the conditions exist to allow a \$ START to be generated by a last of three pulse detector. \$ START sets OUB, resets YRY and DDF, and transfers the operation code from the O-register to the C-register. It also enters the timing pulse generator delay line network.

During the 300 nanoseconds of GS from \$ START to the first \$, control is established to load the G-counter with a count of 33 on the first \$. ϕ M_{64-71/D} becomes enabled to transfer the exponent to D.

Everything from this point on is the same as for FMP instruction.

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GENERAL ELECTRIC COMPANY
COMPUTER EQUIPMENT DEPARTMENT
PHOENIX, ARIZONA

Spec. No.M50EB00107

Cont. on Sh.12-255 Sh. No.12-254

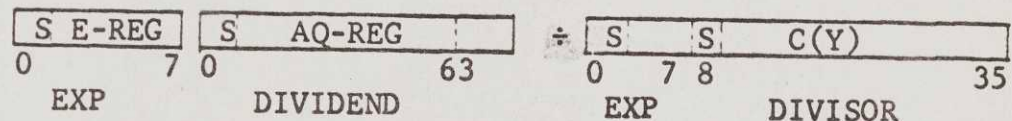
TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

12.3.11 FLOATING POINT DIVIDE GROUP

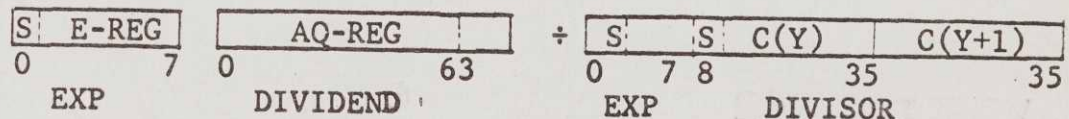
This group of four instructions comprise the floating point divide capabilities of this machine. The major control points and data paths can be seen in figure 12.3.11.

The instructions FDV, FDI, DFDV, and DFDI give the capabilities of dividing by 28-bit (single precision) and 64-bit (double precision) mantissas, including sign. In each case there are eight bits of sexponent including sign.

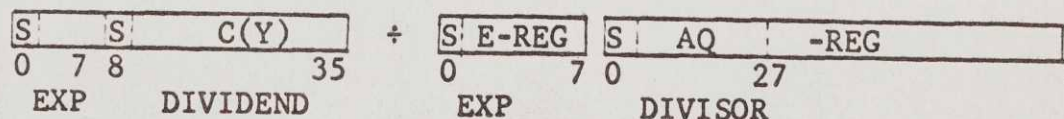
FDV



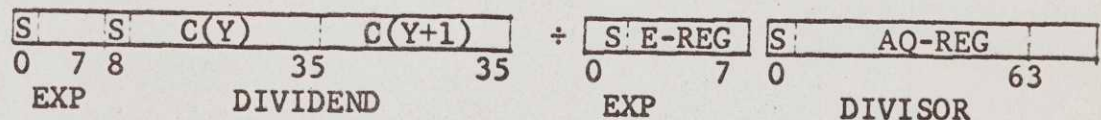
DFDV



FDI



DFDI



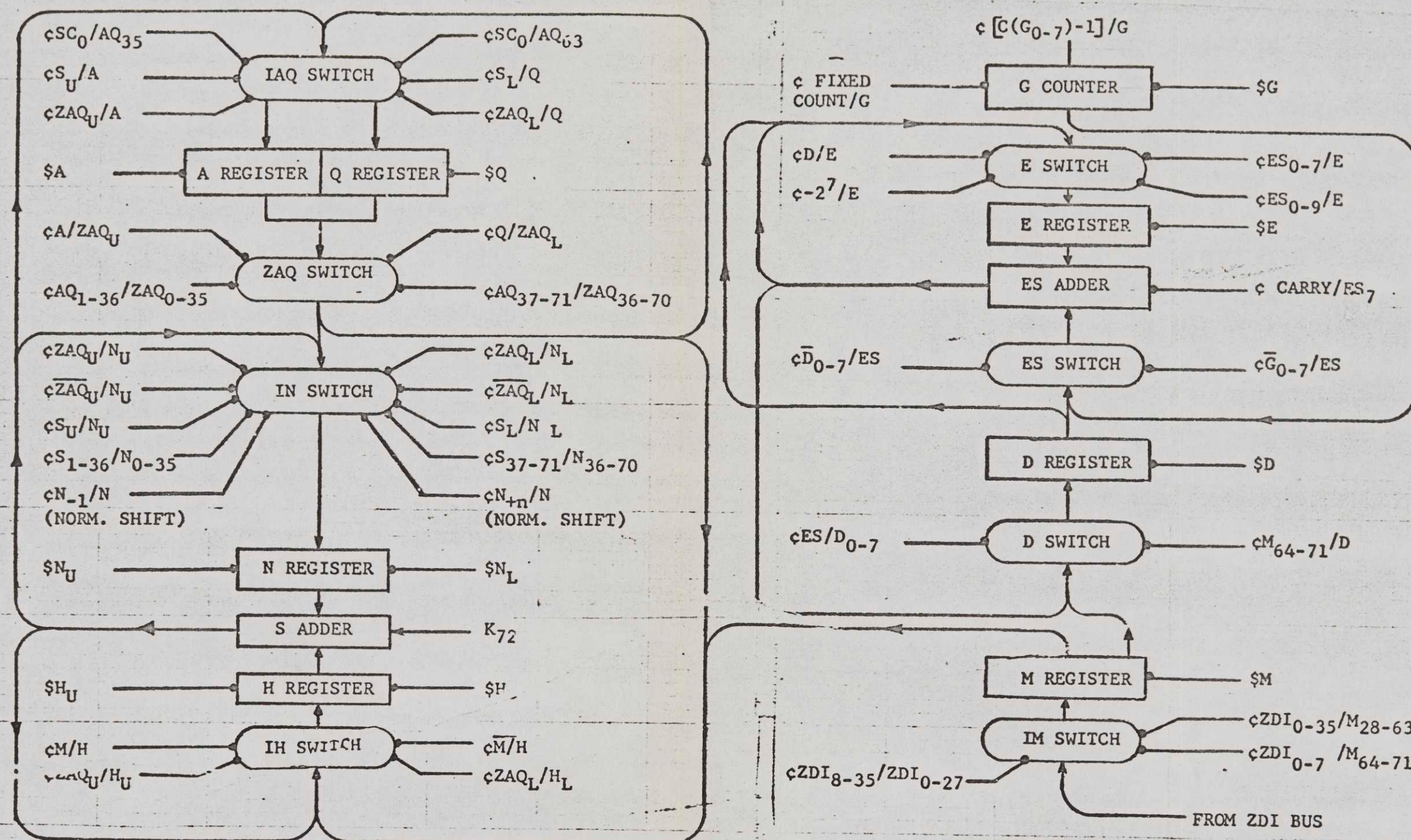


FIG. 12.3.11 FLOATING DIVIDE GROUP REGISTERS AND DATA FLOW

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Spec. No. M50EB00107

Cont. on Sh.12-257 Sh. No.12-256

TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR

12.3.11.1 Single Precision

FDV

During the instruction FDV, a 63 bit fractional dividend mantissa plus sign in the AQ-register and exponent in the E-register are divided by a 27 bit fractional divisor mantissa plus sign and exponent from a memory location Y, to produce a 35 bit fractional quotient mantissa plus sign in the A-register and an exponent in the E-register. The Q-register is cleared to zero.

The load path for the divisor into the M-register places the mantissa and sign from ZDI₈₋₃₅ into M₀₋₂₇ and the exponent from ZDI₀₋₇ into M₆₄₋₇₁. The generation of \$ SET GS and \$ START are as developed in paragraph 12.2.

GS

During GS, the ZAQ and IN switches are enabled to convert the C(AQ) to a positive dividend. The inputs to the N-register are strobed with the signal \$N₀₋₃₅ and \$N₃₆₋₇₁. The control points $\overline{c}AQ_{0-35}/ZAQ_{0-35}$ and $\overline{c}AQ_{36-71}/ZAQ_{36-71}$ are activated, and if the sign of the dividend mantissa in AQ is already positive ($A_0=0$), the control points activated are $\overline{c}ZAQ_{0-35}/N_{0-35}$ and $\overline{c}ZAQ_{36-71}/N_{36-71}$ and $\overline{c}$ reset K_{72} . If the sign of the dividend mantissa is negative ($A_0=1$), the control points $\overline{c}ZAQ_{0-35}/N_{0-35}$, $\overline{c}ZAQ_{36-71}/N_{36-71}$ and set K_{72} are activated to complement AQ and thus convert the dividend to positive. At the same time $\overline{c}M_{64-71}/D_{0-7}$ is enabled, to place the divisor exponent in the D-register.

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GENERAL ELECTRIC COMPANY
COMPUTER EQUIPMENT DEPARTMENT
PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh.12-258 Sh. No.12-257

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

12.3.11.1 - contd

When the \$ START pulse propagates the medium delay elements, the first operate strobe \$ occurs. This allows the following events:

- 1) The GS cycle to reset and the GD1 cycle to set.
- 2) The quotient sign flip-flop (QSF) and Zero indicator to reset.
- 3) \$N strobes either ZAQ or $\overline{\text{ZAQ}}$ into the N-register.
- 4) \$ H is generated, but since no IH switch is enabled, all zeros are loaded into H.
- 5) \$ D strobes the dividend exponent into the D-register.
- 6) The K₇₂ adder control flip-flop is set if it is necessary to complement the C(AQ) to produce a positive dividend.
- 7) The \$ strobe re-enters the Timing Pulse generator delay line network to produce another \$ strobe in about 400 nanoseconds.

GD1

During GD1 the positive dividend will become available at the adder output. The IAQ switch is enabled and the AQ-register is strobed with the positive dividend.

The IAQ switch is enabled by $\phi S_{0-35}/AQ_{0-35}$ and S_{36-71}/AQ_{36-71} . The IH switch is enabled by $\phi M_{0-35}/H_{0-35}$ and $\phi M_{36-63}/H_{36-63}$ if $M_0=1$, or by $\phi \overline{M}_{0-35}/H_{0-35}$ and $\phi \overline{M}_{36-71}/H_{36-71}$ if $M_0=0$. When the \$ strobe occurs at the end of GD1, the following events take place:

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COMPUTER EQUIPMENT DEPARTMENT
PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh.12-259 Sh. No.12-258

TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR

12.3.11.1 - contd

- 1) The GD1 cycle is reset and GD2 cycle is set.
- 2) \$N₀₋₇₁ is generated and loads all zeros into N since no IN switch is enabled.
- 3) \$H is generated transferring the divisor into H.
If the original divisor was positive the one's complement of M is strobed into H at this time and K₇₂ is set to create an effective negative divisor. This is retained until the G=2 cycle.
- 4) ϕ S₀₋₃₅/AQ₀₋₃₅, ϕ S₃₆₋₇₁/AQ₃₆₋₇₁ and \$AQ₀₋₃₅, \$AQ₃₆₋₇₁ is generated to load the positive dividend into the AQ-register.
- 5) The Quotient Sign flip-flop (QSF) is set if the signs of the original dividend and divisor were different as indicated by $M_0 \neq A_0$.
- 6) The \$ strobe re-enters the Timing Pulse Generator delay line network to produce another \$ in about 400 nanoseconds.

GD2

During GD2 the negative divisor will be produced in the S adder and become available on the S bus. Switches are enabled during this time to transfer the positive dividend from AQ to N. The G counter is set to a count of 38 if the divisor is not equal to zero, and the Compare Magnitude flip-flop is set for comparison of the dividend and divisor during G ϕ . The Zero indicator is set if the divisor is zero, and a Divide Check Fault is generated.

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COMPUTER EQUIPMENT DEPARTMENT
PHOENIX, ARIZONA

Spec. No. M50EB00107
Cont. on Sh.12-260 Sh. No.12-259

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

12.3.11.1 - contd

The ZAQ and IN switches are enabled by $\phi AQ_0-35/$ ZAQ_0-35 , $\phi AQ_{36-71}/ZAQ_{36-71}$, $\phi ZAQ_0-35/N_0-35$ and $\phi ZAQ_{36-71}/N_{36-71}$.

When the \$ strobe occurs at the end of GD2, the following events take place:

- 1) The GD2 cycle is reset and the $G\phi$ cycle is set.
- 2) \$N is generated which strobes the divisor into the N-register.
- 3) \$G₀₋₇ is generated which strobes the count of 38 into the G-counter if the divisor is not zero ($S \neq 0$).
- 4) The Compare Magnitude flip-flop (CMFF) is set.
- 5) The Zero Indicator is set, and the Divide Check Fault strobe (\$DVCK) is sent to the BF if the divisor is zero ($S=0$). The Abort flip-flop is set in the OU and the OU is brought to an initialized state.
- 6) If a Divide Check did not occur because of a zero divisor, the \$ strobe re-enters the Timing Pulse Generator to produce another \$ strobe in about 400 nanoseconds.

$G\phi$ (CMFF)

The magnitude of the divisor and dividend mantissas are compared in the S-adder at this time to determine whether the actual divide process is ready to begin. One of two conditions will exist and operation of the $G\phi$ (CMFF) cycle will be affected as follows:

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GENERAL ELECTRIC COMPANY
COMPUTER EQUIPMENT DEPARTMENT
PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh.12-261 Sh. No.12-260

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

12.3.11.1 - contd

- 1) If the $|\text{dividend mantissa}| \geq |\text{divisor mantissa}|$, the divide operation is not ready to begin.

In this case, the dividend mantissa is shifted right one bit position and the dividend exponent is increased by one. The CMFF will remain set and the G-counter will not be decremented. The control points enabled for this are $\phi N_0/N_0$, $\phi N_{0-34}/N_{1-35}$, $\phi N_{35-70}/N_{36-71}$ to shift the dividend mantissa right, and $\phi \text{CARRY}/ES_7$, $\phi ES_{0-9}/E_{0-9}$ to increment the dividend exponent.

When $\$$ strobe occurs at the end of this $G\emptyset$ (CMFF) cycle the following events occur:

- 1) $\$N$ is generated to complete the right shift of the dividend.
- 2) $\$E_{0-9}$ is generated to increment the dividend exponent register.
- 2) If the $|\text{dividend mantissa}| < |\text{divisor mantissa}|$, the divide operation is ready to begin.

In this case, the dividend mantissa will be shifted left one bit position, the AQ-registers will be cleared, and the G-counter will be decremented by one. The control points enabled for this are $\phi N_{1-35}/N_{0-34}$, $\phi N_{36}/N_{35}$, $\phi N_{37-71}/N_{36-70}$ to shift the dividend mantissa left, and ϕFCD to decrement the G-counter.

When the $\$$ strobe occurs at the end of this $G\emptyset$ (CMFF) cycle, the following events occur:

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COMPUTER EQUIPMENT DEPARTMENT
PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh.12-262 Sh. No.12-261

TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR

12.3.11.1 - contd

- 1) $\$N$ is generated which enables the left shift of the dividend mantissa.
- 2) $\$AQ_0-71$ clears the AQ-register.
- 3) $\$G_0-7$ enables decrementation of the G-counter.
- 4) $\$$ and $\overline{SC}_0$ will reset the CMFF flip-flop.

$G\emptyset (G>3)(\overline{CMFF})$

During the next 34 $G\emptyset$ cycles or until the G-counter equals 3, all but the last of the divide subcycles are completed to produce the quotient in the A-register. For each of these 34 $G\emptyset$ cycles the magnitude of the divisor mantissa in the H-register is subtracted from the magnitude of the dividend mantissa in the N-register, the subtraction taking place in the S-adder. If there is a carry from the most significant bit of the S-adder ($SC_0=1$) indicating that the $|current\ dividend\ mantissa| \geq |divisor\ mantissa|$, or in other words, that the current dividend is divisible by the divisor, then the adder result (remainder) is shifted left one bit and transferred to the H-register to become the new dividend for the divide operation to be performed in the next $G\emptyset$ cycle. The control points enabled for this are $\phi S_1-36/N_0-35$ and $\phi S_{37-71}/N_{36-70}$. If there is no carry from bit zero of the adder (the current, dividend mantissa < divisor mantissa or in other words, the dividend mantissa is not divisible by the divisor mantissa), the contents of the N-register (current dividend mantissa) are shifted left one bit position to form a new dividend for the divide operation to be performed in the next $G\emptyset$ cycle. The control points enabled for this are $\phi N_1-35/N_0-34$, $\phi N_{36}/N_{35}$, and $\phi N_{37-71}/N_{36-70}$.

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PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh.12-263 Sh. No.12-262

TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR

12.3.11.1 - contd

At the end of each of the 34 $G\emptyset$ ($G>3$) cycles, a new partial quotient is formed. This is accomplished by shifting the contents of the AQ-register left one bit position and transferring the contents of the S-adder carry output (SC_0) to bit 35 of the A-register. Thus the quotient is generated, one bit per $G\emptyset$ ($G>3$) cycle with the most significant bit being generated first. The control points enabled for this are $\phi AQ_1-36/ZAQ_0-35$, $\phi AQ_37-71/ZAQ_36-70$, $\phi ZAQ_0-35/AQ_0-35$, and $\phi SC_0/AQ_35$. ϕFCD also is present to enable decrementation of the G-counter by one.

When the \$ strobe occurs at the end of each $G\emptyset(G>3)$ cycle the following events occur:

- 1) \$N enables the loading of a new dividend into the N-register, the generation of the new dividend being dependent on the state of the carry from the adder bit zero.
- 2) \$AQ₀₋₃₅ enables formation of a new partial quotient thru shifting of the old partial quotient left one bit position and loading a new quotient bit into AQ₃₅.
- 3) \$G₀₋₇ decrements the G-counter by one.
- 4) The \$ strobe re-enters the Timing Pulse generator to produce a subsequent \$ 320 nanoseconds later.

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COMPUTER EQUIPMENT DEPARTMENT
PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh.12-264 Sh. No.12-263

TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR

12.3.11.1 - contd

GØ (G=3)

At the time the G-counter is decremented to G=3, the last subtraction of the divisor mantissa from the dividend mantissa has been performed. In this cycle, the result of the last subtraction is used to form the last partial quotient. The last partial quotient is formed by shifting the contents of the AQ-register left one bit position and loading the content of the S-adder carry output (SC₀) into bit 35 of the A-register. The K₇₂ flip-flop is reset, the H-register is cleared, and the G-counter is decremented by one. The control points enabled for this are ϕ AQ₁₋₃₆/ZAQ₀₋₃₅, ϕ AQ₃₇₋₇₁/ZAQ₃₆₋₇₀, ϕ ZAQ₀₋₃₅/AQ₀₋₃₅, ϕ ZAQ₃₆₋₇₁/AQ₃₆₋₇₁, ϕ SC₀/AQ₃₅, and ϕ FCD. It should be noted that the control point ϕ SC₀/AQ₃₅ overrides the ϕ ZAQ/AQ for bit 35.

When the \$ strobe occurs at the end of GØ (G=3), the following events occur:

- 1) \$AQ₀₋₃₅ enables shifting and loading the last partial quotient in the A-register.
- 2) \$H₀₋₇₁ clears the H-register since no input switches are activated.
- 3) \$G₀₋₇ enables G-counter decrementation.
- 4) \$ resets K₇₂.
- 5) The \$ strobe propagates the medium delay logic and appears after a delay of 320 nanoseconds.

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COMPUTER EQUIPMENT DEPARTMENT
PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh.12-265 Sh. No.12-264

TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR

12.3.11.1 - contd

GØ (G=2)

During the GØ (G=2) cycle the Quotient Sign flip-flop (QSF) determines whether the final quotient must be sign-corrected. If the quotient must be corrected to negative (QSF=1), the complement of the AQ-register is transferred into the N-register and the K72 flip-flop is set. The control points enabled for this are $\phi AQ0-35/ZAQ0-35$, $\phi AQ36-71/ZAQ36-71$, $\phi ZAQ0-35/N0-35$, $\phi ZAQ36-71/N36-71$. If the quotient does not need to be sign corrected (QSF=0), the contents of the AQ-register are transferred to the N-register. The control points enabled for this are $\phi AQ0-35/ZAQ0-35$, $\phi AQ36-71/ZAQ36-71$, $\phi ZAQ0-35/N0-35$, and $\phi ZAQ36-71/N36-71$.

When the \$ strobe occurs at the end of the GØ (G=2) cycle the following events occur:

- 1) \$N enables the quotient (complemented or not) to be loaded into the N-register.
- 2) \$G0-7 enables decrementing of the G-counter.
- 3) The \$ strobe re-enters the Timing Pulse Generator to produce another \$ after a delay of 400 nanoseconds.

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COMPUTER EQUIPMENT DEPARTMENT
PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh.12-266 Sh. No.12-265

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

12.3.11.1 - contd

GØ (G=1)

At the time the G-counter equals one the divisor exponent is subtracted from the dividend exponent, and the difference is placed in the E-register. The control points enabled for this are $\phi D_{0-7}/ES_{0-9}$ and $\phi CARRY/ES_7$. Should the Zero indicator be set, indicating a quotient mantissa of zero, the E-register bit zero is forced to a one state ($E_0=1$) replacing the exponent difference. This is done to indicate a division result of floating point zero, defined as 0×2^{-128} . This is accomplished by enabling $\phi 2^7/E_{0-7}$. The quotient is returned to the AQ-register via $\phi S_{0-35}/AQ_{0-35}$ and the Sign and Zero indicators are set accordingly.

If the quotient is non-zero ($S \neq 0$) and $S_0 \neq S_1$, it is sent to the AQ-register via $\phi S_{0-35}/AQ_{0-35}$. Should $S_0 = S_1$, indicating an unnormalized quotient, it is retained for normalization and not sent to the A-register at this time.

When the \$ strobe occurs at the end of GØ (G=1) cycle the following takes place:

- 1) The Sign indicator is set if bit zero of the S-adder is a one ($S_0=1$), otherwise it is reset.
- 2) The E-register is strobed with the output of the ES-adder.
- 3) K_{72} is reset.
- 4) If the quotient is zero ($S=0$) or if the quotient is nonzero and bits zero and one of the S-adder are different ($S \neq 0$) ($S_0 \neq S_1$) the final quotient is strobed into the A-register by ϕAQ_{0-35} .

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GENERAL ELECTRIC COMPANY
COMPUTER EQUIPMENT DEPARTMENT
PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh.12-267 Sh. No.12-266

TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR

12.3.11.1 - contd

- 5) The Zero Indicator is set if $S=0$.
- 6) The $G\emptyset$ cycle flip-flop is reset and the GN cycle flip-flop is set if $(S\neq 0)(S_0=S_1)$, or the GF cycle flip-flop is set if $S=0$ or if $S_0\neq S_1$.
- 7) The \$ strobe propagates the slow delay logic after 400 nanoseconds during GF, or it exits the fast delay logic after 230 nanoseconds during GN.

GN

The normalization of the mantissa during a FDU is identical to the action described during GN of a $FN\emptyset$ instruction, see section 3.3.12.1.

GF

If the GF cycle was preceeded by a GN, the GF of the FDU is identical to the GF of the instruction $FN\emptyset$, see section 12.3.12.1.

Should the resulting quotient have been found to be normalized during $(G\emptyset)(G=1)$ the only activity as a result of GF is the generation of a \$ LAST. This pulse signals the control frame (CU) that the operations unit ($\emptyset U$) has completed an instruction.

FDI

The instruction Floating Divide Inverted operates as the name implies. The contents of the A-register, bits zero to twenty eight, being the divisor mantissa and the contents of some location Y, bits eight to thirty-five, becoming the dividend mantissa. This is accomplished by switching the contents of the A-register with the H-register during the GD2 cycle.

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PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh.12-268 Sh. No.12-267

TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR

12.3.11.1 - contd

Exponent manipulation is also reversed by subtracting the $C(E_{0-7})$ from some location Y bits $0-7$.

The loading of the dividend is accomplished through the control points $\phi ZDI_{8-35}/M_{0-27}$ and $\phi ZDI_{0-7}/M_{64-71}$.

GS

The action during this timing cycle is the same as during the FDV instruction, except that the $C(AQ)$ are converted to a negative mantissa.

GD1

As in GS the events during the GD1 cycle are the same as in the FDV instruction, except that the $C(M)$ is converted to a positive mantissa.

GD2

During the GD2 divide cycle the contents of the AQ and H-registers and the E and D-registers are reversed. This is accomplished by enabling the following control points: $\phi S_{0-35}/N_{0-35}$, $\phi S_{36-71}/N_{36-71}$, $\phi AQ_{0-35}/ZAQ_{0-35}$, $\phi AQ_{36-71}/ZAQ_{36-71}$, $\phi ZAQ_{0-35}/H_{0-35}$, $\phi ZAQ_{36-71}/H_{36-71}$, $\phi ES_{0-7}/D_{0-7}$, $\phi D_{0-7}/E_{0-9}$.

When the \$ occurs at the end of the GD2 cycle the following events take place:

- 1) The dividend mantissa is strobed into the N-register.

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PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh.12-269 Sh. No.12-268

TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR

12.3.11.1 - contd

- 2) The divisor mantissa is strobed into the H-register.
- 3) The dividend exponent is strobed into the E-register.
- 4) The divisor exponent is strobed into the D-register.
- 5) K72 is reset.
- 6) The GØ cycle flip-flop is set, and the CMFF flip-flop is set.

The remaining portion of the instruction is the same as the sequence during FDV.

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PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh.12-270 Sh. No.12-269

TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR

12.3.11.2 Double Precision

DFDV

The Double Precision Floating Divide instruction (DFDV) is basically the same as the Floating Divide Instruction (FDV) with the following exceptions.

- 1) The divisor mantissa consists of C(Y)₈₋₃₅ and C(Y+1)₀₋₃₅.
- 2) The G-counter is set to a count of 66 during the GD2 cycle.
- 3) The carry out of S₀ will be inserted into AQ₆₃.
- 4) The quotient mantissa will be contained in C(AQ)₀₋₆₃ at the end of GF.

For a detailed explanation see section 12.3.11.1.

DFDI

The Double Precision Floating Divide Inverted (DFDI) is identical to the Floating Divide Inverted (FDI) instruction with the following exceptions:

- 1) The dividend mantissa consists of the C(Y)₈₋₃₅ and C(Y+1)₀₋₃₅.
- 2) The divisor mantissa is contained in the C(AQ)₀₋₆₃.
- 3) The G-counter is set to a count of 66 during the GD2 cycle.

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GENERAL ELECTRIC COMPANY
COMPUTER EQUIPMENT DEPARTMENT
PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh. 12-271 Sh. No. 12-270

TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR

12.3.11.2 - contd

- 4) The carry out of S_0 will be inserted into AQ_{63} .
- 5) The quotient mantissa will be contained in the $C(AQ)_{0-63}$ at the end of GF.

For a detailed explanation see section 12.3.11.1.

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COMPUTER EQUIPMENT DEPARTMENT
PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh12-272 Sh. No.12-271

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

12.3.12 FLOATING POINT SPECIAL INSTRUCTIONS

This group of two instructions completes the floating point repertoire. They are FNO and FNEG.

12.3.12.1 FNO (Floating Normalize)

Generally, floating point numbers are normalized by shifting the mantissa left and correspondingly decreasing the exponent until no leading zeros are present in the value portion of the mantissa for positive numbers or until no leading ones are present in the value normalize mantissa for negative numbers. Zeros fill in the bit positions vacated on the right in either case.

$$(AQ)_{0-71} \xleftarrow[X]{} (AQ)_{0-71}$$

$$E_{0-7} - X \Rightarrow (E_{0-7})$$

L denotes left shift

X denotes the number of shifts required
to first satisfy the condition $\bar{A}_0 A_1 + A_0 \bar{A}_1$

In the special case of OFLI being set when FNO is entered, the FNO instruction is executed by shifting the mantissa to the right one bit position, replacing the vacated bit position (sign bit) with the inverse of its previous contents, and incrementing the exponent by one as expressed below:

$$(AQ)_{0-70} \Rightarrow (AQ)_{1-71}, (A_0) \Rightarrow (\bar{A}_0)$$

$$\text{and } E_{0-7} + 1 \Rightarrow E_{0-7}$$

COMPANY CONFIDENTIAL

GENERAL ELECTRIC COMPANY
COMPUTER EQUIPMENT DEPARTMENT
PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh.12-273 Sh. No.12-272

TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR

12.3.12.1 - contd

GS

During the GS cycle the H-register is cleared. The contents of the AQ-register are gated through the ZAQ bus and into the N-register. The Sign and Zero flip-flops are both reset and at the end, the GO flip-flop is set.

GO

If the overflow indicator is set as a result of some previous operation, the REV flip-flop will be set.

The operand is examined in the S-adder (outputs of the N- and H-registers are constantly fed to the S-adder and since the H-register was cleared during GS, the S-adder contains only the operand during GO), and if the contents of the S-adder are not zero and $S_0 = S_1$, or if the overflow indicator is set from some previous operation, the GN flip-flop will be set which will start the normalize cycle. If $S_0 = 1$, the Sign flip-flop will be set. If the S-adder contains all zeros, the Zero flip-flop will be set.

The G-counter will be cleared by strobing while no input controls are active.

The GN cycle is now entered if the GN flip-flop is set.

GN

During the GN cycle, the contents of the N-register may be left undisturbed (first GN cycle only), shifted right one, or shifted left one, four or sixteen bit positions. This shifting is accomplished in the N-register with its associated shifting logic. The conditions which control shifting, together with resulting action are tabulated below:

COMPANY CONFIDENTIAL

GENERAL ELECTRIC COMPANY
COMPUTER EQUIPMENT DEPARTMENT
PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh.12-274 Sh. No.12-273

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

12.3.12.1 - contd

CONDITIONS	ACTION
1) REV FF Set	$N_{0-70} = N_{1-71}, N_0 = N_0$ (Shift right one)
2) $[GN][\overline{REV}][\overline{ZERO}][(N_0 \dots N_{15}) + (\overline{N}_0 \dots \overline{N}_{15})]$ (Bits 0-15 of the N-register are alike, the REV flip-flop is not set and the ZERO flip-flop is not set.)	$N_{16-71} = N_{0-55}, 0 = N_{56-71}$ (Shift left sixteen)
3) $[GN][\overline{REV}][\overline{ZERO}][(N_0 \dots N_3) + (\overline{N}_0 \dots \overline{N}_3)][(N_0 \dots N_{15}) + (\overline{N}_0 \dots \overline{N}_{15})]$ (Bits 0-3 of the N-register are alike, the REV flip-flop is not set, the ZERO flip-flop is not set, and bits 0-15 of the N-register are not alike.)	$N_{4-71} = N_{0-67}, 0 = N_{68-71}$ (Shift left four)
4) $[GN][\overline{REV}][\overline{ZERO}][N_0 N_1 + \overline{N}_0 \overline{N}_1]$ $[(N_0 \dots N_3) + (\overline{N}_0 \dots \overline{N}_3)]$ (Bits 0 and 1 of the N-register are alike, the REV flip-flop is not set, ZERO flip-flop is not set, and bits 0-3 of the N-register are not alike.)	$N_{1-71} = N_{0-70}, 0 = N_{71}$ (Shift left one)

COMPANY CONFIDENTIAL

GENERAL ELECTRIC COMPANY
COMPUTER EQUIPMENT DEPARTMENT
PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh.12-275 Sh. No.12-274

TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR

12.3.12.1 - contd

If a shift of four or sixteen is required, the possibility of an overshift of one bit exists.

For example, if bits 0-3 are all zeros and bit 4 is a one, a left shift of four will be made. In this case, the sign bit will be changed from plus to minus, which case is included in the definition of overshift.

If the shifting action called for will result in an overshift, the REV flip-flop gets set in the current GN cycle so that a right shift of one will be executed in the next GN cycle to correct for the overshift.

The fact that an overshift will be made in the current GN cycle is detected by implementation of the following logic expression:

$$[GN][\overline{REV}][\overline{ZERO}][(N_0 \dots N_{15}) + (\overline{N}_0 \dots \overline{N}_{15})][N_0 \overline{N}_{16} + \overline{N}_0 N_{16}] + \\ [GN][\overline{REV}][\overline{ZERO}][(N_0 \dots N_3) + (\overline{N}_0 \dots \overline{N}_3)][N_0 \overline{N}_4 + \overline{N}_0 N_4]$$

The information needed for properly decrementing the exponent register is retained in the G-counter. The number of shifts made in each GN cycle are added to the contents of the G-counter by means of control logic and appropriate control signals. In the case where a right shift is required due to a previous overflow or an overshift in a previous GN cycle, the signal "Full Counter Decrement" is applied and causes the G-counter to be decremented by one.

Generation of the signal LSN (last normalize shift) determines whether the normalization is complete with the current GN cycle or whether further GN cycle(s) are required. The following logic is implemented to generate LSN.

COMPANY CONFIDENTIAL

GENERAL ELECTRIC COMPANY
COMPUTER EQUIPMENT DEPARTMENT
PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh.12-276 Sh. No.12-275

TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR

12.3.12.1 - contd

$$\begin{aligned} \text{LSN} = & [(N \text{ DET } 1)(N_1\bar{N}_2 + \bar{N}_1N_2) + (N \text{ DET } 4_B)(\bar{N}_4N_5) + \\ & (N \text{ DET } 4_B)(N_4\bar{N}_5) + (N \text{ DET } 16_B)(\bar{N}_{16}N_{17}) + \\ & (N \text{ DET } 16_A)(N_{16}\bar{N}_{17}) + (N_0\bar{N}_1 + \bar{N}_0N_1) + \text{REV}] \text{ GN} \end{aligned}$$

This specifies that if the bits which will replace bits N_0 and N_1 in this shift cycle are not equal, normalization of the mantissa will be complete with this shift cycle.

A GF cycle follows the last GN cycle.

GF

At the end of the last GN cycle, the normalized mantissa is contained in the S adder since the contents of the N-register and the H-register are constantly being summed and the H-register was cleared during the GS cycle.

The normalized mantissa is gated and strobed into the AQ-register from the S-adder.

The contents of the G-counter are gated to the ES- (Exponent) adder together with a carry bit to the ES_7 for addition to the contents of the ES-register. This addition of the two's complement of the contents of the G-counter effects a subtraction of it from the contents of the ES-register. The resulting contents of ES_{0-7} are gated and strobed into the ES-register if the ZERO indicator is not set. If the ZERO indicator is set, a one is forced into bit 0 of the ES-register. This yields an exponent equal to -2^7 or -128 which, with a mantissa of $0.00\dots 0$, has been defined as the machine representation of the number zero.

If an exponent underflow or overflow exists, the appropriate flip-flop will be set.

COMPANY CONFIDENTIAL

GENERAL ELECTRIC COMPANY
COMPUTER EQUIPMENT DEPARTMENT
PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh.12-277 Sh. No.12-276

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

12.3.12.2 FNEG (Floating Negate)

In general, the Floating Point Negate instruction is performed by forming the two's complement of the mantissa contained in the AQ-register and then normalizing the resultant.

GS

During the GS cycle the H-register is cleared by strobing with no input control activated.

The contents of the AQ-register are gated to the ZAQ bus and ZAQ is gated and strobed into the N-register. This puts the one's complement of the mantissa into the N-register.

The Sign and Zero flip-flops are both reset and K_{72} flip-flop is set.

The outputs of the N- and H-registers are constantly summed in the S-adder and K_{72} is also added into the least significant bit position. Since the H-register is cleared to zero, adding K_{72} to the one's complement of the operand results in the two's complement in the S-adder.

GO

During the GO cycle the contents of the S-adder are gated and strobed into the N-register.

The REV flip-flop is set if the overflow condition is present. That is, if $C_0C_1 + C_0\bar{C}_1$ is true.

The GN flip-flop will be set if the overflow condition is present or if the contents of the S-adder are not zero and S_0 and S_1 are alike (indicating that the number is not normalized).

COMPANY CONFIDENTIAL

GENERAL ELECTRIC COMPANY
COMPUTER EQUIPMENT DEPARTMENT
PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh.12-278 Sh. No. 12-277

TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR

12.3.12.2 - contd

The Sign indicator will be set according to the following logic:

$$\text{Set SIGN} = S_0 \cdot \overline{\text{OVERFLOW CONDITION}} + \overline{S_0} \cdot \text{OVERFLOW CONDITION}$$

The Zero flip-flop will be set if the contents of the S-adder are zero.

K₇₂ flip-flop will be reset.

GN-GF

If the GN flip-flop is set, the next cycle will be a GN cycle, otherwise the next cycle will be a GF cycle. In either case, the action from this point is identical to that described for the same timing cycles of the FNO instruction except that if the overflow indicator is set, it does not get reset in the GF cycle as it does for a FNO instruction.

COMPANY CONFIDENTIAL

GENERAL ELECTRIC COMPANY
COMPUTER EQUIPMENT DEPARTMENT
PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh.12-279 Sh. No.12-278

TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR

12.4

G-COUNTER DESCRIPTION

The G-counter provides:

- 1) Sequence control for all instructions requiring multiple operation cycles. For example, multiply, divide, and GTB instructions.
- 2) Control for executing the specified number of shifts and the bits per shift cycle sequence during shift instructions.
- 3) Control for executing the required number of mantissa alignment shifts and the bits per align cycle sequence for floating instructions.
- 4) Register capability for accumulating the number of bit positions a mantissa is shifted during a normalization cycle.

The G-counter is an 8-bit counter/register which can assume the following logical configurations dependent upon the function it is performing:

- 1) Eight-bit decremental counter when providing sequence control for multiply, divide, and GTB instructions. The number of operation cycles required by each instruction is inserted in the counter and decremented by one after each operation cycle.

Other special functions require this full counter decrement-by-one capability and are discussed in paragraph 12.4.13.

COMPANY CONFIDENTIAL

GENERAL ELECTRIC COMPANY
COMPUTER EQUIPMENT DEPARTMENT
PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh.12-280 Sh. No.12-279

TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR

12.4 - contd

- 2) Three individual counters each having decremental capability. Shifts and/or aligns are performed by shifting either 16-, 4-, or 1-bit(s) per cycle. The number of shifts of 16 are defined by bits G_{1-3} , shifts of 4 by G_{4-5} , and shifts of 1 by G_{6-7} . Each of these counters is individually decremented in a 16, 4, 1 order.
- 3) Three individual counters each having incremental capability, as a parallel to the execution of shifts or aligns. Normalization shifts are accrued by the G-counter in a 16, 4, 1 order. The number of shifts of 16 are accrued in G_{1-3} , shifts of 4 in G_{4-5} , and shifts of 1 in G_{6-7} . The total number of normalization shifts is sent to the exponent section to perform exponent correction.

COMPANY CONFIDENTIAL

GENERAL ELECTRIC COMPANY
COMPUTER EQUIPMENT DEPARTMENT
PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh.12-281 Sh. No.12-280

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

12.4.1 G-COUNTER CONTROL DURING MULTIPLY, DIVIDE AND
GTB INSTRUCTIONS

12.4.1.1 Operation Cycles Required

The following table lists the number of operation cycles required for each operation and the timing cycle during which this number is inserted in the G-counter. This number will be decremented by one at the end of each GO cycle.

FIXED COUNT INSERTION

<u>Inst.</u>	<u>Set G =</u>	<u>Timing Cycle</u>	<u>G₁G₂G₃G₄G₅G₆G₇</u>
FMP	15	GS	0 0 0 1 1 1 1
UFM	15	GS	0 0 0 1 1 1 1
DFMP	33	GS	0 1 0 0 0 0 1
DUFM	33	GS	0 1 0 0 0 0 1
FMP _{DU}	6	GS	0 0 0 0 1 1 0
UFM _{DU}	6	GS	0 0 0 0 1 1 0
DFMP _{DU}	6	GS	0 0 0 0 1 1 0
DUFM _{DU}	6	GS	0 0 0 0 1 1 0
MPF	19	GS	0 0 1 0 0 1 1
MPY	19	GS	0 0 1 0 0 1 1
MPF _{DU}	10	GS	0 0 0 1 0 1 0
MPF _{DL}	19	GS	0 0 1 0 0 1 1
MPY _{DU}	10	GS	0 0 0 1 0 1 0
MPY _{DL}	19	GS	0 0 1 0 0 1 1
DVF	38	GD2	0 1 0 0 1 1 0
DIV	38	GD2	0 1 0 0 1 1 0
FDV	38	GD2	0 1 0 0 1 1 0
DFDV	66	GD2	1 0 0 0 0 1 0
FDI	38	GD2	0 1 0 0 1 1 0
DFDI	66	GD2	1 0 0 0 0 1 0
FDV _{DU}	38	GD2	0 1 0 0 1 1 0
DFDV _{DU}	66	GD2	1 0 0 0 0 1 0
FDI _{DU}	38	GD2	0 1 0 0 1 1 0
DFDI _{DU}	66	GD2	1 0 0 0 0 1 0
BCD	6	GD2	0 0 0 0 1 1 0
GTB	36	GS	0 1 0 0 1 0 0

DU = Direct Upper
Modifier

DL = Direct Lower
Modifier

COMPANY CONFIDENTIAL

GENERAL ELECTRIC COMPANY
COMPUTER EQUIPMENT DEPARTMENT
PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh.12-282 Sh. No.12-281

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

12.4.1.2

Fixed Count Insertion Control Equations

Decode: (1) = $V_4 V_7 = \text{DFDV} + \text{DFDI}$
(2) = $V_4 \bar{V}_7 = \text{FDV} + \text{FDI}$
(3) = $\bar{V}_4 V_7 = \text{DVF} + \text{DIV}$
(4) = $\bar{V}_4 \bar{V}_7 = \text{BCD}$
(5) = $V_0 \bar{V}_1 V_4 \bar{V}_5 \bar{V}_6 V_7 = \text{DFMP} + \text{DUFM}$
(6) = $V_0 \bar{V}_1 \bar{V}_4 \bar{V}_5 \bar{V}_6 = \text{MPF} + \text{MPY}$
(7) = $V_0 \bar{V}_1 \bar{V}_2 V_4 \bar{V}_5 \bar{V}_6 \bar{V}_7 = \text{FMP} + \text{UFM}$
(8) = $V_2 V_4 V_5 \bar{V}_7 \bar{V}_8 = \text{GTB}$

(1) FIXED COUNT/G1 = $[\text{DFDV} + \text{DFDI} + (\text{DFDV} + \text{DFDI}) \text{DU}] (\text{GD2})$
= (1) (GD2)
(2) FIXED COUNT/G2 = $[(\text{FDI} + \text{FDV}) + (\text{DVF} + \text{DIV}) + (\text{FDI} + \text{FDV}) (\text{DU})] (\text{GD2}) + (\text{DFMP} + \text{DUFM} + \text{GTB}) (\text{GS})$
= $[(2 + 3)] (\text{GD2}) + [(5) (\text{DU}) + (8)] (\text{GS})$
(3) FIXED COUNT/G3 = $[(\text{MPF} + \text{MPY}) + (\text{MPF} + \text{MPY}) \text{DL}] (\text{GS})$
= (6) (DU) (GS)
(4) FIXED COUNT/G4 = $[(\text{MPF} + \text{MPY}) (\text{DU}) + (\text{FMP} + \text{UFM})] (\text{GS})$
= $[(6) (\text{DU}) + (7) (\text{DU})] (\text{GS})$
(5) FIXED COUNT/G5 = $[(\text{FDI} + \text{FDV}) + (\text{FDI} + \text{FDV}) (\text{DU}) + (\text{DVF} + \text{DIV}) + \text{BCD}] (\text{GD2})$
+ $[(\text{FMP} + \text{UFM}) + (\text{FMP} + \text{UFM}) (\text{DU}) + (\text{DFMP} + \text{DUFM}) (\text{DU}) + \text{GTB}] (\text{GS})$
= $[2 + 3 + 4] (\text{GD2}) + [7 + (5) (\text{DU}) + 8] (\text{GS})$

COMPANY CONFIDENTIAL

GENERAL ELECTRIC COMPANY
COMPUTER EQUIPMENT DEPARTMENT
PHOENIX, ARIZONA

Spec. No.M50EB00107

Cont. on Sh.12-283 Sh. No.12-282

TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR

12.4.1.2 - contd

$$\begin{aligned} \textcircled{6} \quad \text{FIXED COUNT/G6} &= [(FMP + UFM) + (FMP + UFM) DU \\ &\quad + (DFMP + DUFM) DU + (MPF + MPY) \\ &\quad + (MPF + MPY) DU + (MPF + MPY) (DL)] (GS) \\ &\quad + [(DVF + DIV) + (FDI + FDV) \\ &\quad + (FDI + FDV) DU + BCD](GD2) \\ &\quad + (DFDV + DFDI) (GD2) \\ &= [7 + 6 + 5 (DU)](GS) + (1+3+2+4) (GD2) \end{aligned}$$

$$\begin{aligned} \textcircled{7} \quad \text{FIXED COUNT/G7} &= [(FMP + UFM) + (MPF + MPY) + (MPF + MPY) DL \\ &\quad + (DFMP + DUFM)] (GS) \\ &= [(7 + 6 + 5) (\overline{DU})] (GS) \end{aligned}$$

$$\begin{aligned} \textcircled{8} \quad &DU = \text{DIRECT MODIFIER FLIP-FLOP} \\ &\$ \text{ SET DUMF} = [\$DUMF]_{CF} \\ &\text{RESET DUMF} = (\$) (GF) (DUMF)_{\Delta} + \text{ABORT} \end{aligned}$$

COMPANY CONFIDENTIAL

GENERAL ELECTRIC COMPANY
COMPUTER EQUIPMENT DEPARTMENT
PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh.12-284 Sh. No.12-283

TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR

12.4.2 G-COUNTER CONTROL DURING SHIFTS OR ALIGNS

12.4.2.1 Philosophy of Align Count Control During Floating Operations

Problem Statement

In performing floating-point addition and subtraction where the register bits are handled in parallel (to achieve computation speeds limited by circuit speeds and a practical degree of logic complexity), it is necessary to compare the magnitude of the exponents of addend and augend (for addition) or subtrahend and minuend (for subtraction) to determine how much the mantissa, associated with the smaller exponent, must be shifted to the right so as to achieve the digit alignment required before actually forming a sum. The exponent comparison consists of subtracting the exponent of the word from memory from the exponent of the word held in an internal register. The resulting difference may be positive or negative. The sign determines which word is to be shifted right in the subsequent alignment. The magnitude determines how far right the shift is to proceed.

If either positive and/or negative magnitude representation is to be used in two's complement coding, then the magnitude decode logic will be twice as complex as that required for just positive number representation. This complexity may be avoided by converting any negative difference to its two's complement which is always positive and always has the identical magnitude. This alternative entails more time delay as the one's complement of the negative difference is added to unity (in the least bit position) to obtain the two's complement, and a carry may propagate the full length of the exponent adder. The following scheme avoids the delay of the two's complementation yet requires much less magnitude-detection logic than would be required by using both positive and negative differences in the two's complement coding.

COMPANY CONFIDENTIAL

GENERAL ELECTRIC COMPANY
COMPUTER EQUIPMENT DEPARTMENT
PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh.12-285 Sh. No.12-284

TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR

12.4.2.1 - contd

Absolute-Value Detection

The initial exponent subtraction is performed without change. (In the 635, subtraction is performed by adding the one's complement [bit complement] of the subtrahend to the minuend after setting the least-significant carry bit.) If the difference is positive (indicated by the most significant bit of the adder output having a zero value), then the difference is transferred to the G-counter for storage (and subsequent countdown during alignment shifts). If the difference is negative, the one's complement of the adder is transferred to the G-counter except the sign bit (most significant bit) retains the unity value which denotes a negative difference.

The contents of the G-counter therefore will hold the required number of align counts if the most significant bit of the counter is zero (positive) and will hold the align count less one if the most significant counter bit is unity (negative). The align-shift logic thus must account for the difference in apparent count according to the sign bit of the G-counter. For many magnitude values, adjacent combinations represent the two possible representations in the counter, hence in some cases the shift logic is very little more complex than just that of all-positive representation.

COMPANY CONFIDENTIAL

GENERAL ELECTRIC COMPANY
COMPUTER EQUIPMENT DEPARTMENT
PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh.12-286 Sh. No.12-285

TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR

12.4.2.1 - contd

Implementation

The G-counter has eight bits, so that excepting the sign bit 128 shifts can be counted. However, the mantissa register is limited to 72 bits so shift counts exceeding 71 simply result in the align mantissa becoming all zeros (including sign, hence the number zero). This mantissa-magnitude >71 detection takes place prior to transfer of difference to align counter, hence the >71 detection must work on conventional two's complement coding. A simple clearing of register substitutes for align-right shift shifting when the count exceeds 71. The following discussion assumes an align-shift count less than 72.

The 645 provides shifts of 16-, 4-, and 1-bit positions. Overshifting of 1-bit position is permitted, with subsequent correction, to achieve a significantly faster shifting operation. Thus, shift 16 is required whenever the align counter contains a number equivalent to 15 or more; shift 4 is required when the counter contains a number equivalent to 3 or more. All shifts of 16 must be performed before shifts of 4 and all shifts of 4 must be performed before shifts of 1. Overshift sets a Reverse flip-flop which signals that the next shift must be exactly 1-bit position in the opposite direction (under align which is normally a right shift, reverse calls for a left shift). The following table shows the required control combinations.

COMPANY CONFIDENTIAL

GENERAL ELECTRIC COMPANY
COMPUTER EQUIPMENT DEPARTMENT
PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh.12-287 Sh. No.12-286

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

12.4.2.1 Table -- G-Counter Contents

Req'd Count Magnitude	G-Counter Contents														Control Operations and Comments		
	Positive No.							Negative No.									
	G ₀	G ₁	G ₂	G ₃	G ₄	G ₅	G ₆	G ₇	G ₀	G ₁	G ₂	G ₃	G ₄	G ₅	G ₆	G ₇	
0	0	0	0	0	0	0	0	0									No negative representation of zero; do not shift
1	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	Shift right one, set counter to zero
2	0	0	0	0	0	0	1	0	1	0	0	0	0	0	0	1	Shift right one, decrement counter by one
3	0	0	0	0	0	0	1	1	1	0	0	0	0	0	1	0	Shift right four, set Reverse, set counter to zero
4	0	0	0	0	0	1	0	0	1	0	0	0	0	0	1	1	Shift right four, set counter to zero
5	0	0	0	0	0	1	0	1	1	0	0	0	0	1	0	0	Shift right four, decrement counter by four
⋮	⋮	⋮	⋮	⋮					⋮	⋮	⋮	⋮					⋮
13	0	0	0	0	1	1	0	1	1	0	0	0	1	1	0	0	Shift right four, decrement counter by four
14	0	0	0	0	1	1	1	0	1	0	0	0	1	1	0	1	Shift right four, decrement counter by four
15	0	0	0	0	1	1	1	1	1	0	0	0	1	1	1	0	Shift right 16, set Reverse, set counter to zero
16	0	0	0	1	0	0	0	0	1	0	0	0	1	1	1	1	Shift right 16, set counter to zero
17	0	0	0	1	0	0	0	1	1	0	0	1	0	0	0	0	Shift right 16, decrement counter by 16
⋮	⋮								⋮								⋮
71	0	1	0	0	0	1	1	1	1	1	0	0	0	1	1	0	Shift right 16, decrement counter by 16
72	0	1	0	0	1	0	0	0	1	1	0	0	0	1	1	1	Shift counts of 72 or greater will not be put into counter for purposes of mantissa alignments.

COMPANY CONFIDENTIAL

GENERAL ELECTRIC COMPANY
COMPUTER EQUIPMENT DEPARTMENT
PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh.12-288 Sh. No.12-287

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

12.4.2.1 - contd

Control Logic Resulting from Hybrid Coded Table

$$\text{Shift 16} = G_1 + G_2 + G_3 + G_4 \cdot G_5 \cdot G_6 (G_0 + G_7) = \text{SH16}$$

$$\text{Shift 4} = (\overline{\text{SH16}}) (G_4 + G_5 + G_6 [G_0 + G_7]) = \text{SH4}$$

$$\text{Shift 1} = (\overline{\text{SH16}}) (\overline{\text{SH4}}) (G_0 + G_6 + G_7) = \text{SH1}$$

$$\text{Set Reverse} = ([\text{SH16}] \bar{G}_1 \bar{G}_2 \bar{G}_3 + [\text{SH4}] \bar{G}_4 \bar{G}_5) (\bar{G}_0 + \bar{G}_7)$$

$$\text{Clear G} = (\text{Last Align Shift}) + (|\text{Exponent Diff}| > 71)$$

Last Align

$$\begin{aligned} \text{Shift} = & (G=16) + (G=4) + (G=1) + (G=-113) + G=-125) \\ & + (G=-128) + \text{REV} \end{aligned}$$

With the exception of the "Last Align Shift" signal, the term " $G_0 + G_7$ " or the term " $G_0 + G_7$ " constitute the main difference in logical complexity between the requirements of this hybrid code scheme and an all-positive number representation (as would be obtained by two's complementing negative counts). This demonstrates the economy of this code scheme with this particular shifting scheme. The justification would be weaker if the over-shift and reverse scheme were not used. The negative count representation if read directly will always be $2^{n-1} + 1 - N$ where n is the number of bits in the counter and N is the absolute (positive) value of the shift count. Thus, exponent differences of (-16), (-4), and (-1) will appear in the counter as (-113), (-124), and (-128) respectively.

NOTE: The shift 16, shift 4, and shift 1 logic developed above also is applicable to shift instructions.

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GENERAL ELECTRIC COMPANY
COMPUTER EQUIPMENT DEPARTMENT
PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh.12-289 Sh. No.12-288

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

12.4.2.2 Equations for Transfer of Align Count from ES- to G-Counter

E - D = Positive (E-register minus D-register)

1) $\phi ES_{0-7}/G_{0-7} = (GE)(\overline{ES}_0)(\overline{ES}/\geq 72)$

2) $\phi \text{ SET } G_{0-7}$

a) $\phi \text{ SET } G_0 = (\phi ES_{0-7}/G_{0-7})(ES_0)$

b) $\phi \text{ SET } G_1 = (\quad " \quad)(ES_1)$

c) $\phi \text{ SET } G_2 = (\quad " \quad)(ES_2)$

d) $\phi \text{ SET } G_3 = (\quad " \quad)(ES_3)$

e) $\phi \text{ SET } G_4 = (\quad " \quad)(ES_4)$

f) $\phi \text{ SET } G_5 = (\quad " \quad)(ES_5)$

g) $\phi \text{ SET } G_6 = (\quad " \quad)(ES_6)$

h) $\phi \text{ SET } G_7 = (\quad " \quad)(ES_7)$

E - D = Negative

1) $\phi \overline{ES}_{0-7}/G_{0-7} = (GE)(ES_0)(\overline{ES}/\geq 72)$

2) $\phi \text{ SET } G_{0-7}$

a) $\phi \text{ SET } G_0 = (\phi \overline{ES}_{0-7}/G_{0-7})(ES_0)$

b) $\phi \text{ SET } G_1 = (\quad " \quad)(\overline{ES}_1)$

c) $\phi \text{ SET } G_2 = (\quad " \quad)(\overline{ES}_2)$

d) $\phi \text{ SET } G_3 = (\quad " \quad)(\overline{ES}_3)$

e) $\phi \text{ SET } G_4 = (\quad " \quad)(\overline{ES}_4)$

f) $\phi \text{ SET } G_5 = (\quad " \quad)(\overline{ES}_5)$

g) $\phi \text{ SET } G_6 = (\quad " \quad)(\overline{ES}_6)$

h) $\phi \text{ SET } G_7 = (\quad " \quad)(\overline{ES}_7)$

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GENERAL ELECTRIC COMPANY
COMPUTER EQUIPMENT DEPARTMENT
PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh. 12-290 Sh. No. 12-289

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

12.4.2.3 Equations for Transferring the Number of Shift
Counts to G-Counter

$$\begin{aligned} 1) \quad \phi M_{11-17}/G_{1-7} &= (GS) \text{ (ALL SHIFTS)} \\ &= (GS) (V_0 V_1 V_2 V_4) (\overline{GTB}) \\ &= (GS) (V_0 V_1 V_2 V_4) (\overline{V_4 \overline{V_7} \overline{V_8}}) \end{aligned}$$

$$2) \quad \phi \text{ SET } G_{1-7}$$

$$a) \quad \phi \text{ SET } G_1 = (\phi M_{11-17}/G_{1-7})(M_{11})$$

$$b) \quad \phi \text{ SET } G_2 = (\quad " \quad)(M_{12})$$

$$c) \quad \phi \text{ SET } G_3 = (\quad " \quad)(M_{13})$$

$$d) \quad \phi \text{ SET } G_4 = (\quad " \quad)(M_{14})$$

$$e) \quad \phi \text{ SET } G_5 = (\quad " \quad)(M_{15})$$

$$f) \quad \phi \text{ SET } G_6 = (\quad " \quad)(M_{16})$$

$$g) \quad \phi \text{ SET } G_7 = (\quad " \quad)(M_{17})$$

COMPANY CONFIDENTIAL

GENERAL ELECTRIC COMPANY
COMPUTER EQUIPMENT DEPARTMENT
PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh.12-291 Sh. No.12-290

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

12.4.2.4 G-Counter Decrement During Shifts or Align

- 1) The execution of the number of shifts specified by the G-counter during all shift or align operations is on a 16, 4, and 1 sequential basis.

The G-counter is decremented by 16, 4, and 1 until the number of shift counts is expended. The controls for this shift order are:

- a) $GSH_{16} = (SHIFT\ 16)[GA + GO\ (SHIFTS)]$
b) $GSH_4 = SHIFT\ 4\ [GA + GO\ (SHIFTS)]$
c) $GSH_1 = SHIFT\ 1\ [GA + GO\ (SHIFTS)]$

- 2) Counter logic during three counter decrement control.

		n						
		G_1	G_2	G_3	G_4	G_5	G_6	G_7
a)	SET $G_7 = (G_6 \bar{G}_7)$	1	1	1	1	1	1	1
	RESET $G_7 = (G_7)$	1	1	0	1	0	1	0
b)	SET $G_6 = 0$	1	0	1	0	1	0	1
	RESET $G_6 = (G_6 \bar{G}_7)$	1	0	0	0	0	0	0
		0	1	1				
		0	1	0				
c)	SET $G_5 = (G_4 \bar{G}_5)$	0	0	1				
	RESET $G_5 = (G_5)$	0	0	0				
		n + 1						
		G_1	G_2	G_3	G_4	G_5	G_6	G_7
d)	SET $G_4 = 0$	1	1	0	1	0	1	0
	RESET $G_4 = G_4 \bar{G}_5$	1	0	1	0	1	0	1
e)	SET $G_3 = (\bar{G}_3)$	1	0	0	0	0	0	0
	RESET $G_3 = (G_3)$	0	1	1				
		0	1	0				
		0	0	1				
f)	SET $G_2 = (G_1 \bar{G}_2 \bar{G}_3)$	0	0	0				
	RESET $G_2 = (G_2 \bar{G}_3)$							

COMPANY CONFIDENTIAL

GENERAL ELECTRIC COMPANY
COMPUTER EQUIPMENT DEPARTMENT
PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh.12-292 Sh. No.12-291

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

12.4.2.4 - contd

g) SET $G_1 = 0$

RESET $G_1 = (G_1 \bar{G}_2 \bar{G}_3)$

3) "Clear" G-counter during shifts, align, or normalize.

a) The G-counter must clear to all zeros under the following conditions:

(1) $G = \pm 1 + G = \pm 4 + G = \pm 16$ For Shifts
or
(2) $G = \pm 3 + G = \pm 15$ Aligns

Each of these counts indicates a last cycle shift forthcoming and will require the setting of G to zero.

(3) $GF + (GS)(\bar{GF})$ For initialize

b) "Clear" equation:

Clear = $\{[(G = \pm 1) + (G = \pm 4) + (G = \pm 16)]$
 $+ [(G = \pm 3) + (G = \pm 15)]\}$

$\{GA + [ALL SHIFTS OPS][GO]\} + GF + GS \bar{GF}$

c) To insure that all cS/R Gi control points under control of GSH1, GSH4, or GSH16 are off when shift counts of 1, 4, 16, 3, or 15 are detected, the term clear is included in these control points as an inhibit.

COMPANY CONFIDENTIAL

GENERAL ELECTRIC COMPANY
COMPUTER EQUIPMENT DEPARTMENT
PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh.12-293 Sh. No.12-292

TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR

12.4.2.4 - contd

4) ϕ SET/RESET G_1 (under decrement by 16, 4, 1 control)

a) ϕ SET $G_7 = (\text{GSH1}) (\overline{\text{CLEAR}}) (G_6 \overline{G_7})$

ϕ RESET $G_7 = (\text{GSH1}) (\overline{\text{CLEAR}}) (G_7)$

b) ϕ SET $G_6 = 0$

ϕ RESET $G_6 = (\text{GSH1}) (\overline{\text{CLEAR}}) (G_6 \overline{G_7})$

c) ϕ SET $G_5 = (\text{GSH4}) (\overline{\text{CLEAR}}) (G_4 \overline{G_5})$

ϕ RESET $G_5 = (\text{GSH4}) (\overline{\text{CLEAR}}) (G_5)$

d) ϕ SET $G_4 = 0$

ϕ RESET $G_4 = (\text{GSH4}) (\overline{\text{CLEAR}}) (G_4 \overline{G_5})$

e) ϕ SET $G_3 = (\text{GSH16}) (\overline{\text{CLEAR}}) (\overline{G_3})$

f) ϕ SET $G_2 = (\text{GSH16}) (\overline{\text{CLEAR}}) (G_1 \overline{G_2} \overline{G_3})$

ϕ RESET $G_2 = (\text{GSH16}) (\overline{\text{CLEAR}}) (G_2 \overline{G_3})$

g) ϕ SET $G_1 = 0$

ϕ RESET $G_1 = (\text{GSH16}) (\overline{\text{CLEAR}}) (G_1 \overline{G_2} \overline{G_3})$

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GENERAL ELECTRIC COMPANY
COMPUTER EQUIPMENT DEPARTMENT
PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh.12-294 Sh. No.12-293

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

12.4.3 G-COUNTER CONTROL DURING NORMALIZE

- 1) When normalization is required during floating operations, the number of shifts required to normalize a mantissa is stored in the G-counter.

During GN the G-counter is incremented by factors of 16, 4, and 1. These increments are determined by the conditions of the NSL1, NSL4, and NSL16 detectors where

a) NSL16 = Normalize Left 16-Bit Positions
(G incremented by 16)

b) NSL4 = Normalize Left 4-Bit Positions
(G incremented by 4)

c) NSL1 = Normalize Left 1-Bit Position
(G incremented by 1)

- 2) ϕ SET/RESET G_i during normalization

a) SET G₇ = (NSL₁) ($\overline{G_7}$)

RESET G₇ = (NSL₁) (G₇)

b) SET G₆ = (NSL₁) (G₇)

RESET G₆ = 0

c) SET G₅ = (NSL₄) ($\overline{G_5}$)

RESET G₅ = (NSL₄) (G₅)

d) SET G₄ = (NSL₄) (G₅)

RESET G₄ = 0

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GENERAL ELECTRIC COMPANY
COMPUTER EQUIPMENT DEPARTMENT
PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh.12-295 Sh. No.12-294

TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR

12.4.3 - Contd

- e) $\text{SET } G_3 = (\text{NSL}_{16}) (\bar{G}_3)$
 $\text{RESET } G_3 = (\text{NSL}_{16}) (G_3)$
- f) $\phi \text{ SET } G_2 = (\text{NSL}_{16}) (\bar{G}_2 G_3)$
 $\phi \text{ RESET } G_2 = (\text{NSL}_{16}) (G_2 G_3)$
- g) $\phi \text{ SET } G_1 = (\text{NSL}_{16}) (G_2 G_3)$
 $\phi \text{ RESET } G_1 = 0$

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GENERAL ELECTRIC COMPANY
COMPUTER EQUIPMENT DEPARTMENT
PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh.12-296 Sh. No.12-295

TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR

12.4.4 G-COUNTER DATA INPUT CONTROL

12.4.4.1 General

Data input to G fall into two general categories:

- 1) Fixed count data
 - a) ES, $\overline{\text{ES}}$ /G (align)
 - b) M/G (shifts)
 - c) Number of multi-op subcycles (MPLY, DVD, etc.)
- 2) Counter control logic during shifts or aligns
 - a) Three counters-sequentially decremented by 1. (shifts or aligns)
 - b) Three counters-sequentially incremented by 1. (normalize)
 - c) One counter decremented by 1. (multi-ops)

In the case of category (1), it is desirable to have complementary data inputs to the Set/Reset inputs to each register flip-flop in order to force each flip-flop to the desired state regardless of its previous state. Counter initialization to "all 0's" can be included in category (1) (fixed count = 0). (Except when a fixed count is being inserted.)

Category (2) require separate and individually controllable Set/Reset inputs due to the register's counter function.

Conditional complementary controls for each G-counter bit is the method used to insure the counter will be forced to its proper state during fixed count insertion or when G must be cleared.

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GENERAL ELECTRIC COMPANY
COMPUTER EQUIPMENT DEPARTMENT
PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh.12-297 Sh. No.12-296

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

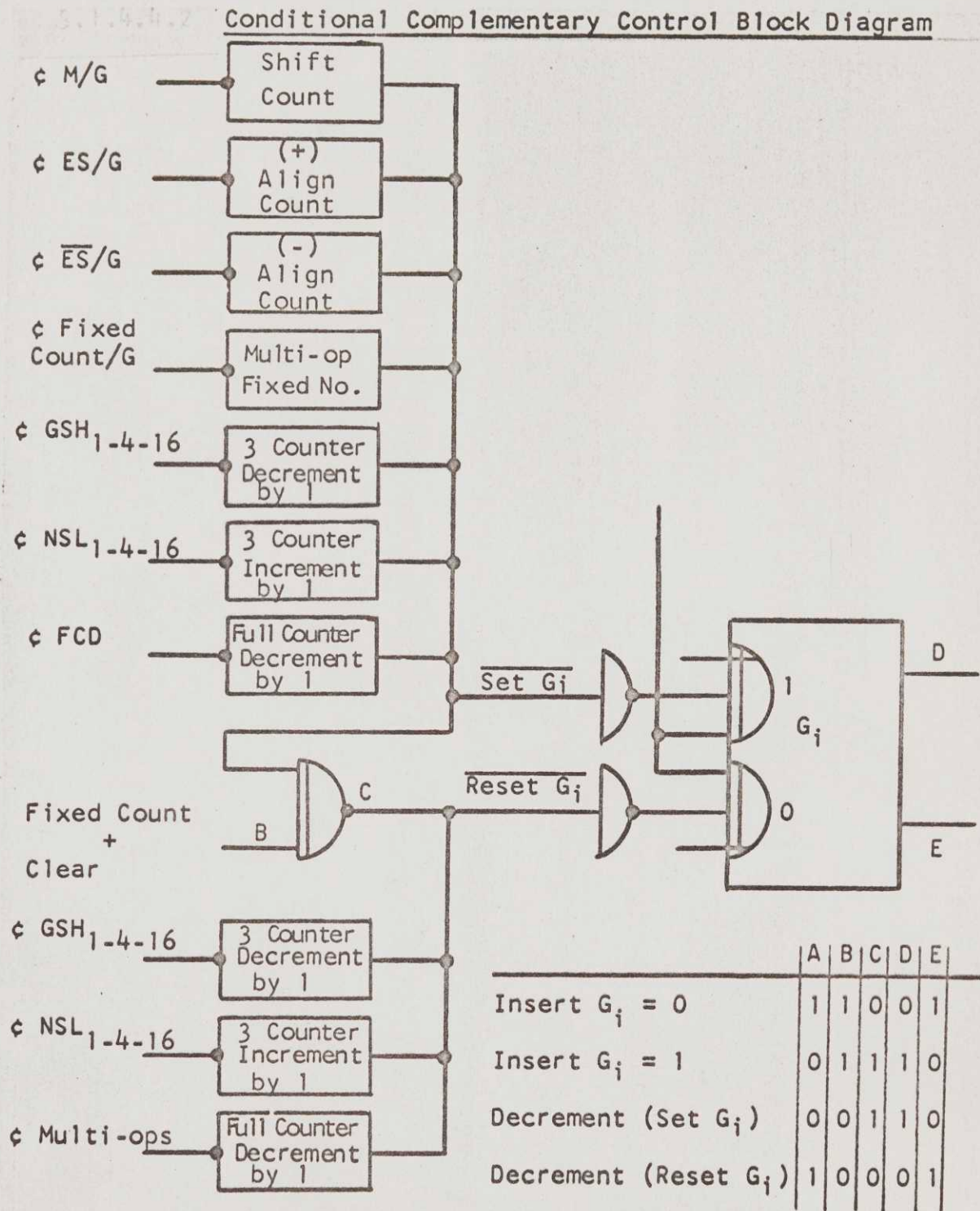


Fig. 12.4.4.1

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Spec. No. M50EE00107

Cont. on Sh. 12-298 Sh. No. 12-297

TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR

12.4.4.2

Conditional Complementary Set/Reset (CCSR) Control Requirements

Complementary Set/Reset inputs to G_{0-7} are required when:

- 1) A specific number of minor cycles is being inserted or
- 2) The counter is to be reset to zero.

The insertion of a specified count into G is required when any one of the following control points is on:

- 1) ϕ ES/G (align count for E-D = positive difference)
- 2) ϕ $\overline{\text{ES}}$ /G (align count for E-D = negative difference)
- 3) ϕ M_{11-17}/G_{1-7} (shift count)
- 4) Fixed Count/G (number of minor cycles during multiply, divide, BCD, or GTB)

The counter is to be reset to zero under the following conditions:

- 1) When the count in G during a Shift instruction or during mantissa alignment (GA) indicates 1, 3, 4, 15, or 16 shifts or alignments remain.
- 2) When $G = 1$ during multiply, divide, BCD, or GTB.
- 3) Unconditionally reset during (GS) ($\overline{\text{GE}}$) (\$) and during (GF) (\$).

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GENERAL ELECTRIC COMPANY
COMPUTER EQUIPMENT DEPARTMENT
PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh.12-299 Sh. No.12-298

TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR

12.5

REPEAT COUNTER DESCRIPTION

During any repeat operation (RPT, RPL, RPD) the OU will count the number of times the specified operation is repeated. Bits 0 through 7 of index register X0 form an 8-bit binary counter capable of counting from any number up to 255 down to 0 and on around again. During the execution of the repeat instruction itself this counter can be set to a specified number from 0 to 255, or left unaltered depending upon whether bit 10 of the repeat instruction word is a one or a zero. In either case it will be decremented each time the repeated operation is executed. This will continue until a terminate condition is met or the count reaches zero (tally runout). When a repeat operation terminates, the difference between the original count and the final count will be the number of times the operation was executed. If the original count was zero, the first operation will cause it to become all ones (255) and it will continue to count down until a terminate condition is met. Therefore, the maximum number of times an instruction can be repeated is 256.

When a repeat instruction is received from memory, it will be strobed into M₀₋₃₅, as well as into the instruction register. During GS it will be transferred to H₀₋₃₅. During GF the transfer path to X₀ will be set up, and if H₁₀ is a one, the contents of H₀₋₁₇ will be strobed into X₀₋₁₇. If the instruction is a RPT or RPL, the SENSE TERM flip-flop will be set by \$ LAST. During a RPT or RPL operation the instruction to be repeated is sent to the OU. At that time the logic to decrement X₀₋₇ will be enabled. Each time GS is reset, X₀₋₇ will be strobed decreasing the count by one. Terminate conditions will not be checked until just prior to \$ LAST of the repeated instruction. Therefore, the instruction will be executed at least once. If X₀₋₇ was initially set to all zeros (repeat 256 times) it will be decremented to all ones prior to the Tally Runout check.

COMPANY CONFIDENTIAL

GENERAL ELECTRIC COMPANY
COMPUTER EQUIPMENT DEPARTMENT
PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh. 12-300 Sh. No. 12-299

TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR

12.5 - Contd

During a RPD operation a pair of instructions will be repeated. When the first instruction is sent to the OU, the decrement logic will be enabled, however, SENSE TERM will not be set until \$ LAST of that instruction, and it will toggle every \$ LAST from then on. Therefore X00-7 will only be strobed at the end of the GS cycle for the second instruction. Likewise the check for Tally Runout is only made at the end of the second instruction. If X00-7 equals zero at \$ LAST time, TALLY RUNOUT IND will be set and c SET TRMF will be sent to the Control Unit to signal that the repeat mode termination procedure should be initiated.

COMPANY CONFIDENTIAL

GENERAL ELECTRIC COMPANY
COMPUTER EQUIPMENT DEPARTMENT
PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh.12-301 Sh. No.12-300

TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR

12.6 INTERVAL TIMER DESCRIPTION

12.6.1 GENERAL

The Interval Timer (Timer Register) is a 24-bit binary counter which provides a program interrupt at the end of a variable interval. The counter can be set to a maximum of approximately 4 minutes total elapsed time via the LDT instruction. The decrement rate is 64 kc (15.625 microseconds) and is generated from a crystal controlled oscillator in the Control Unit.

12.6.2 LDT

The Processor must be in Master mode when executing the LDT instruction in order to load the Timer Register. The execution of this instruction in the Slave mode will have no effect upon the register. The load path to the timer is from the S-adder. The condition [GF] [LDT] [Master/Slave Ind = 1] will collector trigger the timer with the specified time interval. During this duration the 64 kc strobe will have no effect. Decrementing of the time interval will commence between 0 microsecond and 15.625 microseconds after the load is completed.

12.6.3 TIMER RUNOUT

Timer Runout is anticipated by sensing the condition (TIMER = 0 — 01). This level generates a pulse (\$ TIMER = 0) which is transmitted to the Base Frame setting the Timer Runout Fault flip-flop (TROF). The timer continues to count. If the Processor is in Master mode, TROF will remain set until the Slave mode is entered at which time the fault will be recognized and the flip-flop reset. The fault is immediately recognized if the Processor is in Slave at the time of runout.

COMPANY CONFIDENTIAL

GENERAL ELECTRIC COMPANY
COMPUTER EQUIPMENT DEPARTMENT
PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh. 12-302 Sh. No. 12-301

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

12.6.4

STT -- SREG

The Timer Register is stored via the STT or SREG instructions. The store path is via the ZAQ bus onto the Data Out lines and is controlled as follows:

$\phi \text{ TIMER/ZAQ}_{0-23} = (\text{SREG})(\text{GF})(\text{GRU} = 001) + (\text{STT})(\text{GC})$

$\phi \text{ ZAQ}_{0-35}/\text{D}\phi_{0-35} = (\text{same as above})$

In order to insure that Timer Register is not in the process of trickle-down from the previous 64 kc pulse, the oscillator is turned off upon entering the STT or SREG instructions.

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GENERAL ELECTRIC COMPANY
COMPUTER EQUIPMENT DEPARTMENT
PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh.12-303 Sh. No.12-302

TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR

12.7

THE INDICATORS

The indicators may be regarded as individual bit positions in a half-word Indicator Register (IR).

An indicator is set to ON or OFF by certain events in the Processor, or by certain instructions. The ON state corresponds to a binary ONE in the respective bit position of IR; the OFF state corresponds to a ZERO.

The description of each machine instruction in EPS Section I includes a statement about the indicators that may be affected by the instruction, and the condition under which a setting of the indicators to a specific state occurs. If the conditions stated are not satisfied, the status of this indicator remains unchanged.

The Indicator instruction set comprises instructions (LDI, STI, STCI, RTD, RCU, SCU, RET) which transfer data between the lower half of a storage location and the Indicator Register. The following table lists the indicators that have been implemented and their relation to the bit positions of the lower half of a memory location.

COMPANY CONFIDENTIAL

GENERAL ELECTRIC COMPANY
COMPUTER EQUIPMENT DEPARTMENT
PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh.12-304 Sh. No.12-303

TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR

12.7 - Contd

Bit Position	Indicator
18	Zero
19	Negative
20	Carry
21	Overflow
22	Exponent Overflow
23	Exponent Underflow
24	Overflow Mask
25	Tally Run-Out
26	Parity Error
27	Parity Mask
28	Absolute Mode

29	
30	
31	Must be
32	zero
33	
34	
35	

The indicators may be divided into three basic groups as follows:

a) Program Set

Zero
Negative
Carry
Overflow
Exponent Overflow
Exponent Underflow
Tally Runout

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GENERAL ELECTRIC COMPANY
COMPUTER EQUIPMENT DEPARTMENT
PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh.12-305 Sh. No.12-304

TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR

12.7 - Contd

b) Instruction Set

Overflow Mask
Parity Mask
Absolute Mode

c) Hardware Set

Parity

The Indicators in Group A may be subdivided into two groups:

1) Fault Trip Indicators

Overflow
Exponent Overflow
Exponent Underflow

2) Non Fault Trap Indicators

Zero
Negative
Carry
Tally Runout

The Indicators are not actually contained in a register, but are interspersed as individual flip-flops throughout the Arithmetic Frame in the Processor, in close proximity to the logic associated with the setting and resetting of them. There is the exception, the Absolute Mode indicator is in the Control Frame.

The following paragraphs contain descriptions of the control of each individual indicator.

COMPANY CONFIDENTIAL

GENERAL ELECTRIC COMPANY
COMPUTER EQUIPMENT DEPARTMENT
PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh.12-308 Sh. No.12-307

TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR

12.7.5 - contd

Since it is not set "OFF" otherwise, the Exponent Overflow Indicator reports any exponent overflow that has happened since it was last set OFF by certain instructions (see LDI, RET, TEO).

12.7.6 EXPONENT UNDERFLOW INDICATOR

The Exponent Underflow Indicator is affected by floating point arithmetic operations, using the EAQ registers or the E register only. It is also affected by Floating Negate and Floating Normalize instructions. The indicator is set ON when the exponent of the result is smaller than -128 which is the lower limit of the exponent range.

Since it is not set "OFF" otherwise, the Exponent Underflow Indicator reports any exponent underflow that has happened since it was last set OFF by certain instructions (see LDI, RET, TEU).

12.7.7 OVERFLOW MASK INDICATOR

The Overflow Mask Indicator can be set ON or OFF only by the instructions LDI, RET, RTD, and RCU.

When the Overflow Mask Indicator is ON, the setting of the Overflow Indicator, Exponent Overflow Indicator, or Exponent Underflow Indicator does not cause an Overflow Fault Trap to occur. When the Overflow Mask Indicator is OFF, such a trap will occur if any one of the three Overflow Indicators is set.

Clearing of the Overflow Mask Indicator to the "unmask" state will not generate a fault from a previously set Overflow Indicator, Exponent Overflow Indicator, or Exponent Underflow Indicator. The status of the Overflow Mask Indicator does not affect the setting, testing, or storing of the Overflow Indicator, Exponent Overflow Indicator, or Exponent Underflow Indicator.

COMPANY CONFIDENTIAL

GENERAL ELECTRIC COMPANY
COMPUTER EQUIPMENT DEPARTMENT
PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh.12-306 Sh. No.12-305

TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR

12.7.1 ZERO INDICATOR

The Zero Indicator is affected by instructions that change the contents of a Processor register (A, Q, AQ, Xn, TR) or adder, and by comparison instructions.

Generally, the indicator is set ON when on completion of an instruction, the new contents of the affected register or adder contains all binary ZERO's, otherwise the indicator is set OFF. An exception to this is as follows: If, during any divide instruction it is discovered that the divisor is zero, the instruction is aborted and the zero indicator set. This indicator may be tested by TZE and TNZ instructions. The status of the indicator is not affected by these instructions.

12.7.2 NEGATIVE INDICATOR

The Negative Indicator is affected by instructions that change the contents of a Processor register, (A, Q, AQ, Xn, TR) or adder, and by comparison instructions.

Generally, the indicator is set ON when on completion of an instruction, the new contents of bit position #0 of this register or adder is a binary ONE; otherwise it is set OFF. Two exceptions to this are as follows: If any divide instruction is aborted for other than divisor equals zero, the sign indicator is set to indicate an illegal divide attempt. This indicator may be tested by the TPL, TMI instructions. The status of the indicator is not affected by these instructions. The second exception appears during the BCD instruction, during which it will be set or reset at the beginning of the operation, depending on the condition of bit #0 of the A-register.

COMPANY CONFIDENTIAL
GENERAL ELECTRIC COMPANY
COMPUTER EQUIPMENT DEPARTMENT
PHOENIX, ARIZONA

Spec. No. M50EB00107
Cont. on Sh.12-307 Sh. No.12-306

TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR

12.7.3 CARRY INDICATOR

The Carry Indicator is affected by additions, subtractions, comparisons, and left shift instructions.

Generally, the indicator is set ON when a carry is generated out of bit position #0; otherwise it is set OFF. An exception to this is that on a left shift instruction if the bits shifted through position Zero are not all the same the carry indicator will be set. This is done to note the fact that the sign has changed and must be taken into account.

The Carry Indicator may be tested by the Transfer on Carry (TRC) and Transfer No Carry (TNC) instructions. The status of the indicator is not affected by these instructions.

12.7.4 OVERFLOW INDICATOR

The Overflow Indicator is affected by arithmetic instructions, Load Complement, Floating Normalize and Negate instructions. It is not affected by shifts, add or subtract logic or And/Or instructions. If the Overflow Indicator is set during an arithmetic operation, it is due to the result of the operation being too large a number to be represented in the associated register. If the Overflow Indicator is set during a load complement or negate type instruction, it is a result of the operand being maximally negative (10—0). The indicator may be tested by the TOV instruction, and will be reset as a result of the operation.

12.7.5 EXPONENT OVERFLOW INDICATOR

The Exponent Overflow Indicator is affected by floating point arithmetic operations, using the EAQ registers or the E register only. It is also affected by floating normalize and floating negate instructions. The indicator is set ON when the exponent of the result is larger than +127 which is the upper limit of the exponent range.

COMPANY CONFIDENTIAL

GENERAL ELECTRIC COMPANY
COMPUTER EQUIPMENT DEPARTMENT
PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh.12-309 Sh. No. 12-308

TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR

12.7.8 TALLY RUNOUT INDICATOR

The Tally Runout Indicator is affected by the repeat instructions (RPT, RPD, RPL), and instructions using IT modification for all tally designators except I and F. If the Tally Runout Indicator is set on completion of a Repeat Type instruction this indicates the repeat sequence was terminated due to a tally count of zero. There is an exception to this; note that in the case of an RPL instruction, a link address of zero also sets the Tally Runout Indicator. If the indicator is off on completion of a repeat type instruction, this means the sequence was terminated due to a specified terminate condition being met. The indicator will also be set if the tally goes to zero during an instruction using IT modification. In this case, the indicator will not be set until the tally modified instruction has been executed. The reason for this is to prevent a transfer of Tally Runout Indicator Off instruction with an IT modification from transferring due to tally runout caused by the instruction itself. This indicator may be tested by the transfer on Tally Runout Indicator Off Instruction. The status of the indicator is not changed by the instruction.

12.7.9 PARITY ERROR INDICATOR

The Parity Error Indicator is set if a parity error is detected by memory under the following conditions:

- a) If a parity error is detected in either word during an instruction Fetch of Y pair.
- b) If a parity error is detected in either word of a double precision operand Fetch.

COMPANY CONFIDENTIAL

GENERAL ELECTRIC COMPANY
COMPUTER EQUIPMENT DEPARTMENT
PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh.12-310 Sh. No.12-309

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

12.7.9 - contd

- c) During a Single Precision Operand Fetch the memory actually pulls two words. If the address (Y) is odd, C(Y) and C(Y-1) are pulled. If the address is even C(Y) and C(Y+1) are pulled. The Processor is only notified i.e. Parity Indicator is set only if the parity error occurs in the C(Y). Contents of Y-1 or Y+1 are not reported to the Processor.

This indicator may be reset by the LDI, RCU, RTD, or RET instructions.

12.7.10 PARITY MASK INDICATOR

The Parity Mask Indicator can be set ON or OFF only by the instructions LDI, RET, RTD, and RCU.

When the Parity Mask Indicator is ON, the setting of the Parity Error Indicator does not cause a Parity Error Fault Trap to occur. When the Parity Mask Indicator is OFF, such a trap will occur if the Parity Error Indicator is set.

Clearing of the Parity Mask Indicator to the "unmask" state will not generate a fault from a previously set Parity Error Indicator. The status of the Parity Mask Indicator does not affect the setting, or storing of the Parity Error Indicator.

12.7.11 ABSOLUTE MODE INDICATOR

The Processor is always in Absolute Mode when this indicator is on. The Processor is in non-Absolute Mode when this indicator is off except for that time during which the Processor is performing an Execute Double as a result of a fault.

COMPANY CONFIDENTIAL

GENERAL ELECTRIC COMPANY
COMPUTER EQUIPMENT DEPARTMENT
PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh.12-311 Sh. No.12-310

TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR

12.7.11 - contd

The Absolute Mode indicator is set if one of the instructions executed during a fault forced XED is any transfer instruction except TSS that causes a transfer of control. It can also be set by a RET or RTD instruction if the Processor is in Master Mode and bit 28 of the operand is a "1". It can also be set by a RCU instruction if bit 28 of Y+3 is a "1".

The Absolute Mode indicator is reset by the execution of a TSS instruction. It can also be reset by any transfer instruction that causes a transfer of control if bit 29 of the instruction word is a "1". It can also be reset by a RET, RTD, or RCU instruction if bit 28 is a "0".

COMPANY CONFIDENTIAL

GENERAL ELECTRIC COMPANY
COMPUTER EQUIPMENT DEPARTMENT
PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh.12-312 Sh. No.12-311

TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR

12.8 SPECIAL CONTROL FLIP-FLOPS

12.8.1 ABORT - ABORT CYCLE

The ABORT flip-flop causes the OU to stop all operations and to reset all essential control flip-flops. An abort sequence can be started by any operation of the OU that will cause a fault, the termination of a repeated operation, or a fault sequence initiated by the CF.

$$\text{ABORT (set)} = (\$ \text{ SET ABORT})_{\text{CF}} + (\$ \text{ SET DVCK}) + (\$ \text{ SET OVFL FLT}) + (\$ \text{ SET TRMF})(\$ \text{ LAST})$$

$$\text{ABORT (reset)} = (\$ \text{ RESET ABORT})_{\text{CF}}$$

12.8.2 BCFF₁ - BYTE CONTROL

BCFF₁ when set, tells the OU that the current instruction has an IT modifier of CI or SC. It is used in conjunction with BMFF to enable the decode of the Byte Position Register to pick up the proper ZAQ/ZDO (that is, ZAQ₃₀₋₃₅/ZDO₁₈₋₂₃, etc.). When the CU detects an instruction calling for IT character modification it sends a pulse (\$BPR) to the OU. This pulse strobes the character position into the Byte Position Register and sets BCFF. The OU will send or receive the proper character. BCFF will be reset at the end of the OU operation.

$$\text{BCFF}_1 \text{ (set)} = \$ \text{ BPR}$$

$$\text{BCFF}_1 \text{ (reset)} = \$ (\text{GF}) + (\text{ABORT})$$

COMPANY CONFIDENTIAL

GENERAL ELECTRIC COMPANY
COMPUTER EQUIPMENT DEPARTMENT
PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh.12-313 Sh. No.12-312

TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR

12.8.3

BCFF₂

BCFF₂ when set, tells the QU that the current instruction has an IT modifier of CI or SC, and it is of the nonstore type. It is used in conjunction with BMFF to enable the decode of the Byte Position Register to enable the proper control logic on the ZDI/M switches (that is, ZDI₀₋₈/M₂₇₋₃₅, ZDI₁₈₋₂₃/M₃₀₋₃₅, etc.). When the CU detects an instruction calling for IT character modification it sends a pulse (\$BPR) to the QU. This pulse strobes the character position into the Byte Position Register and sets BCFF₂ if the instruction is a nonstore. The QU will receive the proper character.

BCFF₂ (set) = \$BPR ($\overline{\text{STORES}}$)

BCFF₂ (reset) = \$(GS)($\overline{\text{GF}}$) + (ABORT)_{CF}

COMPANY CONFIDENTIAL

GENERAL ELECTRIC COMPANY
COMPUTER EQUIPMENT DEPARTMENT
PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh.12-314 Sh. No.12-313

TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR

12.8.4 BMFF - BYTE MODE

BMFF is only meaningful when BCFF is set. It is used to designate whether the character is 6-bit or 9-bit. If the indirect word from memory signifies a 9-bit character by having a 1 in bit 30, BMFF will be set by \$BPR. If bit 30 of the indirect word is a 0, indicating a 6-bit character, BMFF will remain reset. BMFF is reset at the end of the operation.

BMFF (set) = (ZDI₃₀) (\$BPR)

BMFF (reset) = \$(GF)

12.8.5 CMFF - COMPARE MAGNITUDE

During a fixed-point divide operation the absolute value of the dividend is compared against the absolute value of the divisor, and if it is equal to or greater than the divisor a Divide Check Fault occurs. This comparison is made during the first GO cycle. CMFF defines this cycle. It will be set for one cycle only.

CMFF (set) = (GD₂) ($\overline{\text{BCD}}$) (\$)

CMFF (reset) = (Fixed-Point Divide) (\$)

COMPANY CONFIDENTIAL

GENERAL ELECTRIC COMPANY
COMPUTER EQUIPMENT DEPARTMENT
PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh.12-315 Sh. No.12-314

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

12.8.5 - contd

During a floating-point divide the absolute value of the dividend mantissa is compared against the absolute value of the divisor mantissa, and if it is equal to or greater than the divisor it will be shifted right and exponent incremented until it is smaller. The comparison and correction are done in the first GO cycle. However, each shift requires a complete cycle, therefore, the G-counter must be prevented from counting until the OU is ready to start the second GO cycle. Again CMFF set defines this period and prevents the decrementing of the G-counter. On the cycle that the dividend becomes less than the divisor CMFF will reset and the G-counter will be decremented.

$$\text{CMFF (set)} = (\text{GD}_2) (\overline{\text{BCD}}) (\$)$$
$$\text{CMFF (reset)} = (\text{Floating-Point Divides}) (\text{SC}_0) (\$)$$

12.8.6

DDF - DECODE DELAY FLAG

DDF is part of the control for \$ START. In order to generate a \$ START the OU must have had time to decode the op code in the O-register, the operand must be ready, and the previous instruction must be completed. DDF set indicates that the decode lines are stabilized. It is set for a sufficient duration after the receipt of the op code to insure this. It is reset by \$ START.

$$\text{DDF (set)} = (\$ \text{ Set GS})_{\Delta}$$
$$\text{DDF (reset)} = (\$ \text{ START})$$

COMPANY CONFIDENTIAL

GENERAL ELECTRIC COMPANY
COMPUTER EQUIPMENT DEPARTMENT
PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh.12-316 Sh. No.12-315

TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR

12.8.7 DIC - DATA INHIBIT CONTROL

During any multiply operation the M-register is an active register. Therefore, it must be protected against spurious data on its inputs. Since there may be spurious data on the ZDI lines, the ZDI to M control lines must be turned off. This is accomplished with the DIC flip-flop. It will be set when an operand is received for a multiply operation and will be reset when that operation no longer requires the use of the M-register. DIC set will inhibit all ZDI to M control lines except those used for CI or SC operations. It is not necessary to inhibit the lines used for CI and SC because an IT modification cannot start until all operations have been completed, therefore these lines cannot be active during a multiply operation.

DIC (set) = (MPLY)_{ZOR} (\$YRY)

DIC (reset) = (G = 3)

12.8.8 DPFF - DOUBLE-PRECISION

During double-precision load type operations the M-register in the OU will receive two 36-bit words from memory. The DPFF flip-flop is one of the controls for the Data In lines and for the M-register Strobe. When set it will enable the ZDI/M control lines for the second half of a double-precision word and the proper \$M pulses. When reset it will enable the ZDI/M control lines for the first half of a double-precision word or for a single-precision word and the proper \$M pulses. It will be set upon receipt of the first half of a double-precision word and reset upon receipt of the second half of a double-precision word.

DPFF (set) = ($\overline{\text{DPFF}}$) (Double-Precision Ops) (\$DRDY)

DPFF (reset) = ($\overline{\text{Set DPFF}}$) (\$DRDY)

COMPANY CONFIDENTIAL

GENERAL ELECTRIC COMPANY
COMPUTER EQUIPMENT DEPARTMENT
PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh.12-317 Sh. No.12-316

TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR

12.8.9

DUMF - DIRECT MODIFIER

During a multiply operation the number of GO cycles to be executed is determined by the number of bits in the multiplier and the type of multiplication being done. If a Direct Upper modifier is called for, the multiplier is premultiplied by 18 for single-precision multiplies. Consequently, the count inserted into the G-counter must be decreased proportionally. This is accomplished by DUMF. During any floating-point multiply DUMF set results in a count of 6 being inserted into the G-counter rather than a count of 15. During any fixed-point multiply DUMF set results in a count of 10 being inserted into the G-counter rather than 19. DUMF will be set by a Direct Upper signal from the CU and reset upon completion of the first cycle of the operation. DUMF will be set during any instruction that calls for a Direct Upper modifier, however, it will have no effect except on multiply instructions.

$$\text{DUMF (set)} = (\$ \text{DUMF})_{\text{CU}}$$
$$\text{DUMF (reset)} = (\text{GS})(\overline{\text{GF}}) (\text{DUMF}) (\$)$$

COMPANY CONFIDENTIAL

GENERAL ELECTRIC COMPANY
COMPUTER EQUIPMENT DEPARTMENT
PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh.12-318 Sh. No.12-317

TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR

12.8.10 EIFF - EXPONENT INCREMENT

During any divide operation the absolute value of the dividend in the N-register is compared against the absolute value of the divisor in the H-register by adding them together in the S adder. During the compare magnitude (CMFF) cycle, a carry out of the adder (SC_0) indicates that the dividend is equal to or greater than the divisor. If this is the case, a divide cannot take place. In fixed-point the divide will be aborted, but in floating-point the dividend mantissa in N can be shifted right until the absolute value is less than the divisor mantissa thus permitting the divide to take place. When this is required the exponent in the E-register must be incremented by one for each place the dividend is shifted to maintain the true value of the dividend. The incrementing of E is under control of EIFF.

During a floating-point divide the first CMFF cycle will add N and H. If N is equal to or greater than H a carry out of adder bit zero (SC_0) will result. SC_0 will prevent CMFF resetting, will set EIFF, and will shift N one bit position right. On the next CMFF cycle N and H will be added again and EIFF set will gate the E-register to the ES adder, will gate a +1 to the ES adder, and will strobe the result back into E. If SC_0 is false, CMFF and EIFF will reset and N will not be shifted. At this point the divide operation will commence.

During a fixed-point divide a CMFF cycle will add N and H. If N is equal to or greater than H, SC_0 will come true. EIFF will set, but the divide operation will abort and EIFF will be reset by ABORT.

$$\text{EIFF (set)} = (\text{CMFF}) (\text{SC}_0) (\$)$$

$$\text{EIFF (reset)} = (\text{CMFF}) (\overline{\text{SC}_0}) (\$) + (\text{ABORT})_{\text{CT}}$$

COMPANY CONFIDENTIAL

GENERAL ELECTRIC COMPANY
COMPUTER EQUIPMENT DEPARTMENT
PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh. 12-319 Sh. No. 12-318

TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR

12.8.11 FRD - REPEAT DOUBLE

If the CU is in the Repeat Double mode of operation FRD in the OU will set. FRD set will allow SENSE TERM to toggle every OU operation so that it will allow the detection of terminate conditions only on the odd instruction. It will enable the set of TALLY RUNOUT IND. If X0₁₇ is a zero it will prevent the detection of an overflow. (See GE-645 EPS, Section I for details on terminate conditions for a RPD instruction.) FRD will be reset upon completion of the Repeat Double Mode of Operation.

FRD (set) = (RPD) (\$ LAST)

FRD (reset) = (TRMF) (\$ LAST)

12.8.12 FTL - REPEAT/REPEAT LINK

If the CU is in the Repeat or Repeat Link mode of operation FTL in the OU will set. FTL set will accomplish the same function as FRD except that SENSE TERM will set and stay set for the entire operation.

FTL (set) = (RPT + RPL) (\$ LAST)

FTL (reset) = (TRMF) (\$ LAST)

COMPANY CONFIDENTIAL

GENERAL ELECTRIC COMPANY
COMPUTER EQUIPMENT DEPARTMENT
PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh.12-320 Sh. No.12-319

TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR

12.8.13 GRU3, GRU2, GRU1

The G-counter is physically located in the arithmetic frame. In order to speed up the decode of various G-counts in the RF a 3-bit Shift Register is employed (GRU₃ GRU₂, GRU₁). In any multiple GO cycle operation except shifts, GRU₃ will be set when the G-counter is stepped from 4 to 3. Each succeeding \$ pulse will shift the bit down one until the counter is cleared. These three flip-flops are used to decode the various G counts required by the register frame. This counter also is used by the Load Registers and Store Registers operations. It will determine which registers are to be loaded or stored during each sequence. The counter will be stepped at the end of each GF cycle. It will count as follows:

GRU ₃	GRU ₂	GRU ₁	
0	0	0	load or store X0, X1, X2, and X3
1	0	0	load or store X4, X5, X6, and X7
0	1	0	load or store AQ
0	0	1	load or store E and Binary

$$\text{GRU}_3 (\text{set}) = [(\text{GO}) (\overline{\text{Shifts}}) (\text{G}=4) + (\text{GF}) (\text{LREG} + \text{SREG})] [\text{\$GRU}]$$

$$\text{GRU}_3 (\text{reset}) = (\text{GRU}_3)_{\Delta} (\text{\$GRU})$$

$$\text{GRU}_2 (\text{set}) = (\text{GRU}_3)_{\Delta} (\text{\$GRU})$$

$$\text{GRU}_2 (\text{reset}) = (\text{GRU}_2)_{\Delta} (\text{\$GRU})$$

$$\text{GRU}_1 (\text{set}) = (\text{GRU}_2)_{\Delta} (\text{\$GRU})$$

$$\text{GRU}_1 (\text{reset}) = (\text{GRU}_1)_{\Delta} (\text{\$GRU})$$

$$\text{\$GRU} = [(\text{GF}) (\text{LREG} + \text{SREG})] \$$$

COMPANY CONFIDENTIAL

GENERAL ELECTRIC COMPANY
COMPUTER EQUIPMENT DEPARTMENT
PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh.12-321 Sh. No. 12-320

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

12.8.14

H_{72}

During all multiply operations the partial product is formed in the S-adder and shifted two places right when stored back in H (that is, S_{0-70} to H_{2-72}). Normally it is not necessary to remember what was shifted one place left and stored in N (that is, H_{1-72} to N_{0-71}). H_{72} holds the bit shifted from S_{70} for later insertion into N_{71} .

$$H_{72} \text{ (set)} = (S_{70}) (\$)$$

$$H_{72} \text{ (reset)} = (\overline{S_{70}}) (\$)$$

12.8.15

LAFF - LOGICAL ALIGN

During a floating-point subtract, compare, or compare magnitude instruction a peculiar problem can occur. Normally the mantissa alignment is accomplished by arithmetic right shifts. However, if the mantissa in memory is a maximum negative number (that is, sign bit a 1 and all other bits a 0) when it is ones complemented and stored in H the sign bit will be a 0 and all other bits a 1. If this mantissa is chosen to be aligned, because its exponent is less positive than the other exponent, it will be routed through the S-adder to N. K_{72} will be on converting the ones complement to a twos complement. This will result in the mantissa in N having sign bit A 1 and all other bits a 0 (that is, a maximum negative number). N therefore now contains a mantissa which overflowed when twos complemented. However, when the twos complement was formed in the S-adder this detected overflow condition set LAFF. LAFF is in the N shift control logic and in the decrement G-counter logic. It will cause the first shift of N to be a logical right shift of one place making N sign bit a zero, N bit one a 1 and all other bits a 0. Thus, the overflowed mantissa is corrected, the G-counter is decremented by one, and the align cycle(s) continue with normal arithmetic shifts.

$$\text{LAFF (set)} = (\text{GE}) (\text{OFL}) (\overline{\text{ES}}_9) (\$)$$

$$\text{LAFF (reset)} = [(\overline{\text{GE}}) + (\overline{\text{OFL}})] (\$)$$

COMPANY CONFIDENTIAL

GENERAL ELECTRIC COMPANY
COMPUTER EQUIPMENT DEPARTMENT
PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh.12-322 Sh. No.12-321

TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR

12.8.16 LAST

During a Repeat operation an instruction or a pair of instructions will be repeated until the specified terminate conditions have been met. If indicators such as zero or sign are checked before the operation is complete, erroneous terminates could occur. LAST insures that terminate conditions will only be tested between the end of GF and \$ LAST. LAST and SENSE TERM enable ϕ SET TRMF.

LAST (set) = (GF) (\$)

LAST (reset) = \$ LAST

12.8.17 N-1

Shift logic allows shifting N either direction in increments of 1, 4, or 16 bits. To speed up shifting it is permissible to overshift by one and then reverse shift by one. Any left shift whether program or normalization can result in this overshift. In order to prevent losing a bit an extra flip-flop (N-1) holds the overshifted bit. It will be shifted back into N₀ on the reverse shift.

N-1 (set) = [(N₃) (GSH4) + (N₁₅) (GSH16)] (\$)

N-1 (reset) = [(\overline{N₃}) (GSH4) + (\overline{N₁₅}) (GSH16)] (\$)

COMPANY CONFIDENTIAL

GENERAL ELECTRIC COMPANY
COMPUTER EQUIPMENT DEPARTMENT
PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh. 12-323 Sh. No. 12-322

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

12.8.18 N36A

Any type of single-precision right shift can result in an overshift and reverse shift. It is possible to shift from the upper half of N into the lower half of N to prevent loss of information. However, this nullifies the zero detection. An additional flip-flop N36A handles this situation. N36A will hold the last bit shifted out of the upper portion of N and N36-71 will remain all zeros. If an overshift occurred a reverse shift of one is required. The content of N36A will be shifted into N35.

$$N36A \text{ (set)} = [(N_{20}) (GSH_{16}) + (N_{32}) (GSH_4)] \$$$

$$N36A \text{ (reset)} = [\overline{\phi \text{ Set } N36A}] \$$$

12.8.19 N72

Any right shift, whether program or alignment, can result in an overshift and reverse shift. In order to prevent losing the Overshifted bit an Extended N-register Flip-flop (N72) holds the overshifted bit for reinsertion into N71 on the reverse shift.

$$N72 \text{ (set)} = [(N_{68}) (GSH_4) + (N_{56}) (GSH_{16})] (\$)$$

$$N72 \text{ (reset)} = [(\overline{N_{68}}) (GSH_4) + (\overline{N_{56}}) (GSH_{16})] (\$)$$

COMPANY CONFIDENTIAL

GENERAL ELECTRIC COMPANY
COMPUTER EQUIPMENT DEPARTMENT
PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh.12-324 Sh. No.12-323

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

12.8.20 ORBF - OPERATION REGISTER BUSY

When an operation code is received in the OU it will be stored in the O-register. The decode for the GS cycle originates from the O-register. At the end of GS the op code (which is now contained in the C-register) will originate from the C-register, freeing the O-register for a new operation code. ORB defines that period of time when the O-register contains a valid op code. It is used to prevent the strobing of O and it enables the \$ SET GS logic. It will be set when an op code is strobed into the O-register and reset at the end of the GS cycle for that op code.

ORBF (set) = \$OR

ORBF (reset) = (GS) ($\overline{GF}$) (\$)

12.8.21 ORYF - OPERATION DESIGNATOR READY

When the CU has an operation code ready for the OU it sends a pulse (\$ORY) notifying the OU of that fact. This pulse will set ORYF, which will remember that an op code is on the ZOR lines. When the O-register becomes free ($\overline{ORB}=1$), the condition ($\overline{ORB}$) (ORY) will generate a \$OR pulse, which will strobe the new op code into the O-register, set ORBF, and reset ORYF.

ORYF (set) = (\$ORY)

ORYF (reset) = (\$OR)

COMPANY CONFIDENTIAL

GENERAL ELECTRIC COMPANY
COMPUTER EQUIPMENT DEPARTMENT
PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh.12-325 Sh. No.12-324

TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR

12.8.22 OUBF - OPERATION UNIT BUSY

The setting of GS is dependent upon the condition of the OU. If the OU is not busy all that is required is the receipt of an op code. If the OU is busy then the setting of GS must wait until the GF cycle of the current operation or in some cases until the GF cycle has been completed. OUBF, when set, indicates that the OU is performing operations and it prevents ORBF, which is set by the receipt of an op code, from generating a \$ SET GS. When OUBF is reset the condition (OUB) (ORB) will result in a \$ SET GS. OUBF is set by \$ START and will stay set as long as the OU is processing an instruction(s).

OUBF (set) = (\$ START)

OUBF (reset) = (GF) ($\overline{\text{GS}}$) (\$)

12.8.23 PASS AND PPS

During a GO cycle of a multiply operation the multiplier in AQ is added to or subtracted from the partial product in H. The result (new partial product) is shifted two places right and stored back into H₂ - H₇₁. This would normally result in H₀ and H₁ being cleared to zero. There are conditions where either or both H₀ and H₁ must be set to one. Two flip-flops (PASS and PPS) are used to detect these conditions. Whenever the effective multiplier is zero or four the pass flip-flop is set.

PASS (set) = {[(MPLY)] [GS + GO(G>2)]

$\overline{M_{62}} \overline{M_{63}} \overline{\text{STFF}} + M_{62} M_{63} \text{STFF}$] \$

PASS (reset) + [$\overline{c}$ (PASS) set] \$

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Spec. No. M50EB00107

Cont. on Sh.12-326 Sh. No.12-325

TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR

12.8.23 - contd

Due to the fact that the partial product in H is always shifted two places to the right its absolute value is always less than that of the multiplicand. Therefore the partial product sign will always be the same as the sign of the multiplicand if an add takes place and opposite if a subtract takes place. PPS indicates the sign of the partial product.

$$\text{PPS (set)} = [(\text{Sign of Icand}) (\text{ADD}) + \\ (\overline{(\text{Sign of Icand})}) (\text{Sub})] \$$$

$$\text{PPS (reset)} = [(\overline{(\text{Sign of Icand})}) (\text{ADD}) + \\ (\text{Sign of Icand}) (\text{Sub})] \$$$

The effect of these two flip-flops will be as follows:

- a) If PASS is set, H_0 and H_1 will be set if the partial product is negative or H_0 and H_1 will be reset if the partial product is positive.
- b) If PPS is set, H_0 will always be set.
- c) If PPS is set and the current partial product is positive, H_1 will be set in the new partial product.
- d) If a carry out of the S adder occurs, H_1 will be set regardless of whether PPS is set or reset.
- e) In all other cases H_0 and H_1 will be reset.

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Spec. No. M50EB00107

Cont. on Sh.12-327 Sh. No.12-326

TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR

12.8.24 QSF - QUOTIENT SIGN

During the GO cycles of a divide operation the OU will always add a negative divisor to a positive dividend producing a positive quotient. However, if the signs of the original divisor and dividend were different the quotient should be negative. During the first set up cycle of a divide (GD_1) the signs of the divisor and dividend are compared, if they are different QSF will set and remain set until the next operation resets it. During the next to last GO cycle of a divide the accumulated positive quotient in AQ is transferred to N. If QSF is reset, indicating that the quotient should be positive, a straight transfer will take place. If QSF is set, indicating that the quotient should be negative, the ones complement will be transferred to N and K_{72} will be set to change it to a twos complement on the next cycle.

$$\begin{aligned} \text{QSF (set)} &= (GD_1) [(M_0 \overline{A_0} + \overline{M_0} A_0) (DVF + FDV \\ &\quad + DFDV + FDI + DFDI) + (M_0 \overline{Q_0} \\ &\quad + \overline{M_0} Q_0) (DIV)] \$ \end{aligned}$$

$$\text{QSF (reset)} = (GS) \$ + \text{ABORT}$$

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PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh.12-328 Sh. No.12-327

TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR

12.8.25

REV - REVERSE

During any operation that requires shifting N, such as alignment, normalization, or programmed shift, it is possible to overshift by one bit. When this happens a reverse shift of one place is required. On any shift cycle resulting in an overshift REV will set. REV being set dictates that the next movement of N will be one bit position in the direction opposite to the movement which resulted in the overshift.

$$\begin{aligned} \text{REV (set)} &= \{(\text{GN}) [(\text{N DET 4B}) (\text{N4}) + (\text{N DET 4A}) \\ &\quad (\overline{\text{N4}}) + (\text{N DET 16B}) (\text{N16}) + \\ &\quad (\text{N DET 16A})(\overline{\text{N16}})] + [\text{GA}+\text{GO}(\text{SHIFTS})] \\ &\quad [(\text{G}=\underline{+3}) + (\text{G}=\underline{+15})] + (\text{GO})(\text{OFL}) [(\text{FAD}) \\ &\quad + (\text{DFAD}) + (\text{FSB}) + (\text{DFSB}) + (\text{FNO}) \\ &\quad + \text{FNEG})] + [\text{GO}) \\ &\quad (\text{G}=1)(\text{S}_0 \oplus \text{S}_1) (\text{Flt}_{\text{ng}} \cdot \text{Mplys}] + (\text{GO}) (\text{OFLI}) \\ &\quad (\text{FNO})\} \$ \end{aligned}$$

$$\text{REV (reset)} = (\text{REV})_{\Delta} \$$$

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PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh.12-329 Sh. No.12-328

TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR

12.8.26 SDY₁ and SDY₂ - STORE READY

During store operations the OU generates a \$SDY to inform the CU that the operand will be ready for storage by the time memory will be ready for it. SDY₁ will be set when a store instruction, other than a slow store, is strobed into the O-register and it will generate a \$DSY upon completion of the preceding operation. SDY₂ will be set when a slow store instruction is strobed into the O-register and will allow (GS) ($\overline{GF}$) \$ to generate a \$DSY.

SDY₁ (set) = (Slow Stores) (\$OR)

SDY₁ (reset) = ($\overline{\text{Slow Stores}}$) (\$OR)

SDY₂ (set) = [(Fast Store)+(DP Store)+(RAR)](\$OR)

SDY₂ (reset) = [$\overline{[(Fast Store)+(DP Store)+(RAR)]}$](\$OR)

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PHOENIX, ARIZONA

Cont. on Sh. 12-330 Sh. No. 12-329

12.8.27 SENSE TERM

- a) Enable the reset logic for FTL and FRD.
- b) Enable the set logic for TALLY RUNOUT IND.
- c) Inhibit the generation of \$SDY on store instructions if the terminate conditions have been met.
- d) Enable the XO-register Repeat Counter Control logic.

SENSE TERM (reset) = (FRD + TRMF) (STR) (\$ LAST)

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COMPUTER EQUIPMENT DEPARTMENT
PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh.12-331 Sh. No.12-330

TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR

12.8.28

STFF - STRING

During multiply operations the multiplier is looked at two bits at a time (M_{62} M_{63}) to form an effective multiplier for that cycle. This means that the effective multiplier can be 0, 1, 2, or 3. The OU can handle multipliers of 0, 1, or 2 directly, however, an effective multiplier of 3 requires subtracting the multiplicand from the partial product once and adding it four times. The adding four times is accomplished by increasing the next effective multiplier pair by one. This means that it is possible to have an effective multiplier of 0, 1, 2, 3, or 4. An effective multiplier of 4 is handled by making this effective multiplier act like a 0 multiplier and adding one to the next effective multiplier pair. The fact that one must be added to the next effective multiplier is remembered by the STFF flip-flop. It is used along with M_{62} M_{63} in the decoding of the functions to be performed during the GO cycles of a multiply instruction. STFF will be set whenever the effective multiplier is a 3 or a 4.

STFF (set) = {(Multiply)[GS + (GO) (G>3)]}

 {(M₆₂) (M₆₃) ($\overline{\text{STFF}}$) + ($\overline{M_{62}}$)

 (M₆₃) (STFF)} \$

STFF (reset) = {Multiply} {[GS + GO (G>3)]

 [($\overline{M_{62}}$) ($\overline{M_{63}}$)

 ($\overline{\text{STFF}}$) + ($\overline{M_{62}}$) (M₆₃) (STFF) + (M₆₂)

 ($\overline{M_{63}}$) ($\overline{\text{STFF}}$)] + (GO) (G = 3)} \$

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PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh. 12-332 Sh. No. 12-331

TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR

12.8.29 YRY - OPERAND READY

One of the criteria for the generation of \$ START is that the operand will be ready by the time it is required. YRY will be set when this criterion is met. If the operation is a load type, YRY will be set by \$YRY, which is generated by a pulse from the CU when the operand is available. If it is a double-precision load, YRY will not set until the second half of the operand is available. Since the operand is immediately available for a store type operation YRY can be set shortly after the GS cycle is started.

$$\begin{aligned} \text{YRY (set)} &= \$YRY \\ &= (\$DRDY) (\overline{\$ \text{ SET DPFF}}) + (\$ \text{ SET DDF}) \\ &\quad (\text{Stores}) \end{aligned}$$

$$\text{YRY (reset)} = (\$ \text{ START})$$

12.9 LAST OF 2, 3 OR n PULSE DETECTOR

In an asynchronous environment it is sometimes necessary to generate a pulse conditioned on more than one variable. The technique described below is used in the GE-645 for producing the strobes, \$ ØR (places the operation code in the Ø-register and sets ØRB flip-flop), \$ START (starts the timing pulse generator and the ØU operation), and \$SDY (Store data ready).

The last pulse detector is to produce a pulse at the time the last of pulses A, B, C, ... n has set or reset a specified flag. This is advised by anding flags A, B, ..., n. At the time the last input to the AND gate (See fig. 12.9) achieves a "1" state the output goes to "0". This drop in voltage causes the pulse amplifier to generate a positive pulse. In order to generate a new pulse, one of the flags A, B, C, ..., n must change to the opposite state through a set or reset pulse. This causes the output to rise to "1". The detector is now ready to generate a new pulse.

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Spec. No. M50EB00107

Cont. on Sh.12-333 Sh. No.12-332

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

12.9 - contd

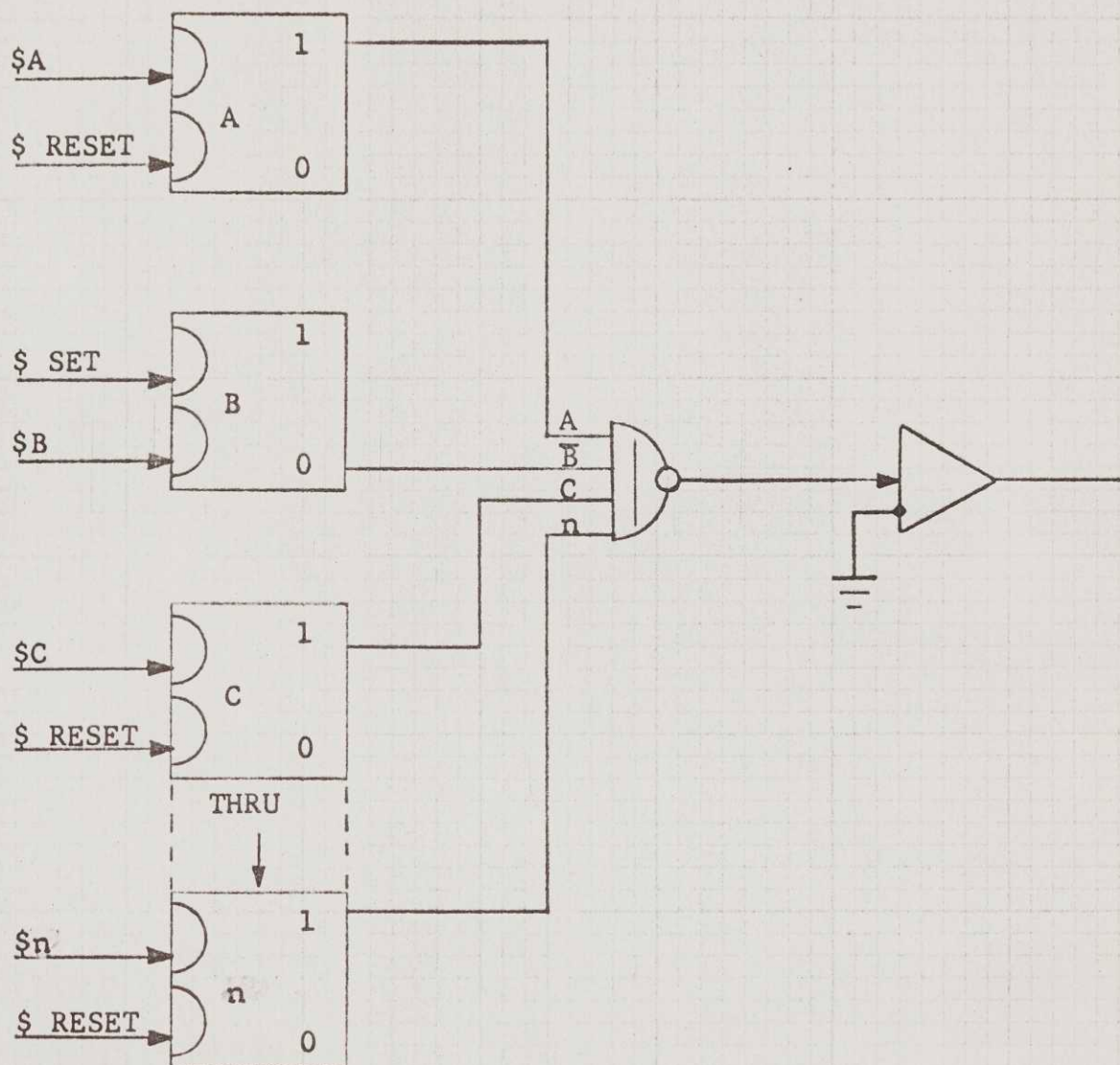


Fig. 12.9

Last of 2, 3 or n Pulse Detector, Logic Diagram

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COMPUTER EQUIPMENT DEPARTMENT
PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh.12-334 Sh. No.12-333

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

12.10 "S" ADDER

12.10.1 GENERAL

The Operations Unit S Adder is a two's complement parallel binary adder which forms the sum of two 72-bit operands contained in the holding registers N0-71 and H0-71. Functionally the adder consists of 12 parallel channels each of which processes corresponding 6-bit bytes of the 72-bit operands held in the N- and H-registers. Each channel processes its assigned operand bytes simultaneously with all other channels so that any given byte resultant sum is available at the adder output at the same time as any other byte independent of its position in the 72-bit word. That is, the most significant byte sum (S0-5) will be available at the output of channel 1 at the same time as S6-11 out of channel 2, S12-17 out of channel 3, etc.

The S Adder may be used to perform the functions of algebraic addition, inclusive OR, exclusive OR, or the logical product (AND) of the two operands contained in N and H. The operation to be performed is controlled by a 3-bit adder command register designated as the K-register. In addition a flip-flop K72 is used to add a one to the least significant bit of the adder. The adder command codes are:

K ₁	K ₂	K ₃	
0	0	0	H ₀₋₇₁ + N ₀₋₇₁
1	1	d	H ₀₋₇₁ V N ₀₋₇₁
1	0	0	H ₀₋₇₁ (V) N ₀₋₇₁
1	0	1	H ₀₋₇₁ . N ₀₋₇₁

where "+" means arithmetic summation, "V" means inclusive OR summation, "(V)" means exclusive OR summation, and "." means logical product (AND). Subtraction is performed by placing the logical complement of the subtrahend in H or N, setting K72, and adding.

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PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh.12-335 Sh. No.12-334

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

12.10.1 - contd

A functional block diagram of the S Adder is shown in Fig. 12.10.1. Each channel (except 11 and 12) consists of five functional blocks of logic, four of which are implemented as modules each on a single logic card. The five functional blocks of logic are:

- 1) Byte Carry Detector module designated as the LOM306A logic card.
- 2) Channel Carry Generator which is implemented with general purpose logic cards.
- 3) LOM303A 2-bit adder cards.
- 4) LOM304A 2-bit adder cards.
- 5) LOM303A 2-bit adder cards.

The time delay through any one 6-bit byte channel is 126 nanoseconds ± 36 nanoseconds. Since all channels operate in parallel the total adder delay required to form the sum of any two numbers from 1 to 72 bits in length will be the same as the delay for longest channel.

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GE-645 PROCESSOR

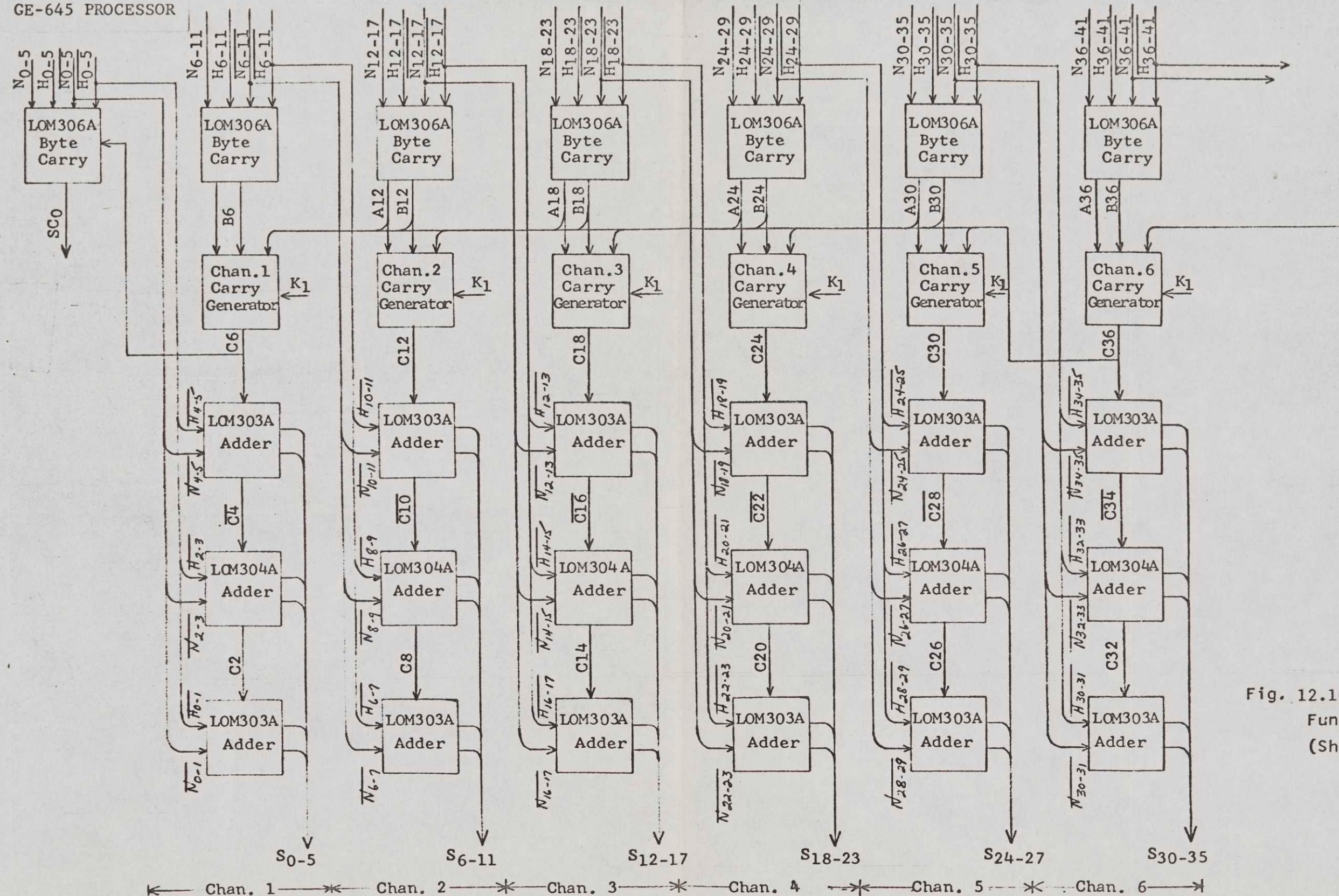


Fig. 12.10.1 S Adder
Functional Block
(Sh 1 of 2)

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GE-645 PROCESSOR

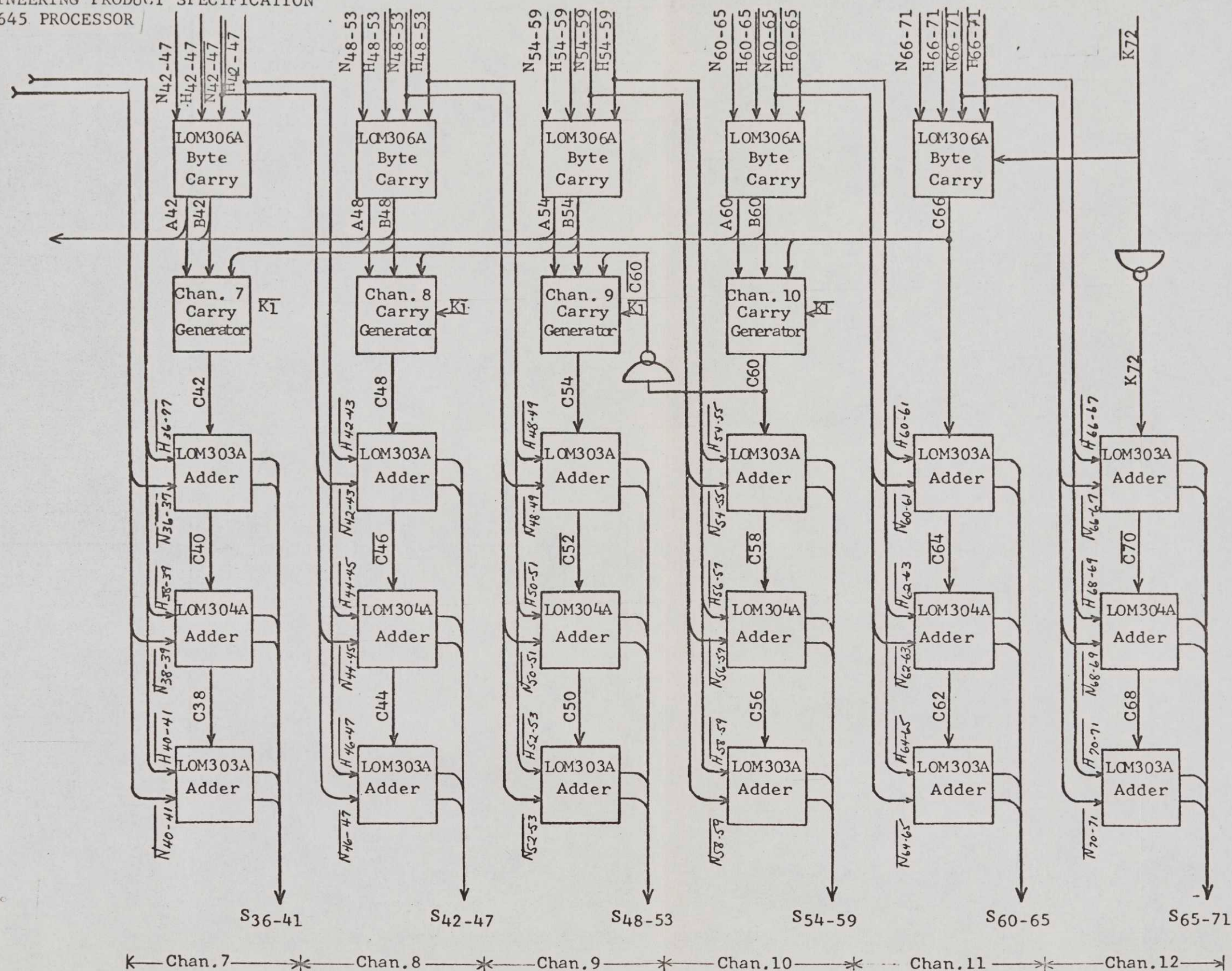


Fig. 12.10.1 S Adder
Functional Block
(Sh 2 of 2)

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Spec. No. M50EB00107

Cont. on Sh.12-338 Sh. No.12-337

TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR

12.10.2 LOOK AHEAD CARRY

This feature of the adder makes the above mentioned speed possible. It consists of the Byte Carry Detector and the Channel Carry Generator.

The function of each Byte Carry Detector module is to determine whether the two byte operands of the next higher numbered channel will produce a carry that should be added to this channel. The outputs, designated A_{6n} and B_{6n} , indicate the result of the byte carry detection as follows:

A_{6n}	B_{6n}	
1	1	an unconditional carry into this channel.
1	0	a carry into this channel only if the next higher numbered channel has a carry into it.
0	X	no carry into this channel.

The Byte Carry Detector for channel n examines the two byte operands entering channel $n + 1$. If the two byte operands have a sum equal to or greater than 2^6 , the A_{6n} and B_{6n} outputs will both be a "1" denoting that a carry is to be entered into channel n . If the two byte operands have a sum exactly equal to $2^6 - 1$, the A_{6n} output will be a "1" and the B_{6n} output will be a "0" denoting that a carry is to be entered into channel n only if a carry is entered into channel $n + 1$. If the two byte operands have a sum less than $2^6 - 1$, the A_{6n} output will be a "0" denoting that no carry is to be entered into channel n regardless of the state of B_{6n} or the carry into channel $n + 1$. There are 12 Byte Carry Detector modules. Channel 12 does not require one as there is no higher numbered channel from which to detect a carry.

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PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh.12-339 Sh. No. 12-338

TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR

12.10.2 - contd

However, a Byte Carry Detector is used to determine if there is a carry out of channel 1 (that is, out of the adder). Figure 12.10.2 shows the logic circuit implementation of the Byte Carry Detector. Pin 41 will be open on all detectors except channel 11 where it will be K₇₂ and the detector for SC₀ where it will be C₆.

Note that each Byte Carry Detector examines only the operand bytes of channel $n + 1$ and as such each detector is operating independently of all other detectors. This is the first stage of the S Adder carry look-ahead network. The Channel Carry Generators perform a second and final stage of carry look-ahead.

The function of the Channel Carry Generator is to examine the outputs of its Byte Carry Detector and the outputs of all Byte Carry Detectors of higher numbered channels to determine whether or not a carry is to be inserted into its channel. The output of the Channel Carry Generator (C_{6n}) will be active if A_{6n} of its Byte Carry Detector is active and either B_{6n} of its detector is active or there is a carry from channel $n + 1$. This logic is implemented so that the carry C_{6n} can be generated within two logic levels. It should be noted that all carries C_{6n} will be inhibited by K₁ set. There are only 10 Channel Carry Generator modules. Channel 12 derives its carry input from K₇₂ and channel 11 derives its carry input from its Byte Carry Detector.

Every sixth carry for the 72-bit addition is produced by the carry look-ahead network. Each carry is then fed into a 6-bit adder which consists of three 2-bit adder modules in cascade.

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Spec. No. M50EB00107

Cont. on Sh.12-340 Sh. No.12-339

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GE-645 PROTOTYPE PROCESSOR

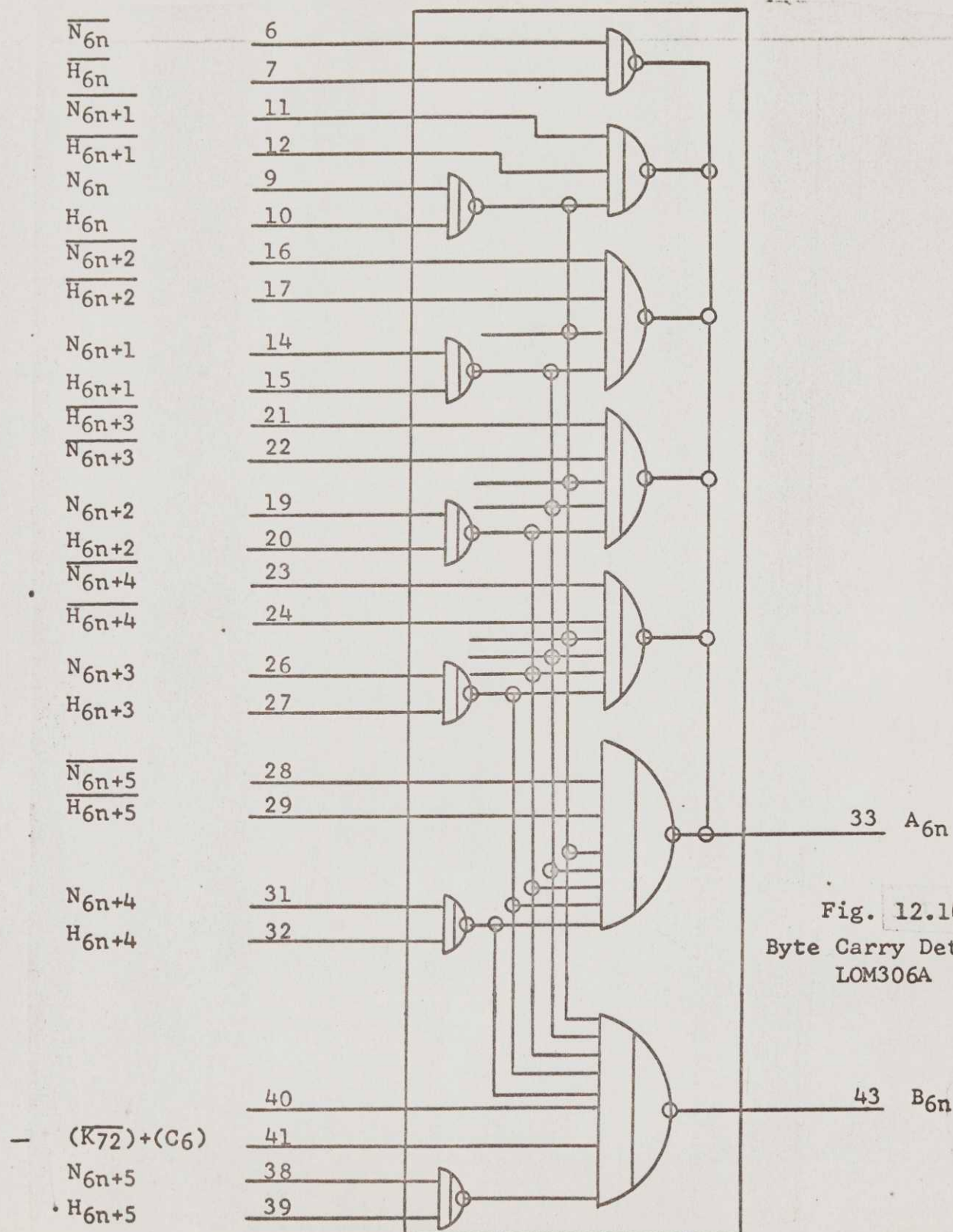


Fig. 12.10.2
Byte Carry Detector
LOM306A

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Spec. No. M50EB00107

Cont. on Sh.12-341 Sh. No.12-340

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

12.10.3 ADDER MODULES

There are two types of adder modules - LOM303A and LOM304A. Each adder module processes two bits of the two byte operands. The only difference in the two modules is in the carry network. Figure 12.10.3a is a functional block diagram of the LOM303A adder module. This gives an over-all picture of how the module works. Each block will be described in detail.

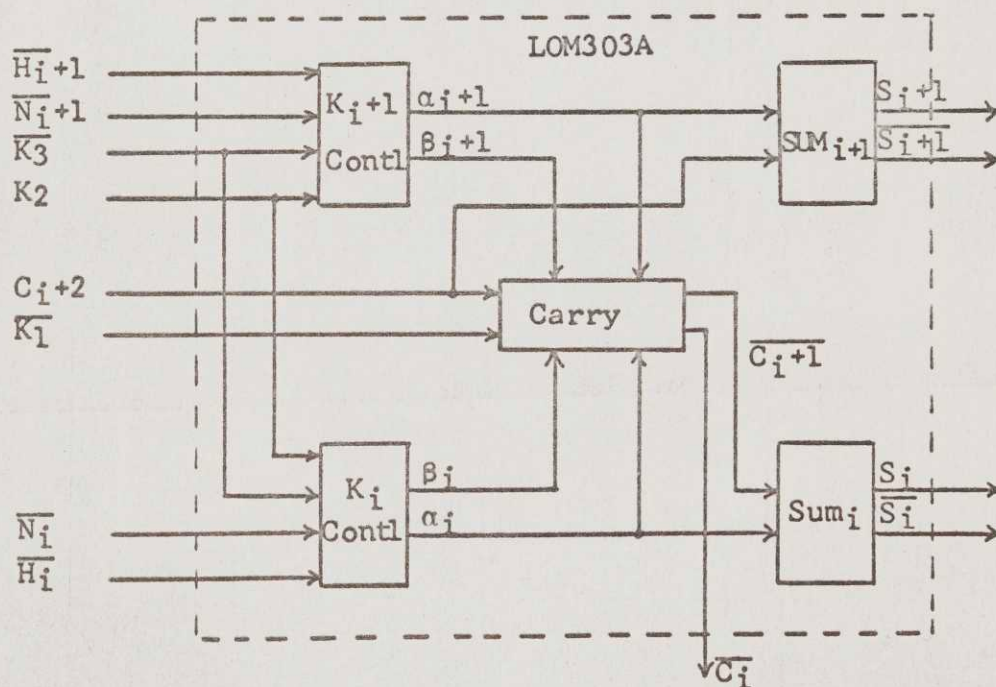


Fig. 12.10.3a
LM303A Adder, Block Diagram

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PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh.12-342 Sh. No.12-341

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

12.10.3 - contd

It might be wise at this time to discuss the implementation of the K flip-flops. As stated before K_1 , K_2 , and K_3 determine what function the adder performs. To cause this function to occur in the adder cards it is necessary to take some control signals from the "1" side of the flip-flop and some from the "0" or L side. Below is a table for both the LOM303A and the LOM304A.

<u>K Register</u>			<u>Function</u>
K_1	K_2	K_3	
0	0	0	Add
1	0	0	Exclusive OR
1	1		Inclusive OR
1	0	1	AND

LOM303A			Pin	Pin	Pin
			19	14	16
			$\overline{K_1}$	K_2	$\overline{K_3}$
Add			+6	0	+6
Exclusive OR			0	0	+6
Inclusive OR			0	+6	+6
AND			0	0	0

LOM304A			Pin	Pin	Pin
			24	14	16
			K_1	K_2	K_3
Add			0	0	+6
Exclusive OR			+6	0	+6
Inclusive OR			+6	+6	+6
AND			+6	0	0

Figure 12.10.3b shows the implementation of the $K_1 + 1$ control portion of the adder module.

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PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh.12-343 Sh. No.12-342

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

12.10.3 - contd

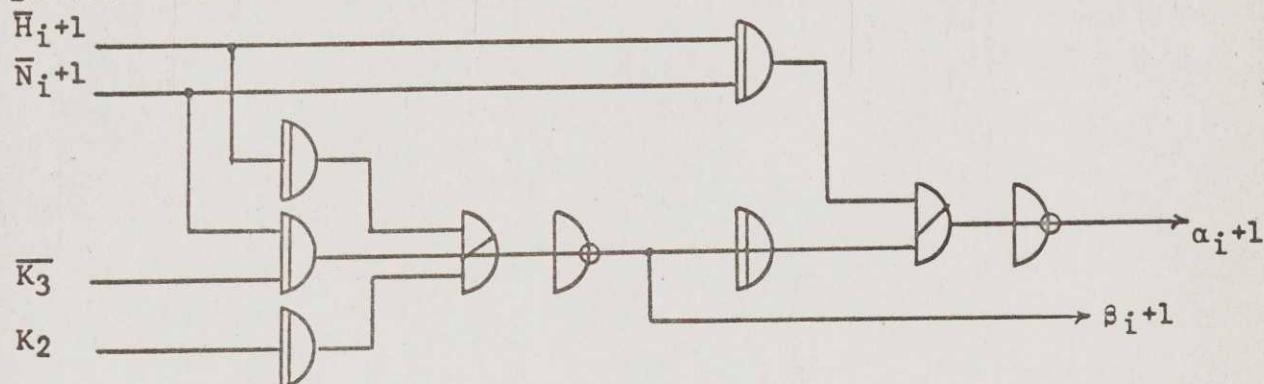


FIG. 12.10.3b LM303A K_{i+1} Control, Logic Diagram

The two outputs of this circuit can best be described by use of a truth table.

Operation	H,N	$\bar{H},N$	H, $\bar{N}$	$\bar{H},\bar{N}$
Add ($\bar{K}_1, \bar{K}_2, \bar{K}_3$)	$\alpha_{i+1}, \beta_{i+1}$	$\alpha_{i+1}, \beta_{i+1}$	$\alpha_{i+1}, \beta_{i+1}$	$\alpha_{i+1}, \beta_{i+1}$
Exclusive OR ($K_1, \bar{K}_2, \bar{K}_3$)	$\alpha_{i+1}, \beta_{i+1}$	$\alpha_{i+1}, \beta_{i+1}$	$\alpha_{i+1}, \beta_{i+1}$	$\alpha_{i+1}, \beta_{i+1}$
Inclusive OR (K_1, K_2, K_3)	$\alpha_{i+1}, \beta_{i+1}$	$\alpha_{i+1}, \beta_{i+1}$	$\alpha_{i+1}, \beta_{i+1}$	$\alpha_{i+1}, \beta_{i+1}$
AND ($K_1, \bar{K}_2, K_3$)	$\alpha_{i+1}, \beta_{i+1}$	$\alpha_{i+1}, \beta_{i+1}$	$\alpha_{i+1}, \beta_{i+1}$	$\alpha_{i+1}, \beta_{i+1}$

The outputs of this circuit become the inputs to the carry and sum circuits. The circuit for α_i and β_i is identical to the one shown above.

Figure 12.10.3c shows the implementation of the $C_i + 1$ carry.

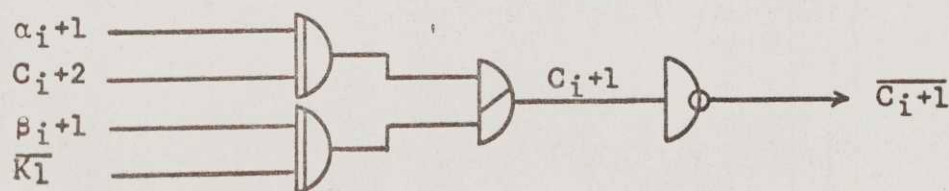


FIG. 12.10.3c LM303A C_{i+1} Carry, Logic Diagram

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Spec. No. M50EB00107

Cont. on Sh.12-344 Sh. No.12-343

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

12.10.3 - contd

$C_i + 2$ is the carry out of the next higher number bit position. It can be the carry output of a LOM304A adder module (C_2 , C_8 , etc.), the carry output of a Channel Carry Detector (C_6 , C_{12} , etc.), the carry output of a Byte Carry (C_{66}), or K_{72} . From this diagram it can be seen that if K_1 is set the carry $C_i + 1$ will depend upon receiving a carry in $C_i + 2$, which in turn will depend upon receiving a carry in, etc. all the way back to K_{72} . If K_{72} is reset, as it will be for all non-add operations, no carries will be generated. If an Add operation is in progress $C_i + 1$ will be true if $B_i + 1$ is true or if $a_i + 1$ is true and there is a carry in. Checking the truth tables for the K control reveals that $C_i + 1$ will be true under the following conditions:

- a) $(N_i + 1) (H_i + 1)$
- b) $(\overline{N_i + 1}) (H_i + 1) (C_i + 2)$
- c) $(N_i + 1) (\overline{H_i + 1}) (C_i + 2)$

$C_i + 1$ is used as an input to the Sum logic for S_i .

Figure 12.10.3d shows the implementation of the C_i carry.

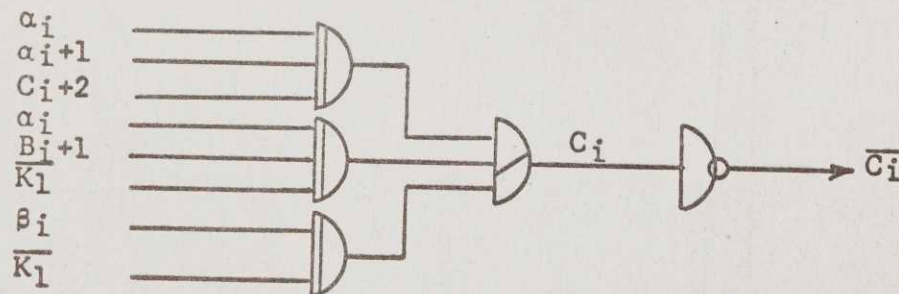


Fig. 12.10.3d

LM303A C_i Carry, Logic Diagram

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TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

For the same reasons as for $C_i + 1$, no carries (C_i) will be generated for non-add operations. For Add operations it was seen that $C_i + 1 = \beta_i + 1 + (\alpha_i + 1) (C_i + 2)$. These same terms are used in the generation of C_i . If they are replaced by $C_i + 1$ then $C_i = (\alpha_i) (C_i + 1) + \beta_i$. In effect the $C_i + 1$ network is reproduced and α_i added. This was done to speed up the generation of C_i . For an Add operation C_i will be true under the following conditions:

- $$\begin{aligned} \text{a)} & \quad (N_i) (H_i) \\ \text{b)} & \quad (\overline{N_i}) (H_i) (C_i + 1) \\ \text{c)} & \quad (N_j) (\overline{H_i}) (C_i + 1) \end{aligned}$$

$\overline{C}_i$ is the carry output of the LOM303A adder module. It should be noted that the LOM303A requires a true carry input and generates the false carry output.

Figure 12.10.3e shows the implementation of the $\text{Sum}_i + 1$ logic.

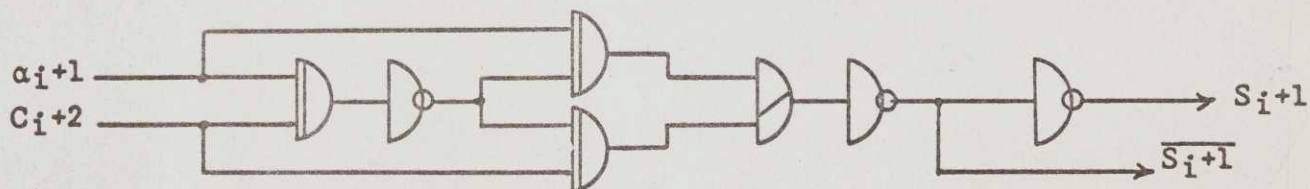


FIG. 12.10.3e LM303A $\text{Sum}_i + 1$, Logic Diagram

From this it can be seen that $S_i + 1$ will be true only if the two inputs ($a_i + 1$ and $C_i + 2$) are not the same. By using the previous information a truth table can be constructed for all operations.

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Spec. No. M50EB00107

Cont. on Sh.12-346 Sh. No.12-345

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

12.10.3 - contd

	H_{i+1}, N_{i+1}	$\overline{H_{i+1}}, \overline{N_{i+1}}$	$H_{i+1}, \overline{N_{i+1}}$	$\overline{H_{i+1}}, N_{i+1}$
Add $\overline{C_i+2}$	$\overline{S_i+1}$	S_i+1	S_i+1	$\overline{S_i+1}$
Add C_i+2	S_i+1	$\overline{S_i+1}$	$\overline{S_i+1}$	S_i+1
Exclusive OR $\overline{C_i+2}$	$\overline{S_i+1}$	S_i+1	S_i+1	$\overline{S_i+1}$
Inclusive OR $\overline{C_i+2}$	S_i+1	S_i+1	S_i+1	$\overline{S_i+1}$
AND $\overline{C_i+2}$	$\overline{S_i+1}$	S_i+1	$\overline{S_i+1}$	$\overline{S_i+1}$

At first glance it would seem that the output will be wrong for the AND operation, however, during an AND operation the ones complement of the operand from memory is stored in H to make the output of the Adder correct.

The Sum_i logic is the same as in Fig. 12.10.3e except that the inputs will be a_i and $\overline{C_i+1}$ and the outputs will be reversed. A truth table can be constructed for this logic. It will be the same as the one for S_i+1 .

The LOM304A adder module is similar to the LOM303A adder module. It requires a false carry input and it produces a true carry output. The circuitry differs only in the carry logic. Figure 12.10.3f is a functional block diagram of the LOM304A module.

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COMPUTER EQUIPMENT DEPARTMENT
PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh.12-347 Sh. No.12-346

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

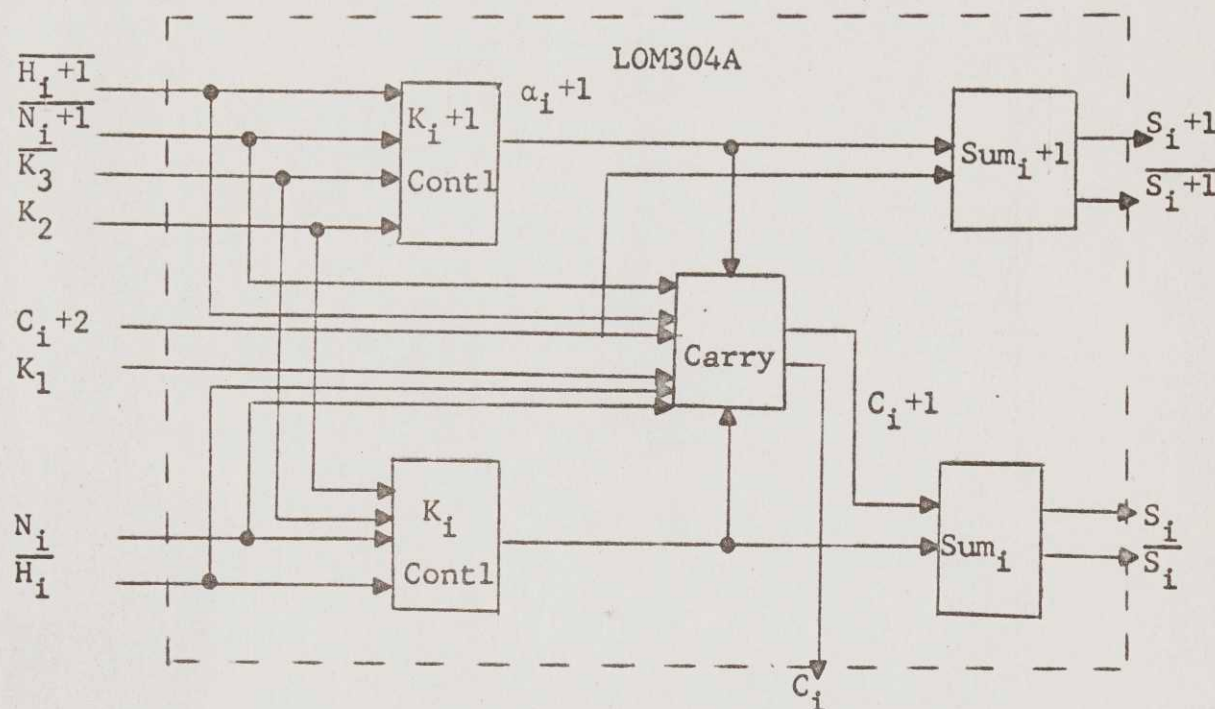


FIG. 12.10.3f LM304A, Block Diagram

The K control logic is identical to the K control logic of the LOM303A module. The β output is not used in the LOM304A. The truth table for the LOM303A will also apply for this module.

Figure 12.10.3g shows the implementation of the C_{i+1} carry.

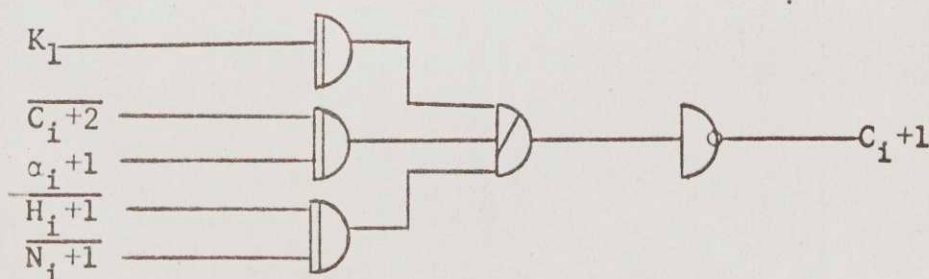


FIG. 12.10.3g LM304A, C_{i+1} Carry, Logic Diagram

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Spec. No. M50EB00107

Cont. on Sh.12-348 Sh. No.12-347

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

12.10.3 - contd

$C_i + 2$ is the carry out of the next higher numbered bit position. It will always be the output of a LOM303A module. From this diagram it can be seen that if K_1 is set $C_i + 1$ will always be false. If K_1 is reset, an Add operation, $C_i + 1$ will be true under the following conditions:

- a) $(H_i + 1) (N_i + 1)$
- b) $(\overline{H_i + 1}) (N_i + 1) (C_i + 2)$
- c) $(H_i + 1) (\overline{N_i + 1}) (C_i + 2)$

$C_i + 1$ is used as input to the Sum logic for $S_i + 1$.

Figure 12.10.3h shows the implementation of the C_i carry.

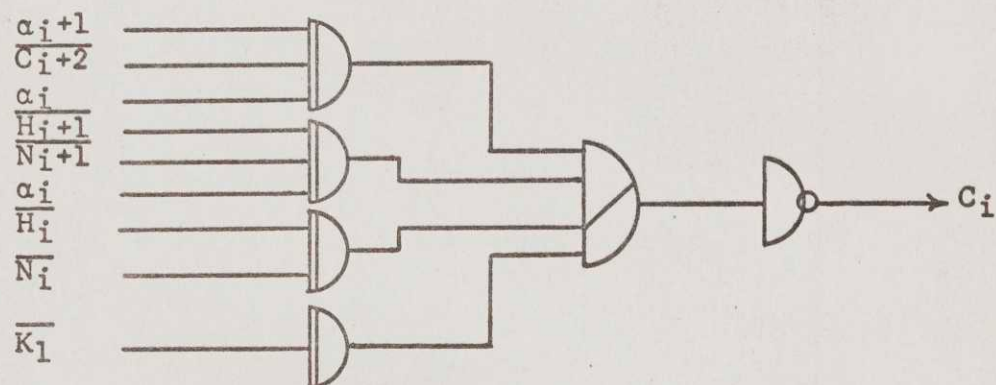


FIG. 12.10.3h LM304A C_i Carry, Logic Diagram

If K_1 is set (all non-add operations) C_i will always be false. During Add operations if any one of the other three gates is satisfied C_i will be false. The truth table follows.

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Spec. No. M50EB00107

Cont. on Sh.12-349 Sh. No.12-348

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

12.10.3 - contd

		(α_i+1)	(α_i+1)	
If C_i+2	H_i+1, N_i+1	H_i+1, N_i+1	H_i+1, N_i+1	H_i+1, N_i+1
$H_i N_i$	C_i	C_i	C_i	C_i
$\overline{H_i} N_i (\alpha_i)$	C_i	C_i	C_i	$\overline{C_i}$
$H_i \overline{N_i} (\alpha_i)$	C_i	C_i	C_i	$\overline{C_i}$
$\overline{H_i} \overline{N_i}$	$\overline{C_i}$	$\overline{C_i}$	$\overline{C_i}$	$\overline{C_i}$

If $\overline{C_i}+2$

$H_i N_i$	C_i	C_i	C_i	C_i
$\overline{H_i} N_i (\alpha_i)$	C_i	$\overline{C_i}$	$\overline{C_i}$	$\overline{C_i}$
$H_i \overline{N_i} (\alpha_i)$	C_i	$\overline{C_i}$	$\overline{C_i}$	$\overline{C_i}$
$\overline{H_i} \overline{N_i}$	$\overline{C_i}$	$\overline{C_i}$	$\overline{C_i}$	$\overline{C_i}$

C_i is the carry output of the LOM304A adder module.
This module requires a false carry input and generates
a true carry output.

The S_i and $S_i +1$ logic is identical to the LOM303A
logic except that the output points are reversed. The
same truth table applies here.

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Spec. No. M50EB00107

Cont. on Sh.12-350 Sh. No.12-349

TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR

12.11 FLOW DIAGRAMS AND ALGORITHM DESCRIPTION

Figure 12.11	Flow Diagram for MPY (Integer Multiply)
Figure 12.11a	Flow Diagram for DIV (Integer Divide)
Figure 12.11b	Flow Diagram for BCD (Binary to Binary Coded Decimal)
Figure 12.11c	Flow Diagram for FAD (Floating Add)

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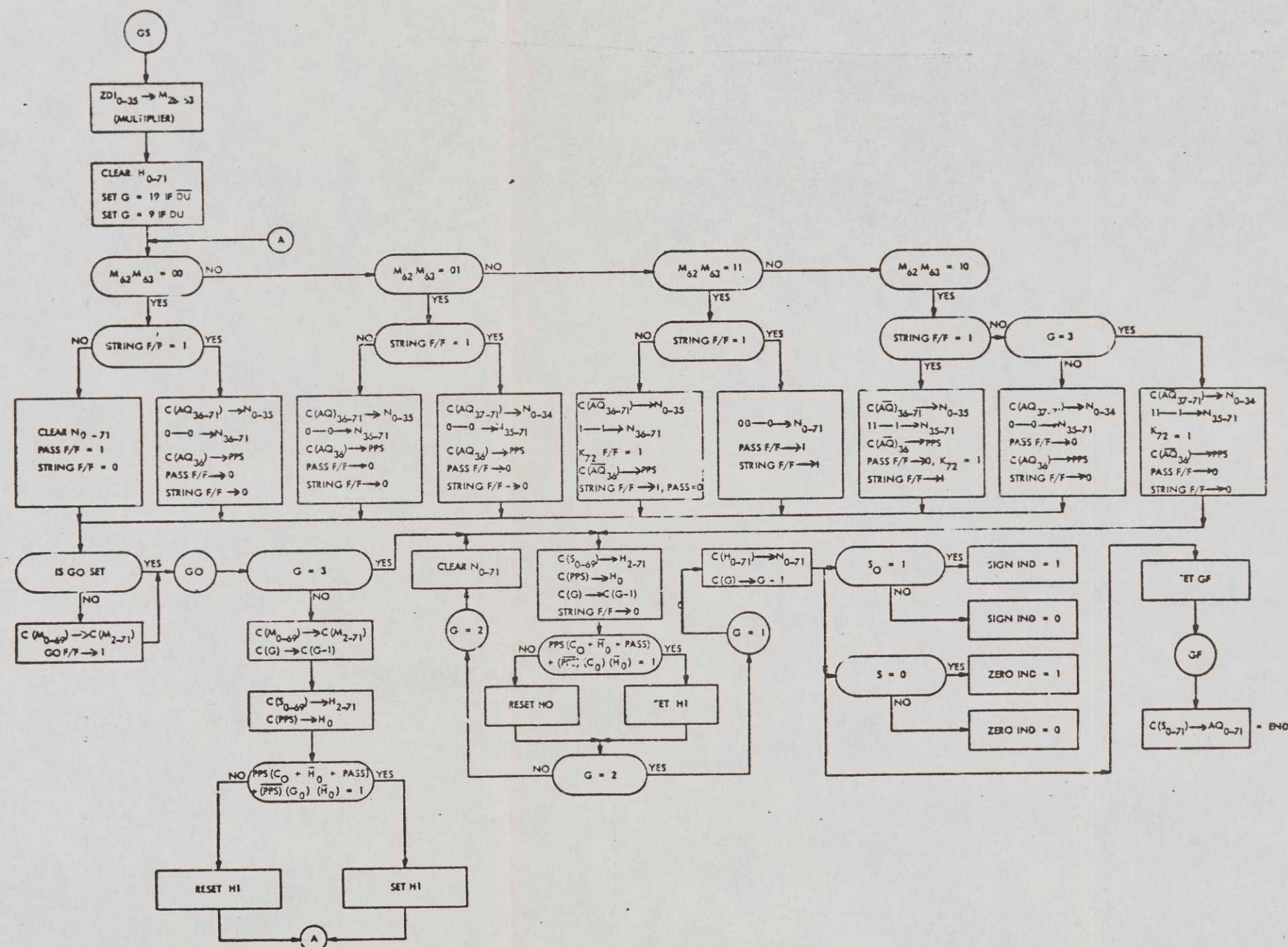


FIG. 12.11 FLOW DIAGRAM FOR MPY (INTEGER MULTIPLY)

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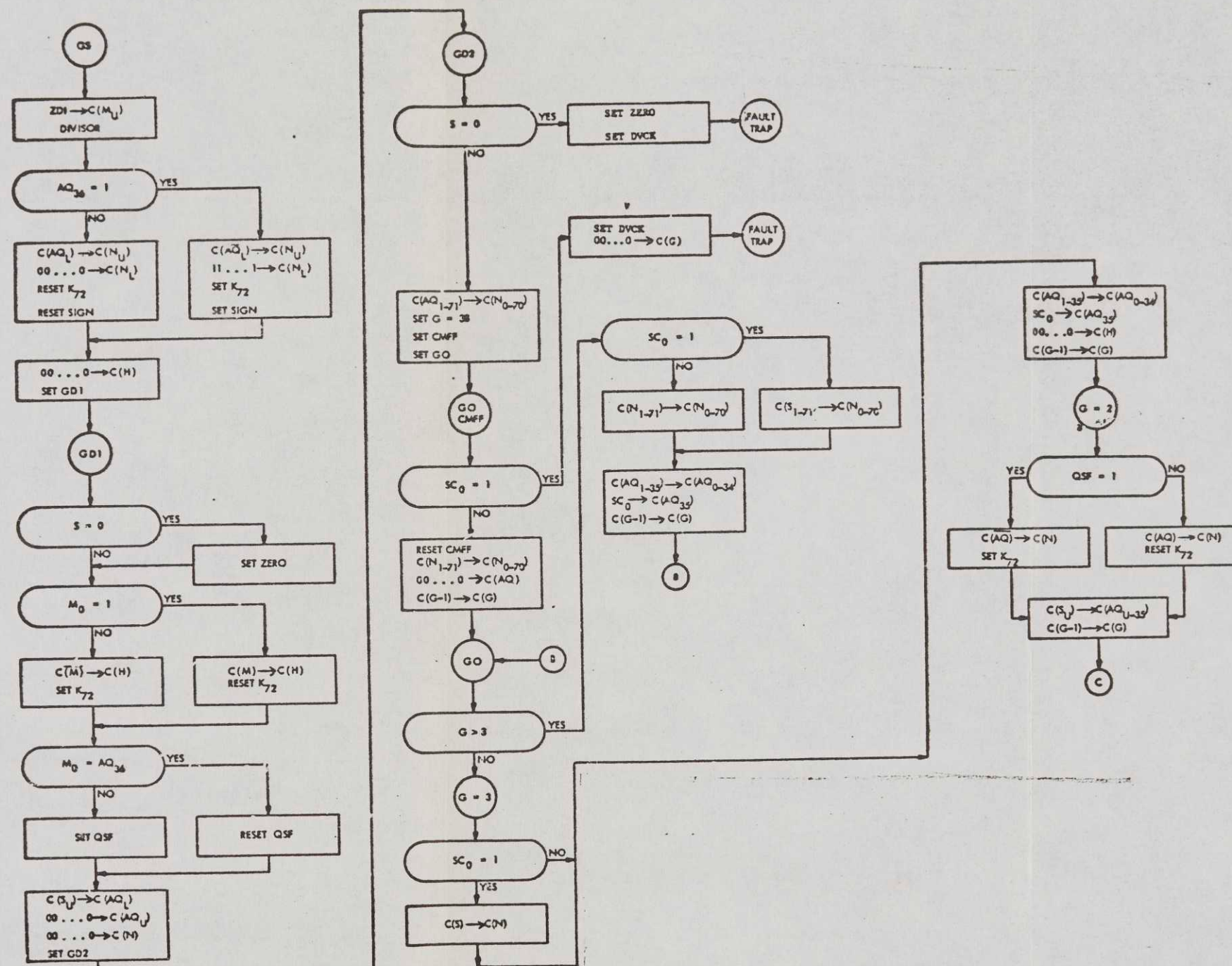


FIG. 12.11a FLOW DIAGRAM FOR DIV (INTEGER DIVIDE)

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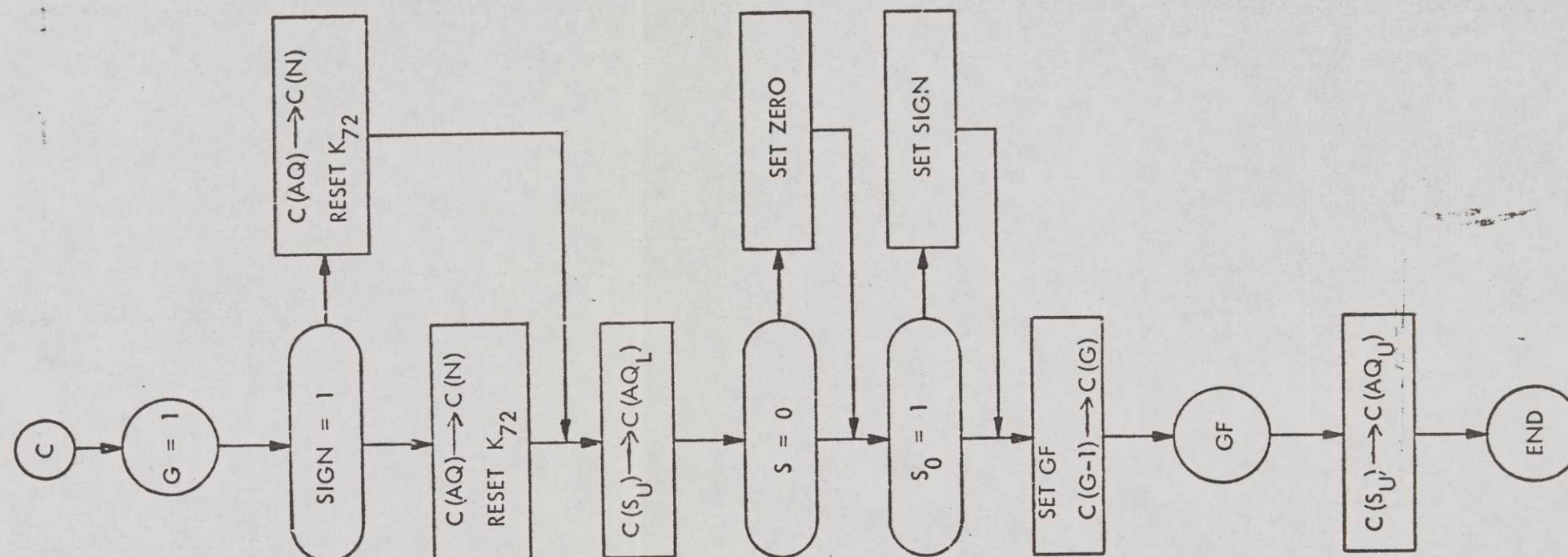


FIG. 12.11a FLOW DIAGRAM FOR DIV (INTEGER DIVIDE)

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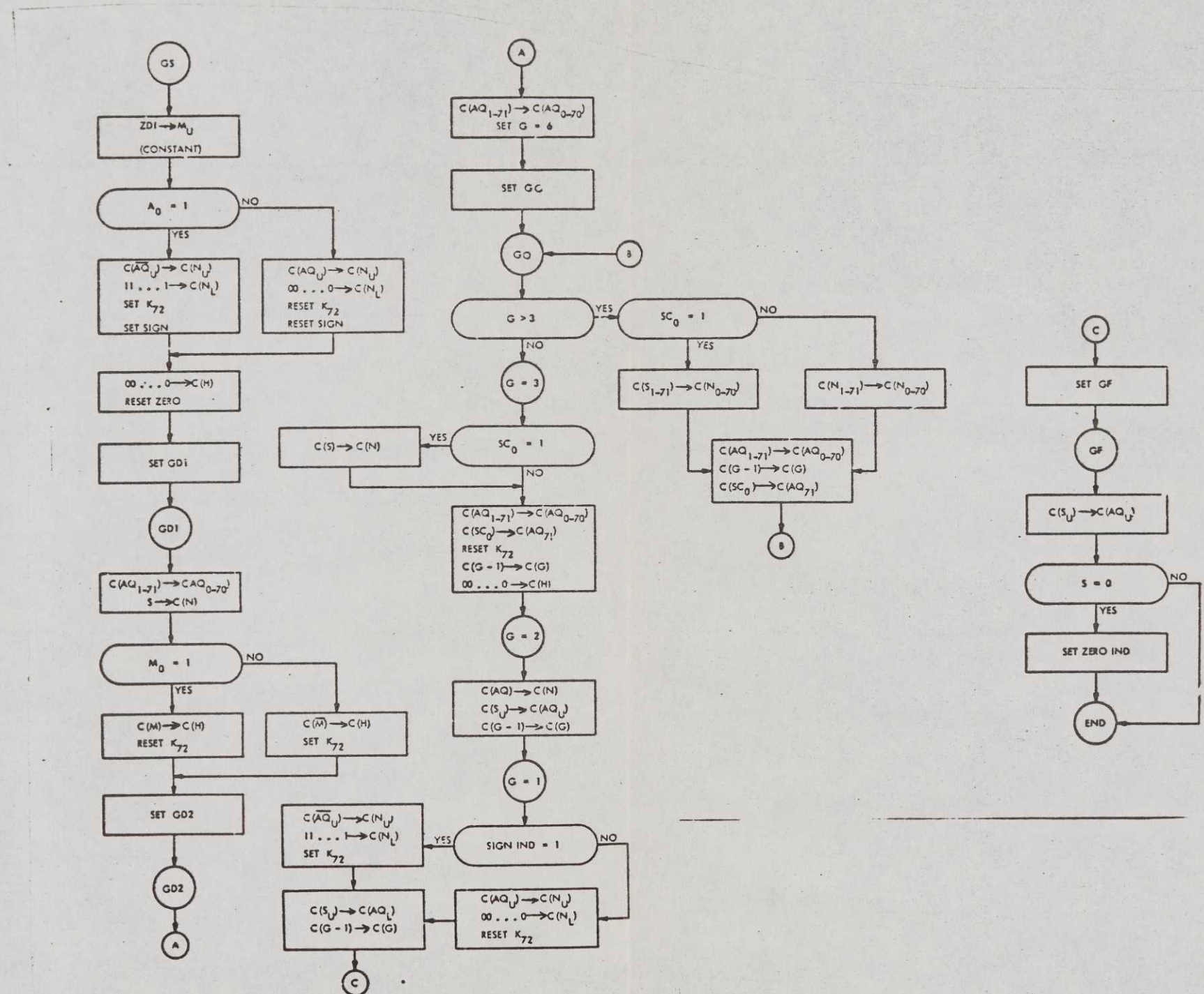


FIG. 12.11b FLOW DIAGRAM FOR BCD (BINARY TO BINARY
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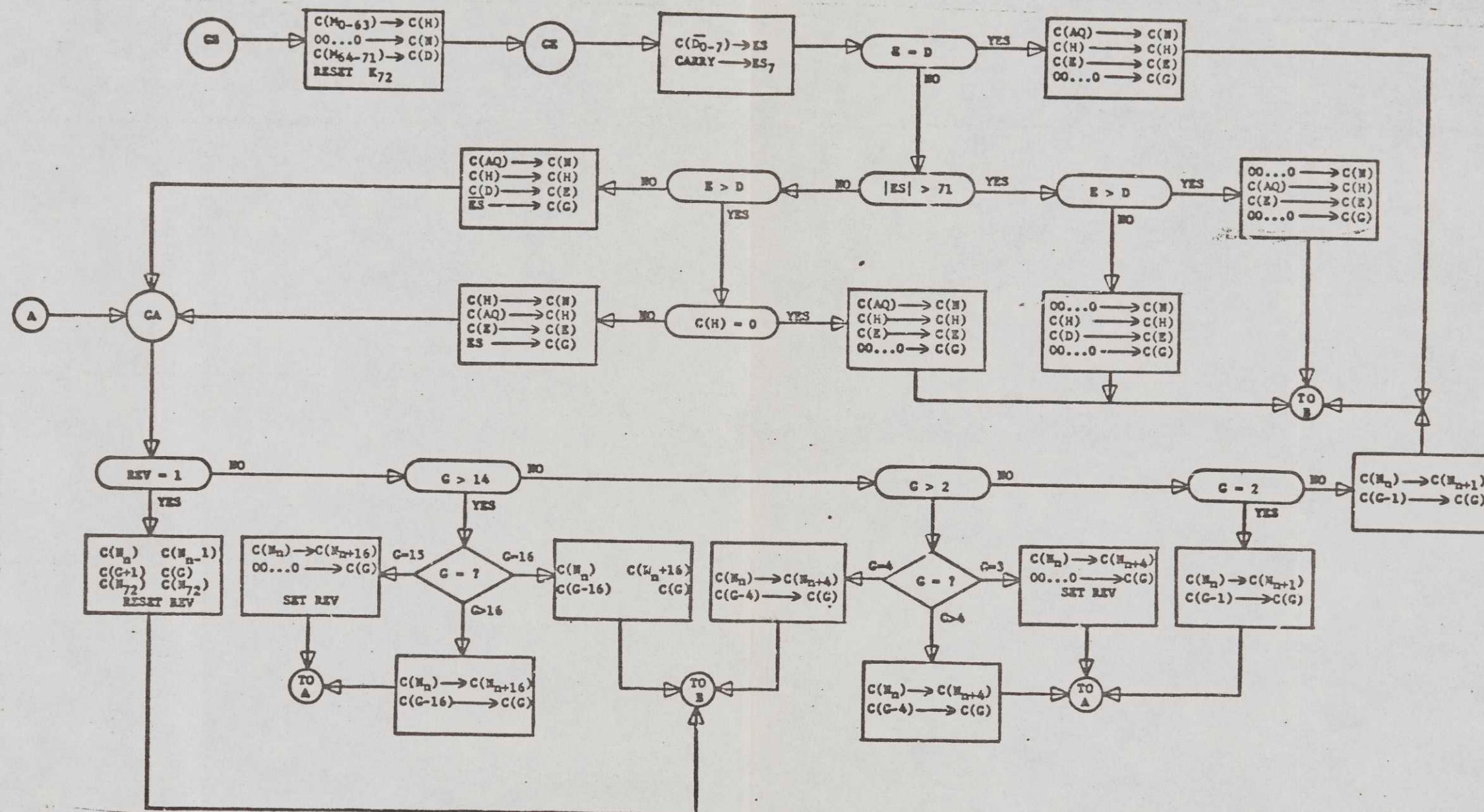


FIG. 12.11c FLOW DIAGRAM FOR FAD (FLOATING ADD)

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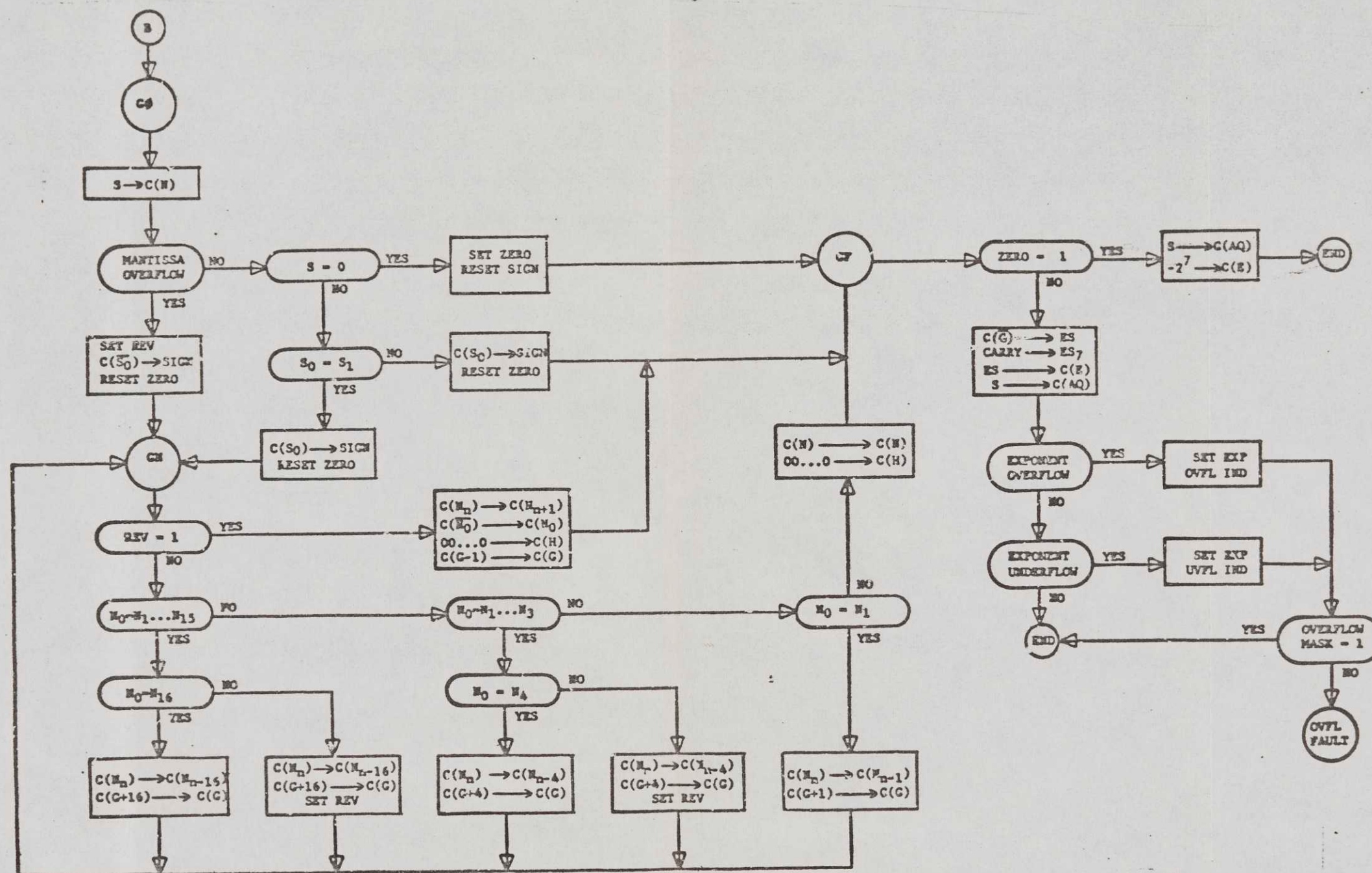


FIG. 12.11c FLOW DIAGRAM FOR FAD (FLOATING ADD)

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Cont. on Sh. 13-2 Sh. No. 13-1

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GE-645 PROTOTYPE PROCESSOR

13.0 MAINTENANCE

The whole philosophy of maintenance of the GE-645 Prototype Processor is still to be determined. This information will evolve out of problems encountered during the debug and checkout phases of the hardware and T&D programs and evolution at the prototype site. Until that time, the information available on the Processor Maintenance Panel in Section 3.0 is the only information pertaining to maintenance in this EPS.

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GE-645 PROTOTYPE PROCESSOR

RELEASES AND APPROVALS for: Sections 7 through 13.

This document was prepared by the GE-645 Project P. & C.E., General Electric Computer Equipment Department, Phoenix, Arizona. In the process of preparing this document, the GE-645 Project has been transferred and is now the responsibility of GE-645 Equipment Design, ACP Section, Special Information Products Department, Phoenix, Arizona.

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